Developing high-bandwidth digital data transmission for next-generation $0\upsilon\beta\beta$ detections

Qing Xia

1.Introduction

nEXO is a next generation neutrinoless double beta decay ($0\upsilon\beta\beta$) experiment using ^{136}Xe with substantially improved sensitivity compared to EXO-200. It will be able to observe neutrinoless double beta decay if it occurs with a half-life below ~10^{28} years [1].

I propose to develop prototype high-speed cables with low radio-activity for signal transmission in the nEXO detector. Aside from applications in $0\upsilon\beta\beta$ experiments, those cables can be used in a large number of future low background experiments searching for dark matter and other rare processes. These next-generation experiments require substantially more electronics channels due to higher data rates. For instance, liquid noble time projection chambers like the large Ar detector of the Deep Underground Neutrino Experiment (DUNE) will also be using cold digital electronics. nEXO in particular, requires 2 orders of magnitude higher data rates than its precursor. However, so far there has been no commercial high bandwidth digital cable which has low enough radioactivity for use in low-background like $0\upsilon\beta\beta$ and dark matter experiments. The instrument I am going to develop consists of an Application-specific integrated circuit (ASIC) developed at BNL, copper microstrip transmission lines on a Kapton substrate, together with warm and cold feedthroughs for the cables transitioning from the liquid xenon volume to the cryostat insulation vacuum and from the vacuum to the external atmosphere.

I expect this project to take two years, with optimizing the cable and feedthrough in the first year, and testing with the BNL electronics in the second year. The end product will be a readout system for the nEXO detector composed of flexible cables and interconnecting circuits, which will have broad applications in the next-generation low-background experiments.

2. Motivation and Prior Art

The current generation of low background experiments are using analog cables that transmit signals to room temperature digital electronics, and a radiopure digital cable does not yet exist. The precursor of the nEXO experiment -- the EXO-200 experiment chooses to use Espanex flat cable MC18-25-00CEM, lot G5C03-23L2 manufactured by Nippon Steel Chemical Co. [2]. It has a ^{40}K concentration of$<146*10^{-9}$g/g, ^{232}Th of $<260*10^{-12}$g/g, and ^{238}U of $<46*10^{-12}$g/g. The choice fell on Kapton flat cables for the following reasons [3]: First, they have largest bandwidth per unit radioactivity compared to twisted pairs of wires used in Ethernet, etc.; Second, they allow access and connections in the very limited space behind the charge collection plane so that active xenon volume can be maximized; Third, they allow for complicated routing into the cable conduits.

On the other hand, the Cryogenic Underground Observatory for Rare Events (CUORE), a neutrinoless double beta decay search experiment a Gran Sasso National Laboratory, selects Cu-PEN (Copper on a Polyethylene 2.6 Naphthalate subtrate) for analog flex cables between the thermistors and the front-end amplifiers [4]. The GERmanium Detector Array (GERDA) experiment uses flexible flat cables made from Pyralux or Cuflon to connect the Ge readout electrode and the JFET-PCB [5]. However, none of these existing cables can meet the requirements for next-generation TPCs with cold digital electronics.

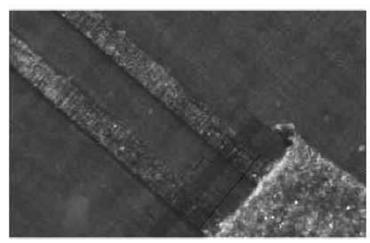
The nEXO experiment is going to have a tonne-scale liquid xenon detector, with an output data rate 2 orders of magnitude higher than EXO-200. Therefore, custom high-speed flat cables need to be tested before utilizing to guarantee the integrity of transmitted signals. Since the cables are light weight but very close to the detector center, they are required to have low-radioactivity to avoid contamination of the liquid xenon detector, as well as low outgassing of electronegative impurities to maintain the electron-lifetime of the charge signal.

3.Technical Details

To test the basic concept of this proposal, a prototype cable was fabricated and preliminary studies using microscope and Time Domain Reflectometry (TDR) have proved the manufacturing of the transmission lines to be quite satisfactory. No apparent discontinuities or tapering have been observed (Fig. 1b). The major loss of the cables comes from the resistive effect of the microstrip transmission lines, which can be reduced in a low-temperature environment.

The TDR setup consists of a pulse generator--PicoScope 9211A, a printed circuit board which connects the signal generator and the cables, and 3 pairs of cables with different lengths on a 0.05mm thick Kapton dielectric material, as is shown in Fig. 1a. The PicoScope operates at a bandwidth of 12 GHz and has a rise time of 100ps to 130ps. The PCB miniboard is made of a 59 mil FR-4 expoxy glass with a dielectric constant between 4.2 and 5.0. Each cable under test is soldered to the circuit board, and there's a 71.5Ω termination between each differential pair to prevent large voltage reflection.

(a)

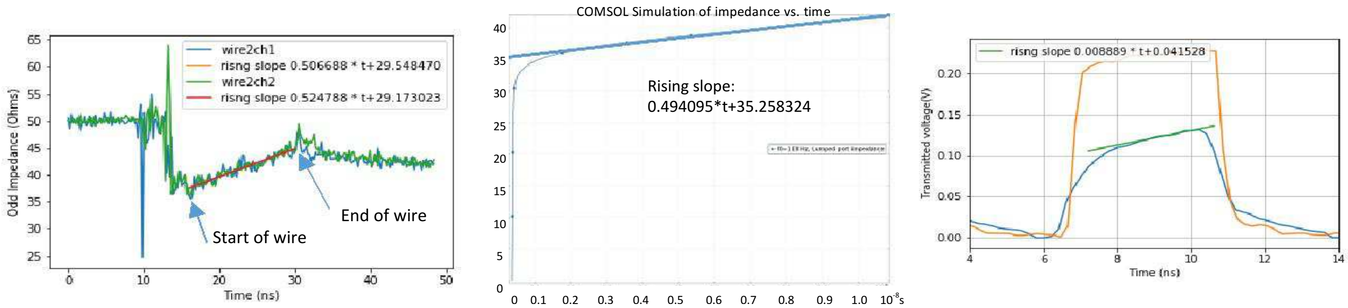


(b)

Fig. 1 (a) 3 pairs of transmission lines under test in the preliminary study. (b)Coupled transmission lines under microscope. No apparent discontinuities or tapering have been observed.

The theoretical calculation shows the cable under test in our experimental setup has a characteristic odd impedance of 39.2Ω [6]. This value is consistent with the TDR measurements carried out on 3 pairs of transmission lines. The result of one of them is shown in Fig. 2a, which indicates a characteristic impedance of 37Ω.

The huge spikes in the impedance vs. time plot are caused by impedance mismatch at the interconnecting surface between the wires under test and the coaxial cables. The slope in the plot can be expressed as $Z_c(t) = Z_0(1+\frac{t}{\tau})$ for t<< τ, where Z_0 is the characteristic impedance (~37Ω) and $\tau = \frac{2L}{R} - \frac{2C}{G}$ [7]. In our experimental setup, τ~100ns. R (~4Ω/m) is measured using a multimeter, G(6*10^{-4}S/m) can be estimated from the loss tangent measurement [8], while L (~2*10^{-7}H/m) and C (~1.5*10^{-10} S/m) are calculated by COMSOL finite element simulation. Therefore, the theoretical value of the impedance slope is 0.33Ω/ns, in which the resistive effect R contributes 0.4Ω/ns, and the shunt conductance G contributes -0.072Ω/ns. Thus the theoretical calculation is roughly consistent with the measured slope ($0.5\Omega/ns$). The COMSOL simulation of impedance vs. time in Fig. 2b also shows a similar slope of $0.49\Omega/ns$



(a) (b) (c)

Fig. 2 (a) TDR measurements of the cable's impedance. The characteristic impedance is measured to be 37 Ω. The slope in the impedance vs. time is caused by resistive loss in the cable. (b) COMSOL simulation of measurement (a). A similar slope shows up in the TDR simulation. (c) Measured input (orange) and transmission pulse signal (blue). The gap between the two is due to loss and impedance mismatch between the microstrip transmission lines and the signal generator's coaxial cables.

The next steps will be:

1.Design new cables with proper length, thickness, and correct impedance that match BNL electronics.

The longest cable in our preliminary study is 2m. The nEXO detector may need a longer cable in reality, so the length needs to be optimized based on the detector design. According to the previous paragraph, the resistive effect plays a major role in the loss of transmission lines. This knowledge can help us improve its design. Increasing the thickness of the transmission line for example, will keep the impedance almost unchanged while reducing its resistance to a great extent. Another issue that remains to be resolved in our preliminary experiment is the impedance mismatching on the interface between the microstrip lines and the coaxial cables which connects to the signal generator. As is shown in Fig 2c, the amplitude of the transmitted pulse is only half of the input pulse. Given the relatively small loss of the transmission lines, this gap between input and output signal is more likely to have been caused by reflection at the beginning and the end of the wire.

Therefore, designing a cable with impedance that matches cold electronics, which consist of front-end mother boards (FEMBs) for ASIC evaluation and signal feedthroughs developed at BNL is crucial for signal transmission quality. More about the cold electronics will be demonstrated in step 3.

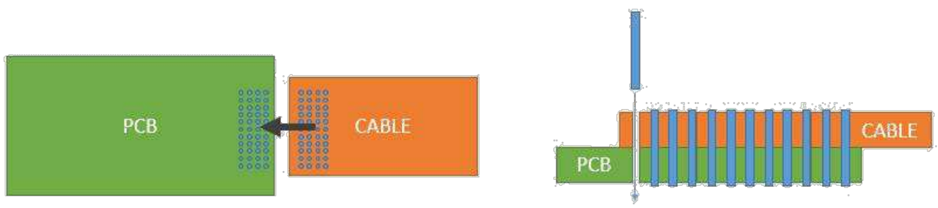
2. Design connection scheme and feedthrough that can interface with the cable.

Three methods of bonding cables to the printed circuit board (PCB) have been proposed [9]. The first option is bump bonding with the bonder machine shown in Fig.4, where the cable is mounted directly onto the PCB without using other connecting wires. The contact is established by beforehand applied bumps. Advantages of this method are the compactness and the low inductance, due to the short conductor lengths. However, we are not yet sure whether the Kapton cables or the quartz PCB can stand the 250°C temperature during the heating and compression process. The second option (Fig. 5a) is to drill similarly sized holes in Kapton cable and PCB, then press fit a pin between the two that will hold at the desired temperature. The third method (Fig. 5b) is wire bonding -- gluing the cable to the PCB as just a mechanical attachment, then wire bond from the cable to the board.

Cable bonding can be done using the equipment mentioned above in High Density Interconnects Lab at BNL. We can then study the signal integrity of our connected circuit by repeating the TDR test that has been done and looking at eye diagrams using a Time Domain Transmission (TDT) setup.

(a) (b)

Fig.4 (a) West Bond Bump Bonder: The device that deposits the bumps. (b)SEC Model 860 Eagle Omni Bonder: Aligns the two surfaces and applies heat and compression



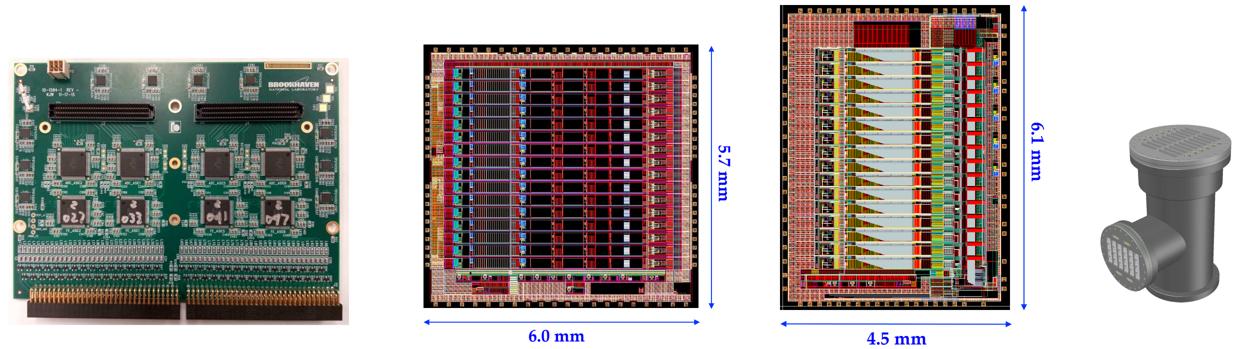
(a) (b)

Fig.5 (a) Connecting PCB and Kapton cable by pressing fit a pin between the two. (b) Wire bond between PCB and the cable. Figures are extracted from [9].

3. Integrate the cables with BNL cold electronics and demonstrate optimized cable and feedthrough performance.

The cold electronics have to be designed to thrive at a temperature of hundreds of degrees below zero in liquid noble detectors, which long past the range where conventional electronics in commercial devices like smartphones, can function. The advantages of cold electronics include [10]: It decouples the electrode and cryostat design from the readout design; the noise is independent of the fiducial volume, and is much lower than with warm electronic, because placing the electronics inside the detector tank reduces noise by shortening the path each signal has to travel before getting amplified. In the case of ProtoDUNE, CMOS in LAr has been measured to have less than half the noise as that at room temperature.

BNL has started CMOs cold electronics study since 2008 [10]. The FEMB designed for ProtoDUNE is composed of 8 16-channel front-end ASICs and 8 16-channel ADC ASICs, shown in Fig.6a,b,c. A cold FPGA is used for sending control programming into ASICs and streaming data out to warm electronics [11]. The feedthrough in Fig. 6d consists of a warm 14'' flange that warm interface electronics boards can plug in directly, and a 10'' flange for cold photon detector cables to plug in [12].



(a) (b) (c) (d)

Fig. 6 (a) FEMB used for cold evaluation tests of FE ASIC. (b) 16-channel low power and low noise cold analog front end ASIC. (c) 16-channel low power and 12-bit 2Msps ADC ASIC. (d) Schematic picture of feedthrough. Figures (a), (b), (c) are from [11], and (d) is from [12].

We expect to finish step 1 and 2 in the first year, and step 3 will be done in the second year with a publication by the end of that year.

4. Qualifications, Collaboration and Resources

I have the necessary preparation to undertake this project because the Wright Lab at Yale where I am working has the PicoScope 9211A signal generator and other hardware, along with the COMSOL simulation software that enable me to carry out measurements of the cable's impedance and RLGC parameters.

To proceed further in this work, I expect to collaborate with Mickey Chiu, Eric Raguzin and other nEXO collaborators in the instrumentation division at BNL. They have expertise in electronic connection and readout system for nEXO [10]. Eric has designed ASIC board to interface with nEXO charge electronics. Substantial expertise and equipment is available at BNL for electronic interconnections including wire bonding, bump bonding, etc. We will work together to integrate realistic cables into the system. The instrumentation division at BNL also has experts in high speed electronics and testing equipment with whom I can work.

I will make use of ASIC and feedthroughs for the cables developed at BNL to ensure smooth signal transitioning from the liquid xenon volume to the cryostat insulation vacuum and from the vacuum to the external atmosphere. Through collaboration with the experts at BNL, a prototype readout system for the nEXO experiment composed of flexible cables and interconnecting circuits is expected to be developed in two years. While this system will be designed specifically for nEXO, the demonstration of radiopure high-bandwidth cabling and interconnection techniques is relevant for many next-generation rare-event searches with large channel counts and high-speed digital electronics.

Reference

[1] J.B.Albert et.al. , Sensitivity and discovery potential of nEXO to neutrinoless double beta decay. arXiv:submit/2036443,2017

[2] D.S. Leonard, Systematic study of trace radioactive impurities in candidate construction materials for EXO-200. arXiv:0709.4524v2,2008

[3] A. Pocar, Flat cables for EXO-200. AIS-SLAC-December 10, 2008

[4] C.Broferio, Electrical characterization of the low background Cu-PEN links of the CUORE experiment. Nuclear Instruments and Methods in Physics Resarch A 718, 211-212, 2013

[5] The GERDA Collaboration, Upgrade for Phase II of the GERDA Experiment. arXiv:1711.01452v1, 2017

[6] Edge Coupled Stripline Impedance Calculator. https://www.eeweb.com/tools/edge-coupled-stripline-impedance

[7] H.Johnson and M.Graham, High-Speed Signal Propagation: Advanced Black Magic

[8] G.Oliver, Using Flex in High-Speed Applications. Dupont Electronic and Communications

[9] E. Raguzin, Interconnections Update, BNL internal material, 2018

[10] C.Bromberg et.al, The Development of Front End Readout Electronics for ProtoDUNE-SP LArTPC, 2017

[11] H. Chen, Update of Cold ASICs Development. BrookHaven National Laboratory, 2016

[12] M. Worcester, Single Phase ProtoDUNE Cold Electornics QA/QC Plan. DUNE Collaboration Meeting at UT Arlington, 2016

[13] M. Jewell et.al., Characterization of an Ionization Readout Tile for nEXO. arXiv:1710.05109 v2, 2018