High-Speed Data Links in CMOS Technology

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Outline

- **The GigaBit Transceiver (GBT) Project with CERN**
  - **A 5-Gbit/s Radiation-Tolerant Optical Receiver of the GBT Project for SLHC**
  - **A High-Resolution Phase Shifter (50-ps-Resolution and 25-ns Range) of the GBT Project for SLHC**
- **Serializer and Laser Driver Design**
- **PLL Design**
  - **Wideband LC Fractional-N PLL**
  - **Ring PLL**
- **Summary**

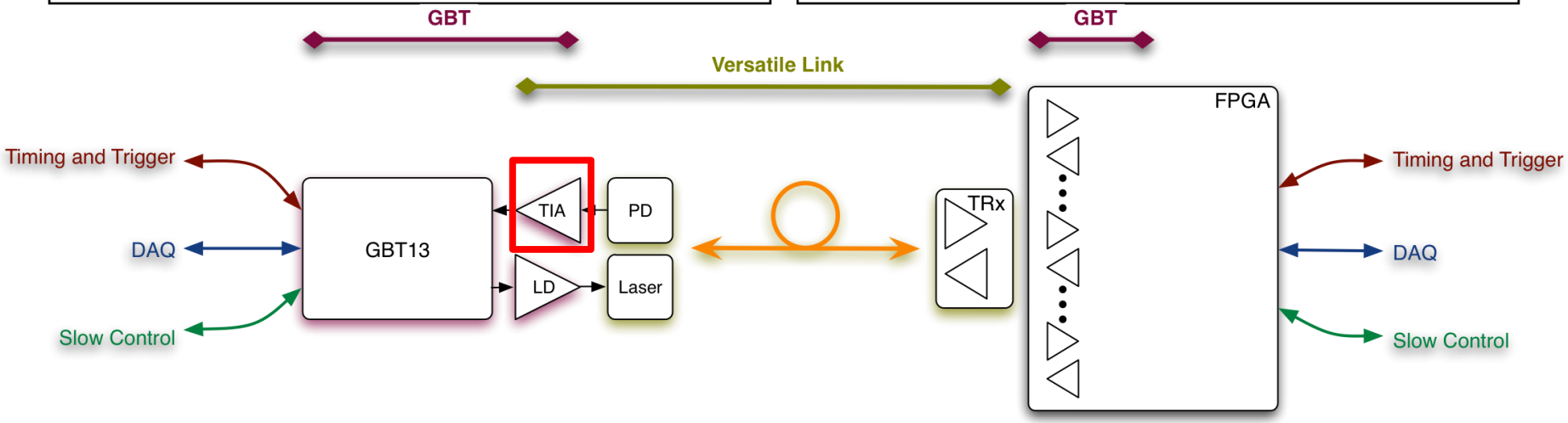
GigaBit Transceiver (GBT) Link Architecture

Defined in the "DG White Paper"

- **"Work Package 3-1"**
  - **Objective:**
    - Development of an high speed bidirectional radiation hard optical link, incorporating DAQ, TTC, and Slow Control into a single link.
  - **Deliverable:**
    - Tested and qualified radiation hard optical link
  - **Duration:**
    - 4 years (2008 – 2011)

Radiation Hard Optical Link:

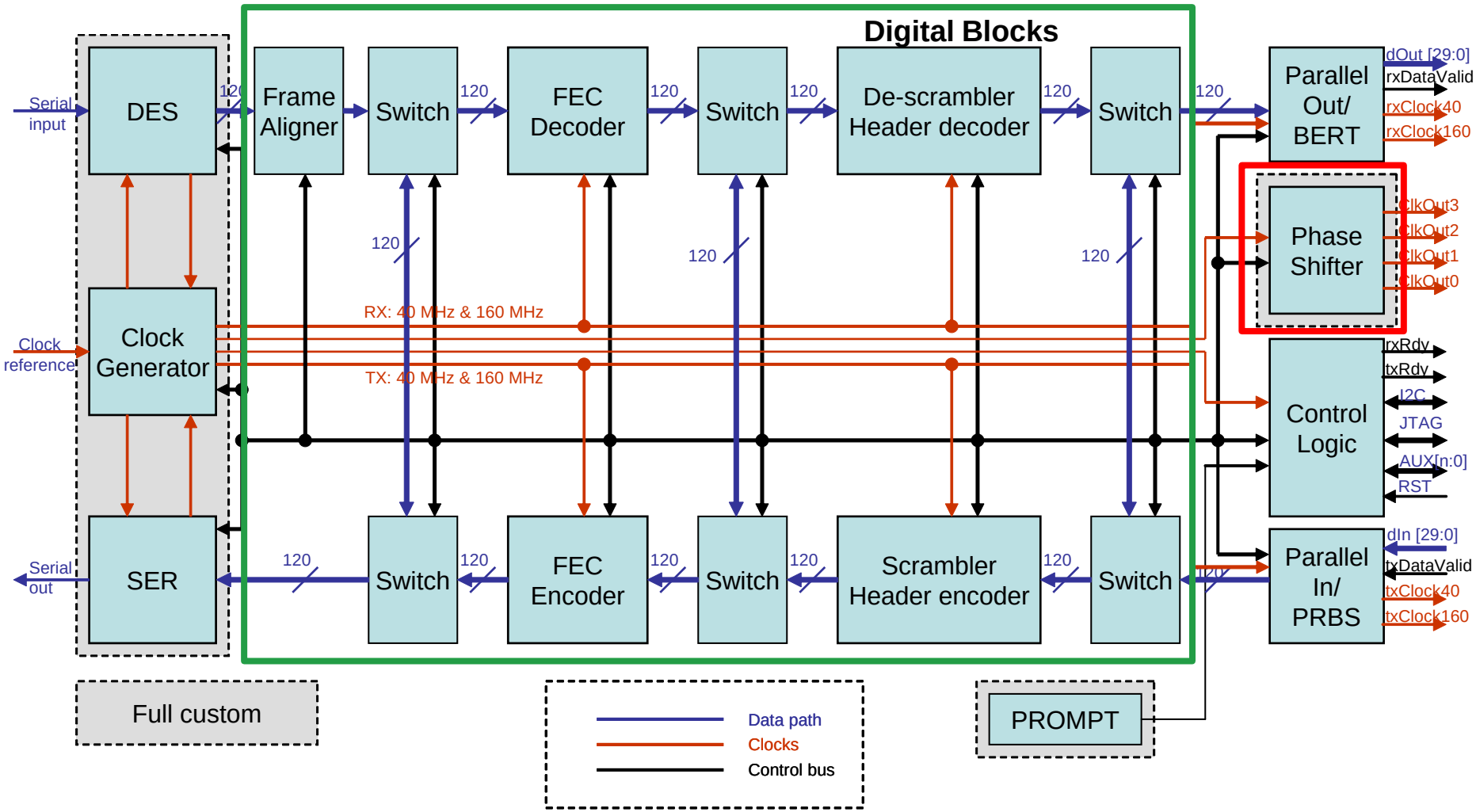
- **GBT project: (led by Paulo Moreira)**
  - **ASIC design**
  - **Verification**
  - **Functionality testing**
  - **Packaging**
- **Versatile link project (led by Jan Troska)**
  - **Opto-electronics**
  - **Radiation hardness**
  - **Functionality testing**
  - **Packaging**



On-Detector
Custom Electronics & Packaging
Radiation Hard

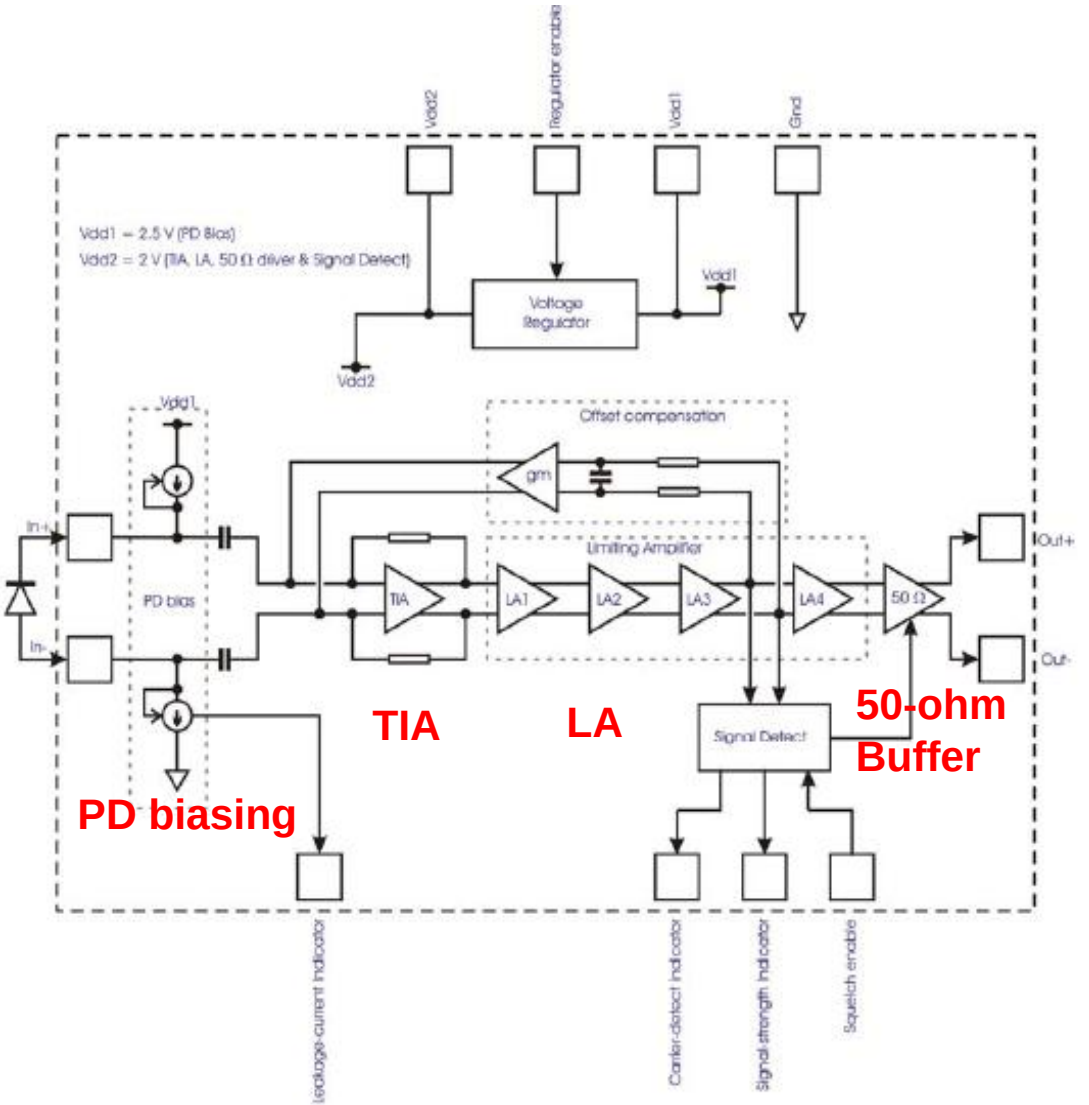
Off-Detector
Commercial Off-The-Shelf (COTS)
Custom Protocol

GBT-SERDES


Digital Blocks
Serial input
DES
Frame Aligner
Switch
FEC Decoder
Switch
De-scrambler Header decoder
Switch
Parallel Out/ BERT
dOut [29:0]
rxDataValid
rxClock40
rxClock160
Phase Shifter
ClkOut3
ClkOut2
ClkOut1
ClkOut0
Clock reference
Clock Generator
RX: 40 MHz & 160 MHz
TX: 40 MHz & 160 MHz
Control Logic
rxRdy
txRdy
I2C
JTAG
AUX[n:0]
RST
Serial out
SER
Switch
FEC Encoder
Switch
Scrambler Header encoder
Switch
Parallel In/ PRBS
dIn [29:0]
txDataValid
txClock40
txClock160
120
Full custom
Data path
Clocks
Control bus
PROMPT

A 5 Gbit/s Radiation-hard Optical Receiver for GBT

- A single chip consisting of
  - A Transimpedance amplifier
  - A Limiting amplifier
  - A 50 Ω line driver
- Main specifications:
  - Bit rate: 5 Gb/s (min)
  - Sensitivity: 20 μA p-p (10^{-12} BER)
  - Total jitter: < 40 ps P-P
  - Dark current: 0 to 1 mA
  - Power supply : 2.5V ± 10%
  - Power consumption < 250 mW
  - Die size: 0.75 mm × 1.25 mm
  - Pin diode capacitance Cd ~ 400 fF
  - Large range of temperature : From -20 C to 80 C
  - Radiation tolerant (up to 200 Mrad)
- Additional features :
  - Internal voltage regulator (with enable/disable control)
  - Leakage-current magnitude indicator
  - Squelch function (with enable/disable control)

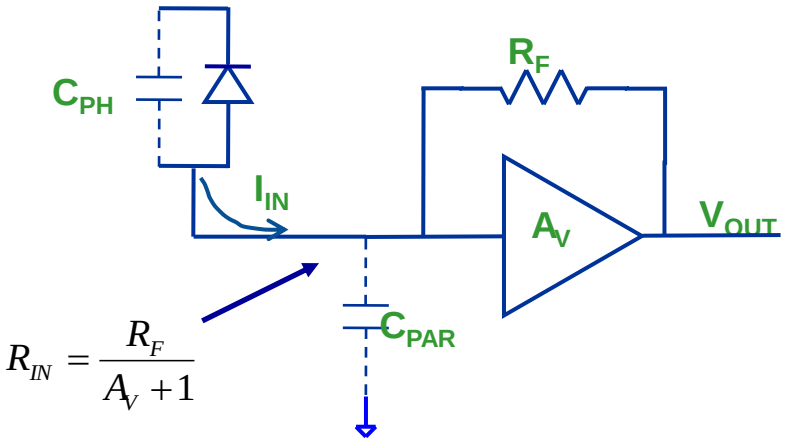


Overview of GBT Optical Receiver Design

- A fully differential architecture
  - Good power supply noise and common-mode noise rejection (PSRR and CMRR)
  - Minimize the effects of cross talk between the TIA and LA stages
  - On-chip AC coupling between the PD and TIA
- Transimpedance amplifier (TIA)
  - Define the sensitivity of the optical receiver-- low noise
  - High bandwidth, and high gain
  - Biasing and leakage current compensation for the PD
- Limiting Amplifier and output buffer (LA)
  - High gain and large output swing
  - Wide bandwidth
  - Offset level compensation

Transimpedance Amplifier

- Shunt (resistive) feedback amplifier is widely used for high speed receiver designs
- To increase the bandwidth:
  - Lowering the Rf
  - Increasing the amplifier open loop gain
  - Lowering the input node capacitance
- The noise contribution of the amplifier mainly comes from the input transistor
- To minimize this noise
  - Increasing the Rf
  - Lowering the input node capacitance
  - Increasing the amplifier transconductance
- Large Rf for low noise and high transimpedance gain
- R and C limit the bandwidth
- Techniques to extend the bandwidth



$$C_T = C_{PH} + C_{PAR} + C_{IN}$$

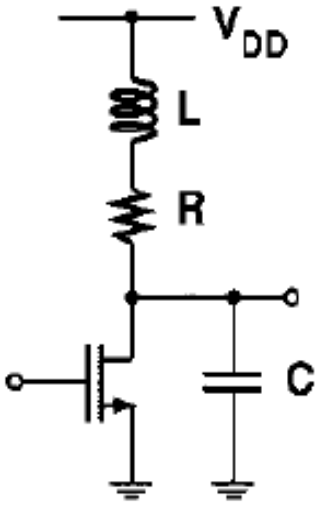
$$Z_T = \frac{v_{out}}{i_{in}} = \frac{-A_V}{A_V + 1} \frac{R_F}{1 + j\omega C_T \frac{R_F}{1 + A_V}}$$

$$BW = \frac{1 + |A_V|}{2\pi . R_F C_T}$$

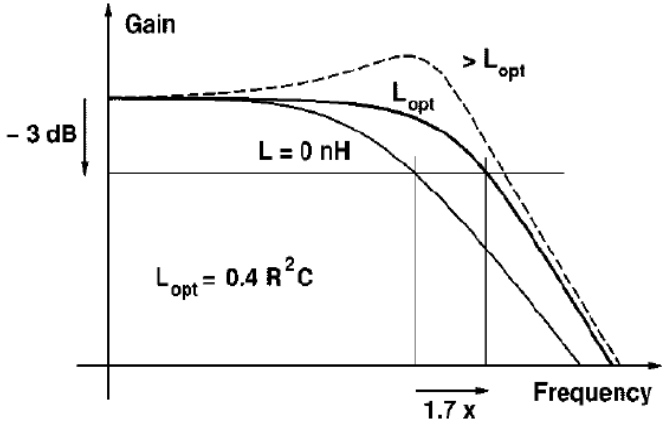
$$i_{n,in}{}^2 = \frac{4kT}{R_F} + \frac{4kT\Gamma}{R_F{}^2} \left(\frac{1}{g_m} + \frac{(2\pi . f . R_F C_T)^2}{g_m} \right)$$

Bandwidth Extension Technique

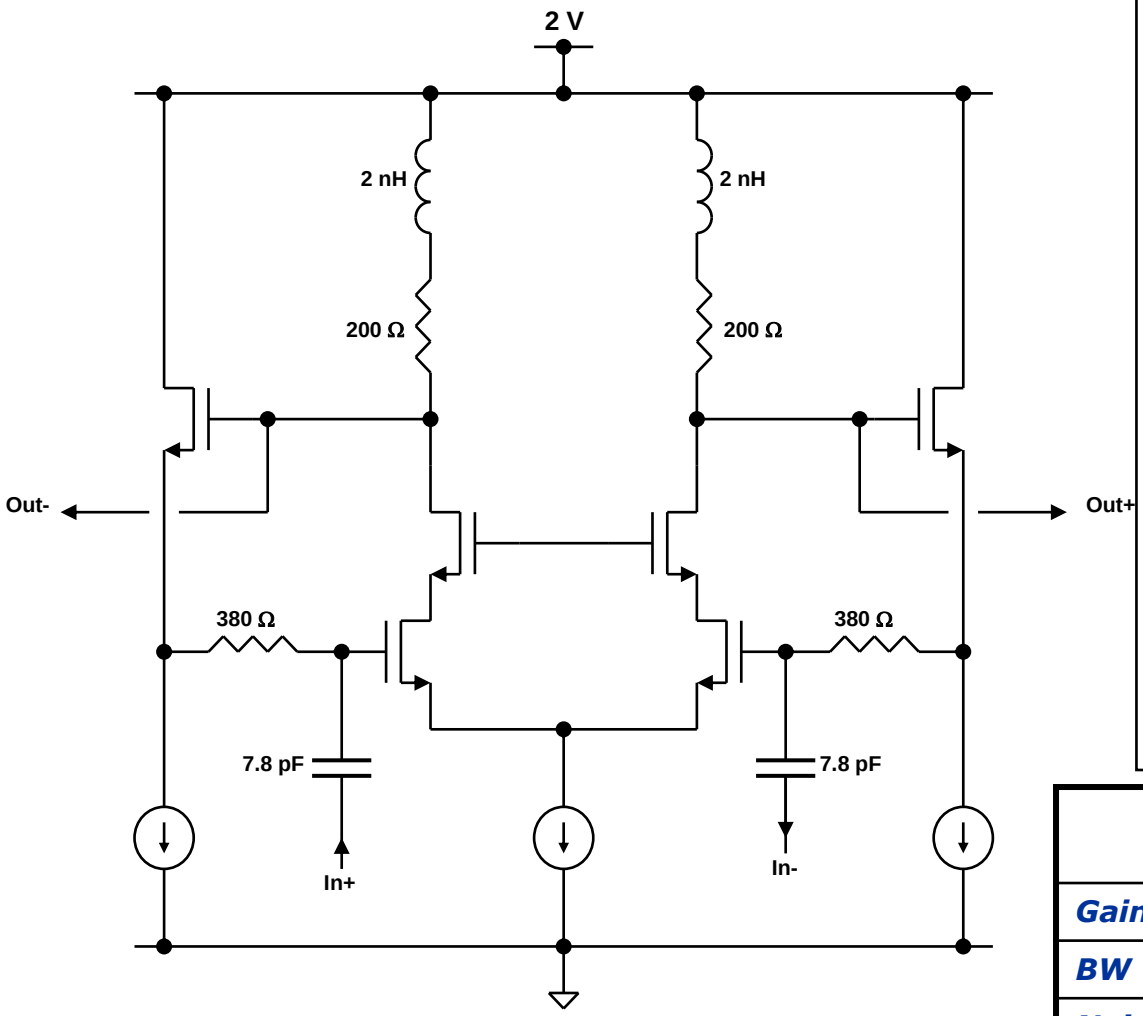
- Inductive(shunt) peaking
  - Introduction of an inductor in series to resonant with the C, enhancing the bandwidth
  - The frequency response of this inductive peaking amplifier is characterized by the ratio m
- $m=L/(R^2C)$



Factor m	Normalized f3dB	Response
0	1.00	No shunt peaking
0.32	1.60	Optimum group delay
0.41	1.72	Maximally flat
0.71	1.85	Maximum bandwidth



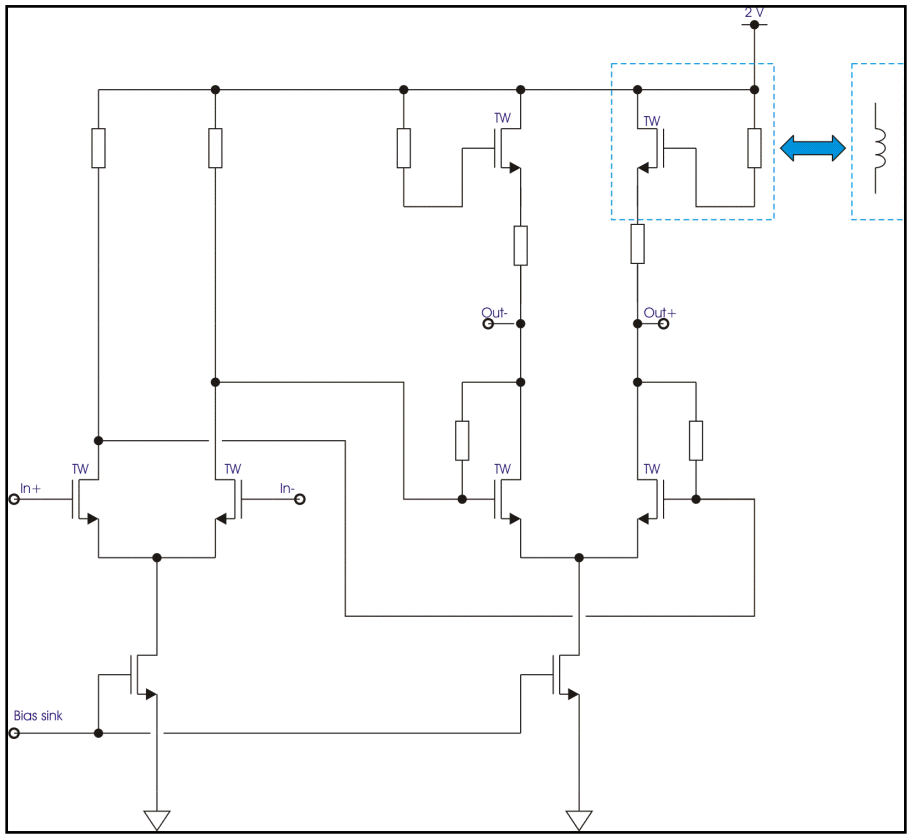
GBT Transimpedance Amplifier

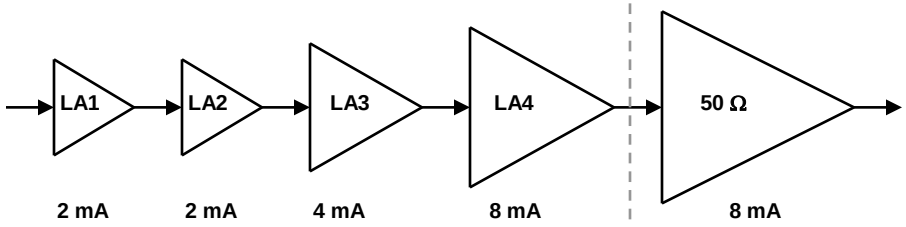


- **Fully differential to minimize**
  - cross talk
  - power supply noise
  - common-mode noise
- **Inductive peaking**
  - Extends the bandwidth
- **Large input transistor for low noise**
- **Cascode**
  - Reduces the Miller effect
- **Drawback:**
  - 2V supply required

	SS, 100˚C	*TT, 27˚C*	*FF, -20˚C*
Gain	*704 Ω*	*700 Ω*	*694 Ω*
BW	*4.0 GHz*	*5.1 GHz*	*6.0 GHz*
Noise	*3.4 μA*	*1.9 μA*	*10 μA*
Power Dissipation	*V_{dd} = 2.5V, I_{dd} = 14 mA, P = 35 mW*		

GBT Limiting Amplifier

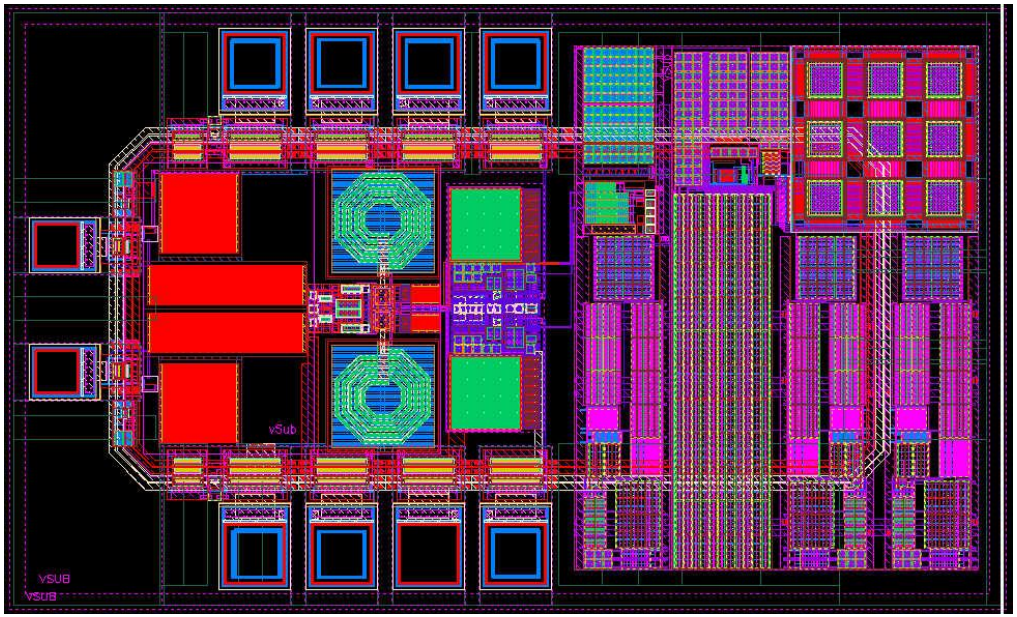




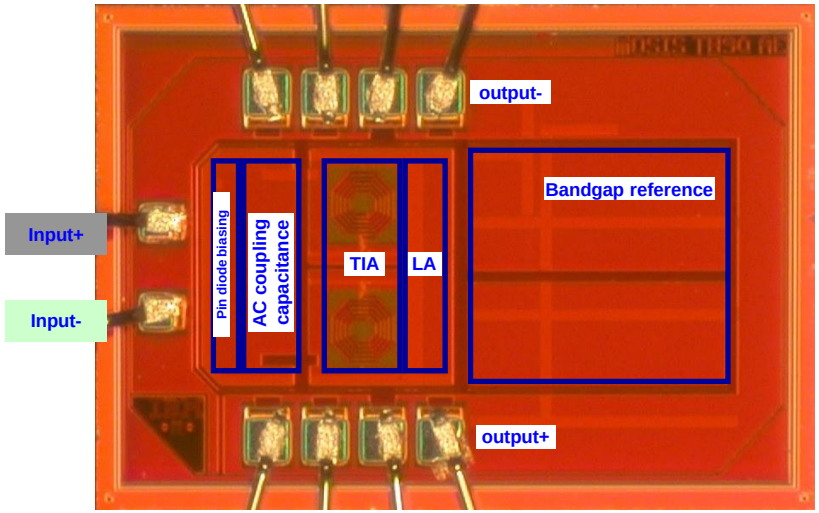
- Modified Cherry and Hopper with resistive loading for high bandwith
- Active inductive peaking
  - BW is increased by 34% by active inductive peaking
- Four gain stages
  - Four gain stages are used to keep the power from being too high.
  - Stages with increasingly larger driving strength to drive the 50-ohm output stage with high bandwidth.
  - "High gain" first stage to reduce the noise contribution from the following stages.

	SS, 100˚C	TT, 27˚C	FF, -20˚C
Gain	24	100	236
BW	4.0 GHz	4.5 GHz	5.0 GHz
Noise	200 μV	309 μV	465 μV
Power Dissipation	V_{dd} = 2.5 V, I_{dd} = 24 mA, P = 60 mW		

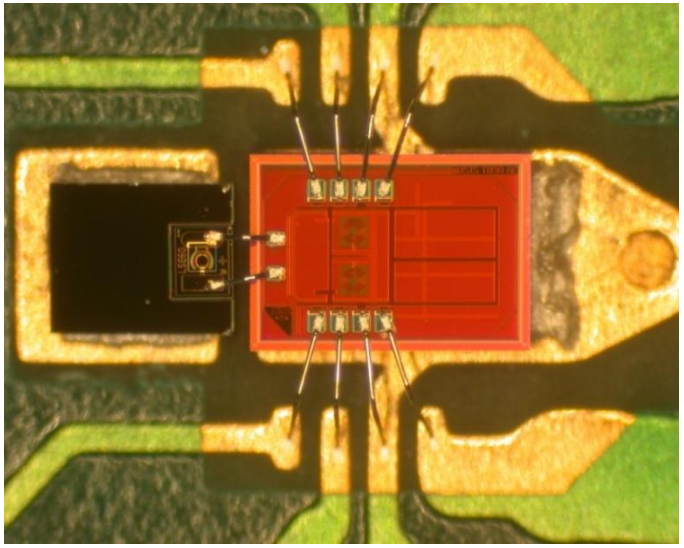
Optical Receiver Chip Layout, Photograph, and Test Setup



- Chip layout, implemented using 0.13 μm IBM CMOS Process
- Die size 0.75 mm x 1.25 mm



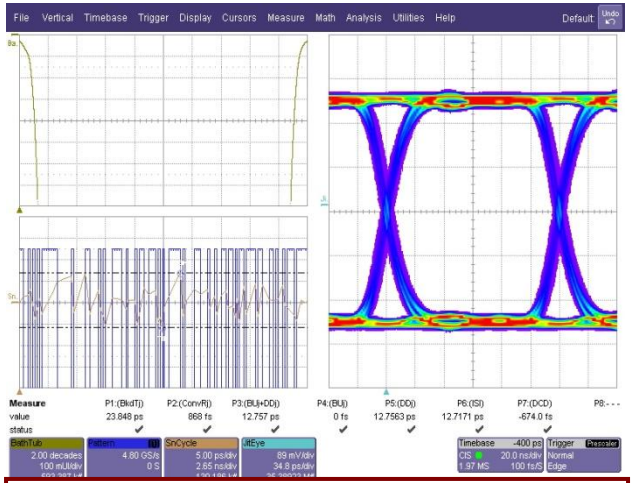
- Chip microphotograph



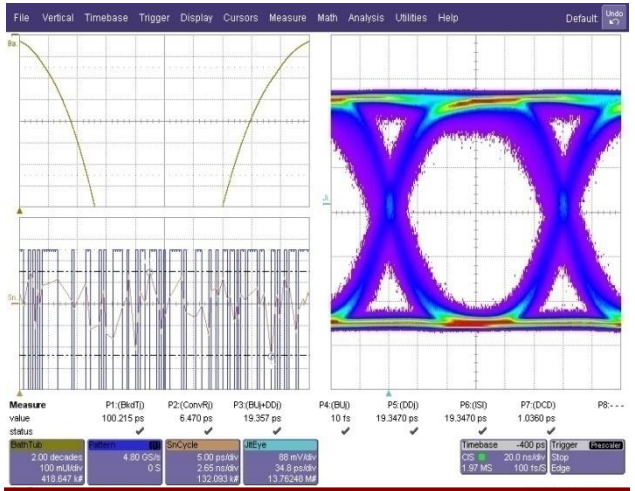
- Chip along with the PD on testboard

Eye Diagram Measurements

- Measured differential eye diagrams at 5 Gbit/s for different optical power at the input (-6 dBm and -18 dBm)
  - Well opened eye diagram for -6 dBm and still correct at -18 dBm
  - The test PRBS sequence length is 2^7-1
  - A constant output swing of 400 mV
- For -6 dBm input :
  - Rise time = 30 ps
  - Total jitter = 0.15 UI @ BER = 10^{-12} (UI = 200 ps)
- For -18 dBm input :
  - Rise time = 60 ps
  - Total jitter = 0.55 UI @ BER = 10^{-12}

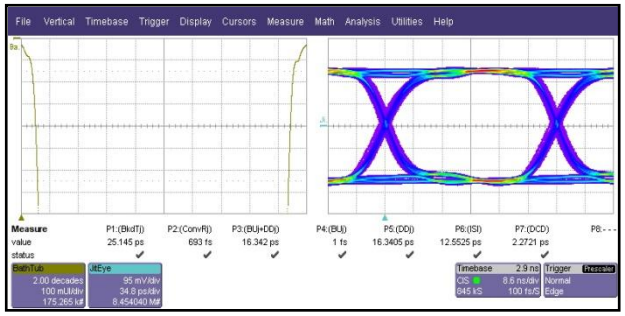


Eye diagram 5 Gbit/s optical power = -6 dBm

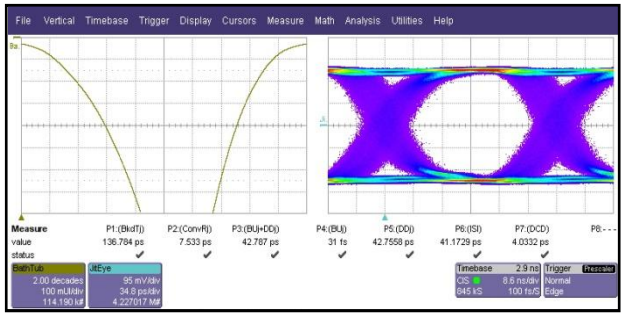


Eye diagram 5 Gbit/s optical power = -18 dBm

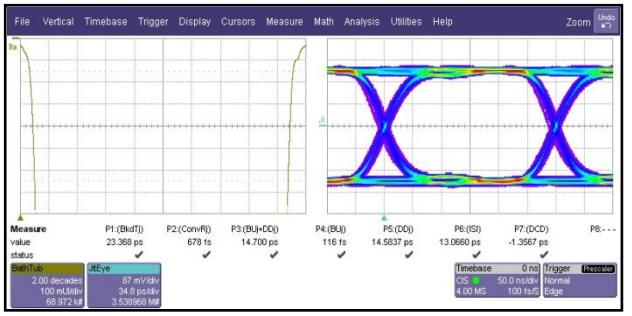
Eye diagrams versus the Total Dose



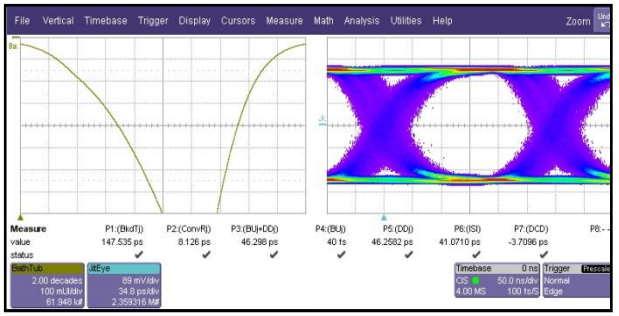
Pre-rad eye diagram (input=500 mV)



Pre-rad eye diagram (input=50 mV)



200 Mrad eye diagram (input=500 mV)

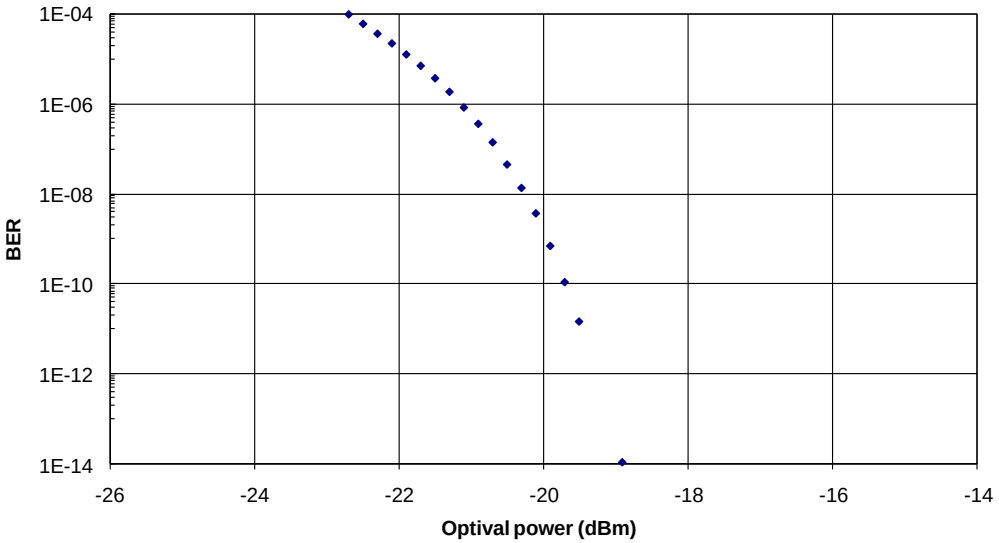


200 Mrad eye diagram (input=50 mV)

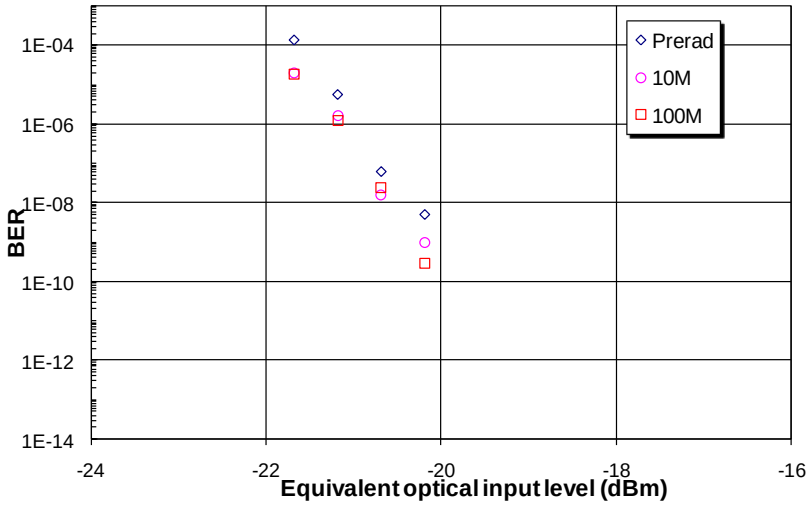
- Electrical board used for irradiation test
- Irradiation test done at CERN Xray facility 4 Mrad/hour
- Only the GBTIA chip is exposed to Xray beam
- No degradation is observed after a dose rate of 200 Mrad

Bit Error Rate Measurements

BER v.s. Input Optical Level



BER v.s. Total Dose



- For Vdd=2V and T=25 °C
- Data pattern : PRBS7
- The sensitivity for a BER of 10^{-12} is estimated to be better than -19 dBm

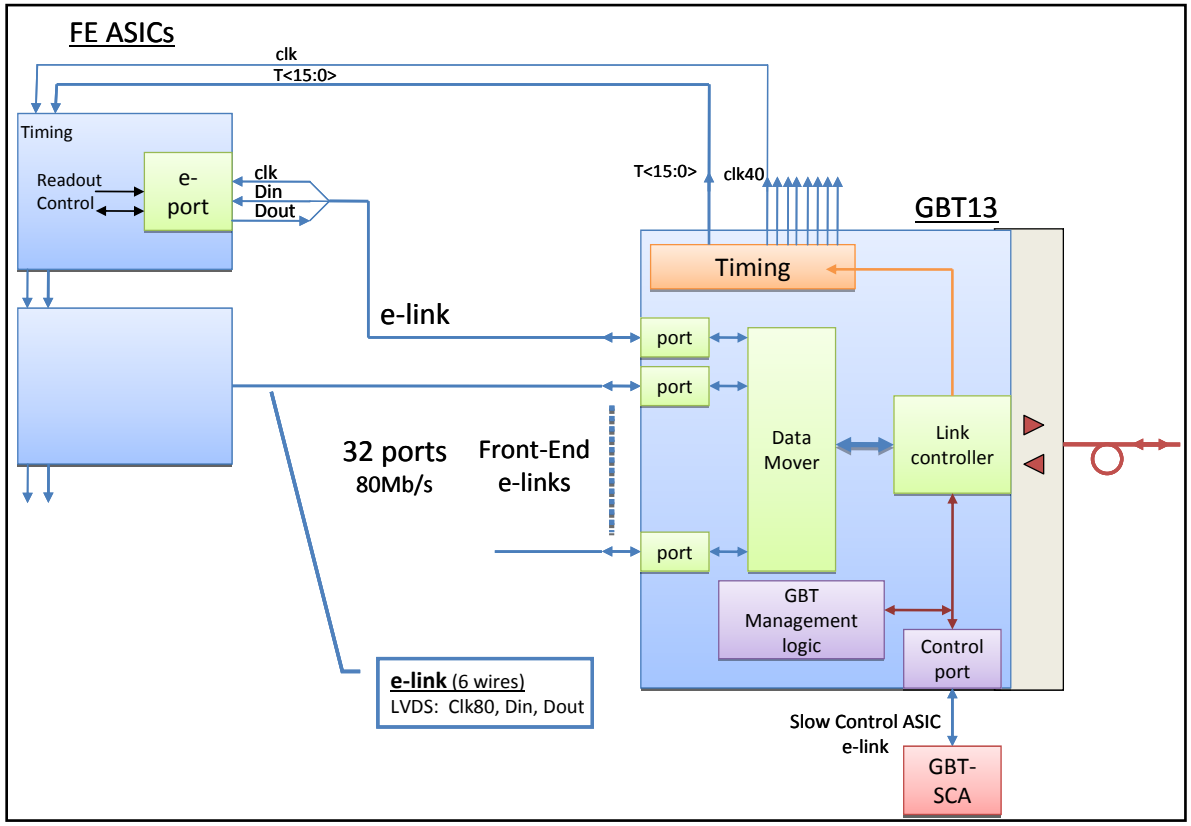
- Effects of total dose (as high as 100MRad) is negligible.

Performance Summary of the GBT Optical Receiver

- **Main Specifications in term of bandwidth and sensitivity are respected**
  - Eye diagram is well opened at 5 Gbit/s
  - BER v.s. the input current shows a good sensitivity
- **The effect of the leakage current is estimated**
  - The sensitivity is degraded by 4 dB
  - The value of the high pass cut off frequency still compatibility with the data encoding used for the GBT
- **Radiation effects :**
  - TID tolerance is proven
  - We have to estimate the single event upset tolerance

Bit rate	5 Gbit/s
Transimpedance gain	40 kΩ
Output voltage	± 0.2 V (50 Ω)
Sensitivity for BER =10-12	-19 dBm
Supply voltage	2 V ± 10%
Power consumption	95 mW
Radiation tolerance	> 200 Mrad
Penalty for high dark current	4 dB

Phase Shifter in the GBT

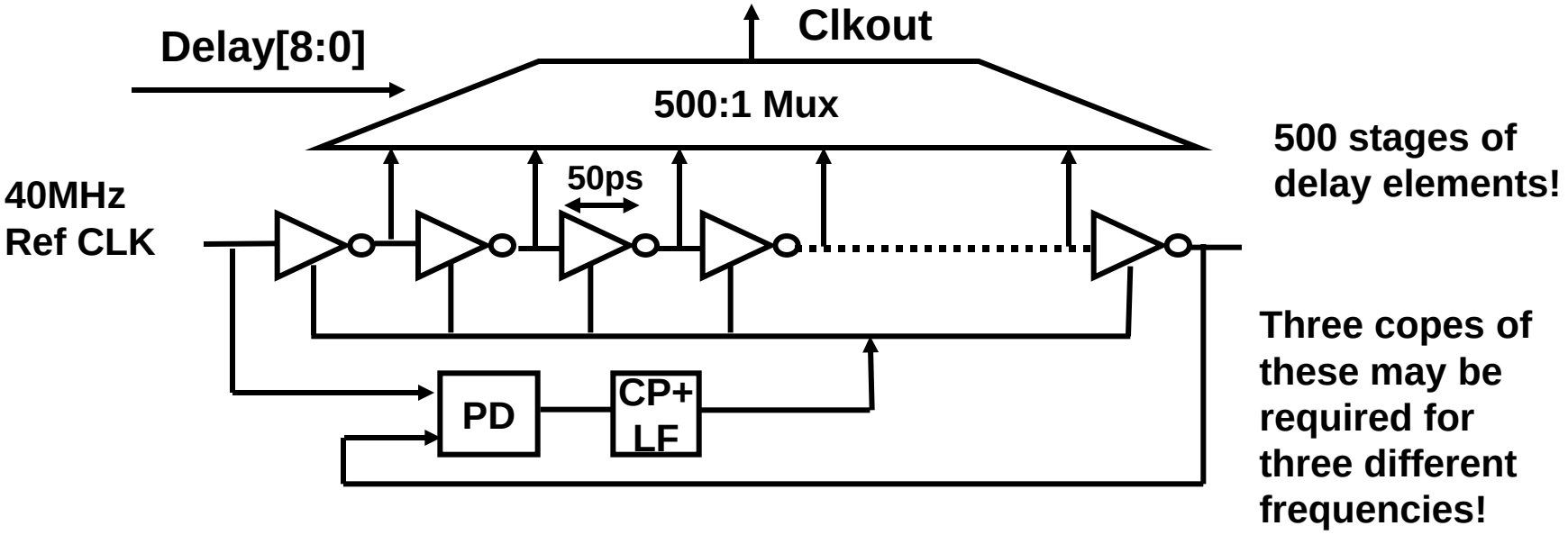


- To provide multiple (~8) clocks synchronized with the main clock for front-end ASICs with frequency of 40 MHz, 80 MHz, and 160 MHz.
- To allow for compensation of the cable/fiber lengths, the time-of-flight of particles and delays in the electronic circuits.
- The 8 reference clocks are programmable both in ***phase*** and ***frequency***.
- The required phase resolution is ***50 ps*** independently of the clock frequency.

Phase Shifter Specs

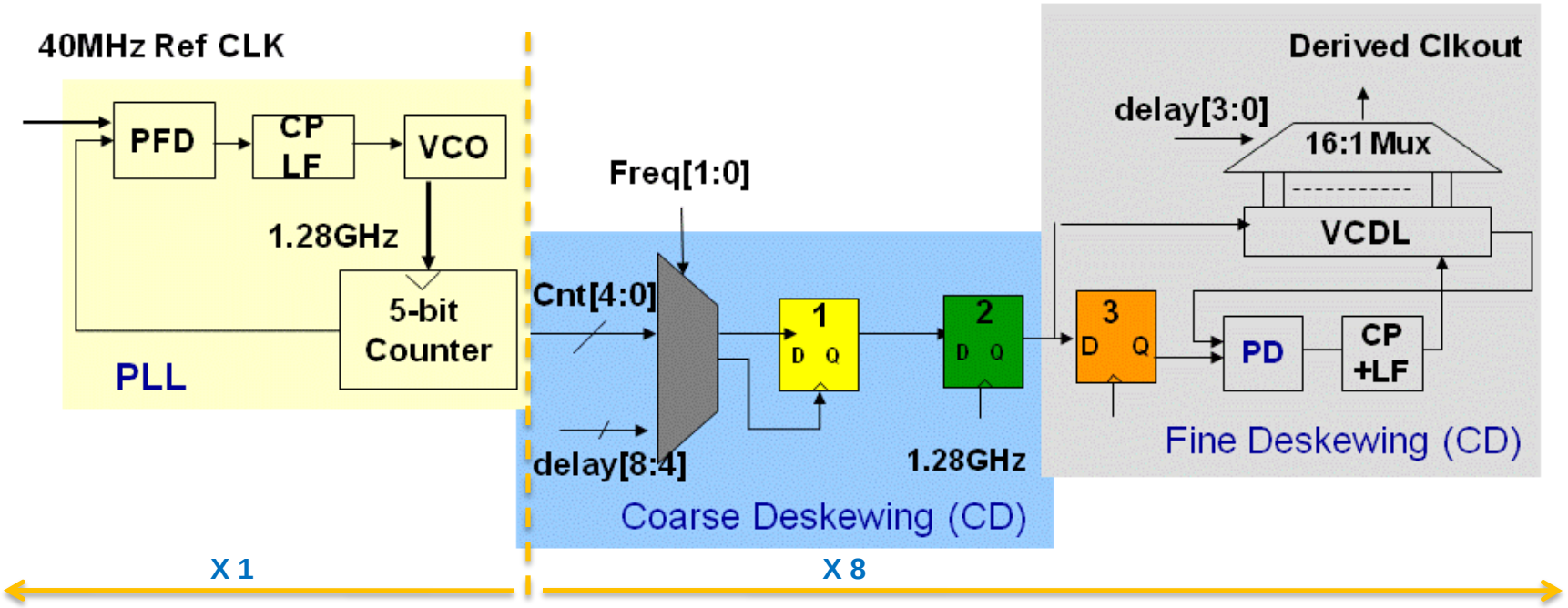
#	specification	min	typ	max	unit	note
	Number of outputs	**8**				
	Frequencies	**40, 80 and 160**			**MHz**	**programmable per output, set by control word Freq[1:0]**
	Phase resolution	**50**			**ps**	**Set by Delay[8:0]**
	DNL			**20%**	**LSB (50ps)**	
	INL			**30%**	**LSB (50ps)**	
	Jitter RMS			**5**	**ps**	
	Jitter P-P			**30**	**ps**	
	Temperature coefficient			5	ps/deg	
	Supply coefficient			50	ps/V	
	Logic levels					Programmable: CMOS/LVDS
	Synchronized with the 40Mhz main clock					

Phase Shifter Architecture #1



- 500 stages of delays are needed for a resolution of 50 ps in a range of 25 ns.
- Considerable amount of switching power and switching noise.

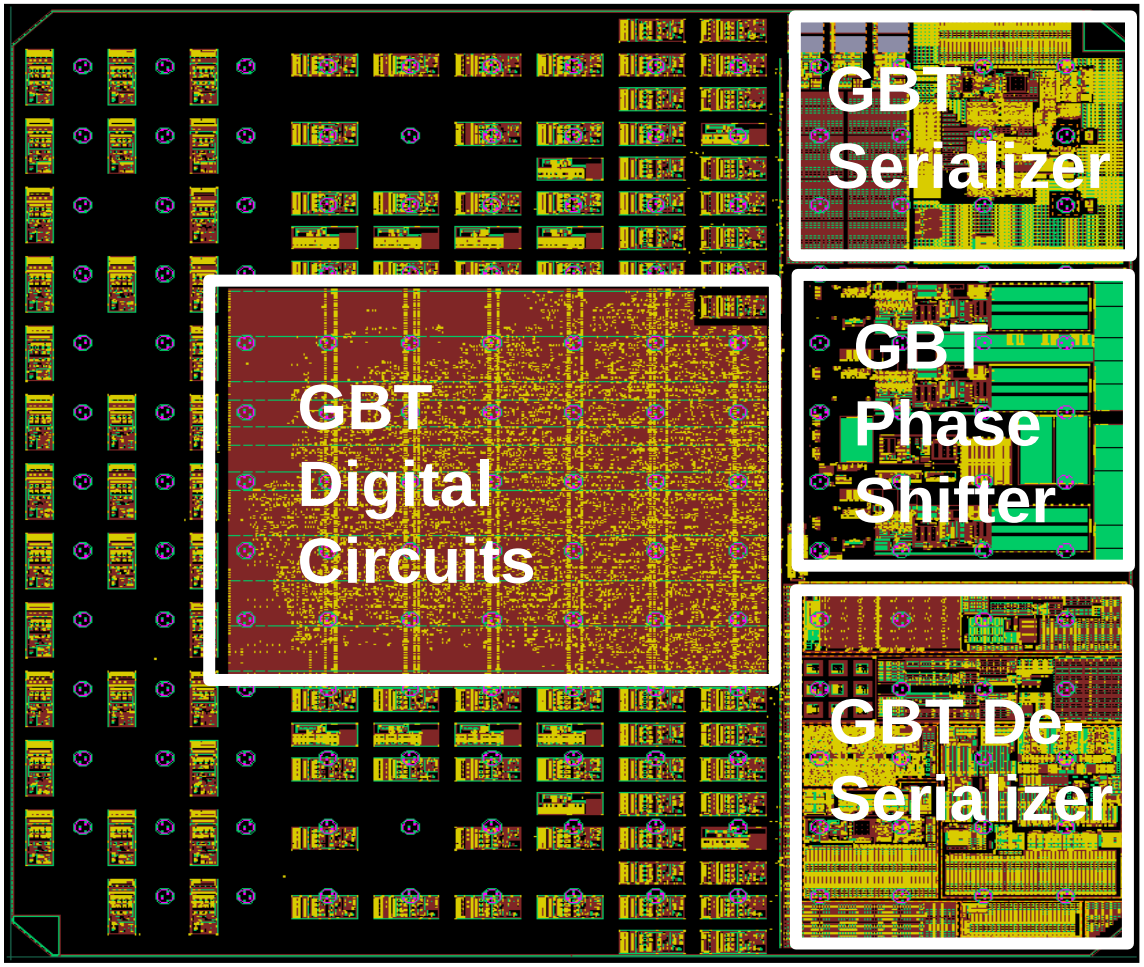
Phase Shifter: Architecture #2



Main features:

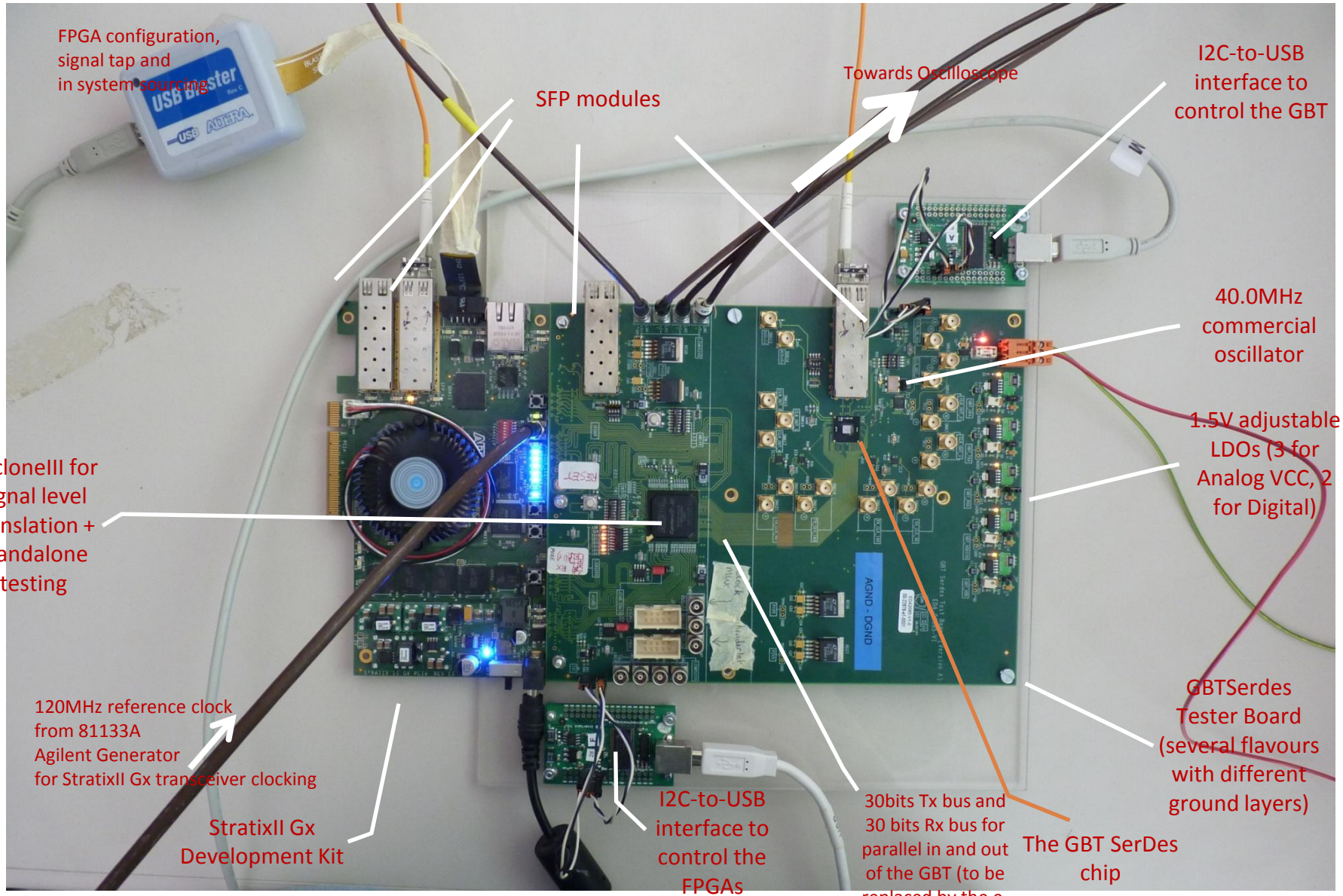
- 3 channels in the GBT – SerDes
- 1 PLL + Counter generates the three frequencies: 40 / 80 and 160 MHz
- 1 DLL per channel: 48.83 ps resolution
- Mixed digital/analogue phase shifting technique:
  - Coarse deskewing – Digital: Δt(coarse) = 781.25 ps
  - Fine deskewing – Analogue: Δt(fine) = 48.83 ps
- Power consumption: 5.6 mW/channel (simulated)
- Simulated Differential non-linearity: <6.7% LSB
- Simulated Integral non-linearity: INL<6.5% LSB

GBT-SerDes Chip Layout



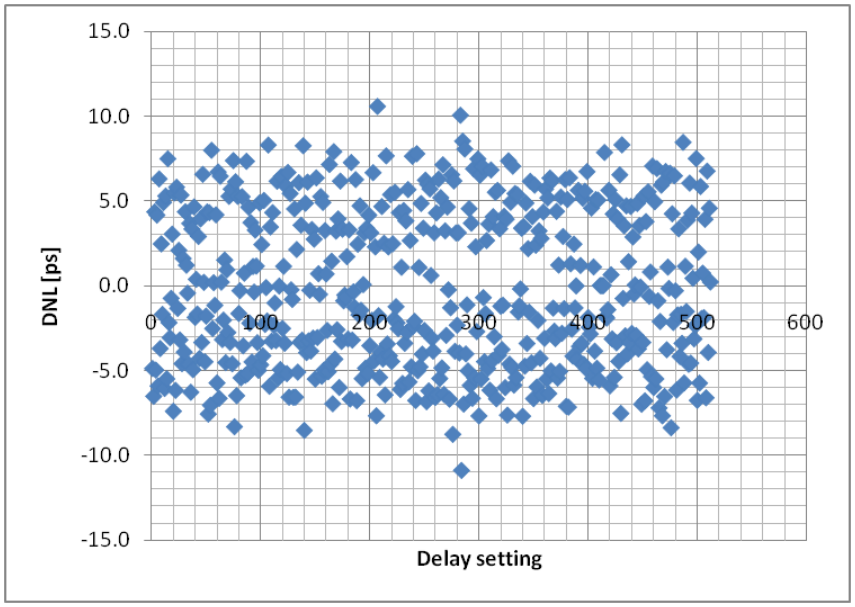
Packaged in a custom 13 × 13 bump-pad C4 package (168 pin)

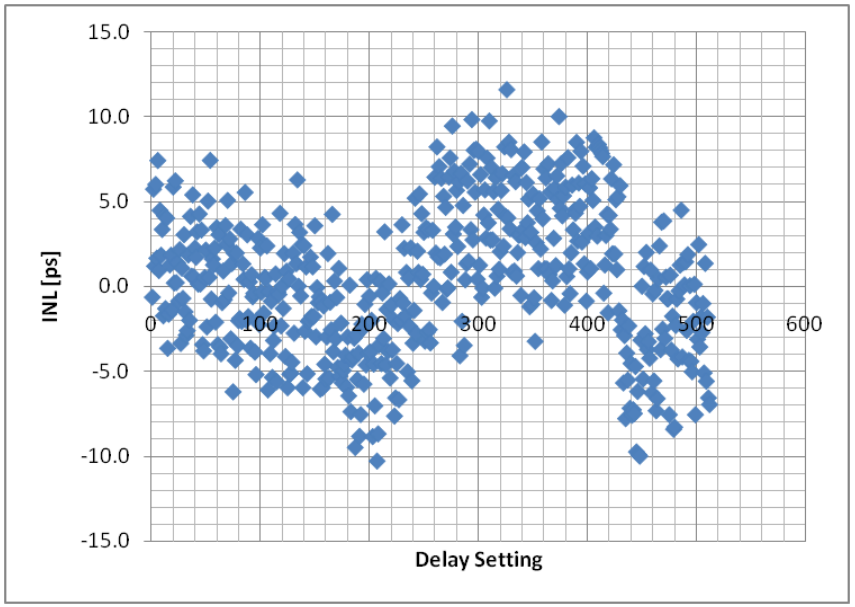
Test Setup


FPGA configuration, signal tap and in system sourcing
SFP modules
Towards Oscilloscope
I2C-to-USB interface to control the GBT
40.0MHz commercial oscillator
1.5V adjustable LDOs (3 for Analog VCC, 2 for Digital)
CycloneIII for signal level translation + standalone testing
120MHz reference clock from 81133A Agilent Generator for StratixII Gx transceiver clocking
StratixII Gx Development Kit
I2C-to-USB interface to control the FPGAs
30bits Tx bus and 30 bits Rx bus for parallel in and out of the GBT (to be replaced by the e-ports)
The GBT SerDes chip
GBTSerdes Tester Board (several flavours with different ground layers)

Phase Shifter: Measurements

- Resolution: Δt = 50 ps
- Differential Non-Linearity
- σ = 4.7 ps (9.6% of Δt)
- pp = 21.5 ps (44% of Δt)
- Jitter: σ = 5 ps (pp = 30 ps)
- Integral Non-Linearity
- σ = 4.3 ps (8.7% of Δt)
- pp = 21.9 ps (48.7% of Δt)



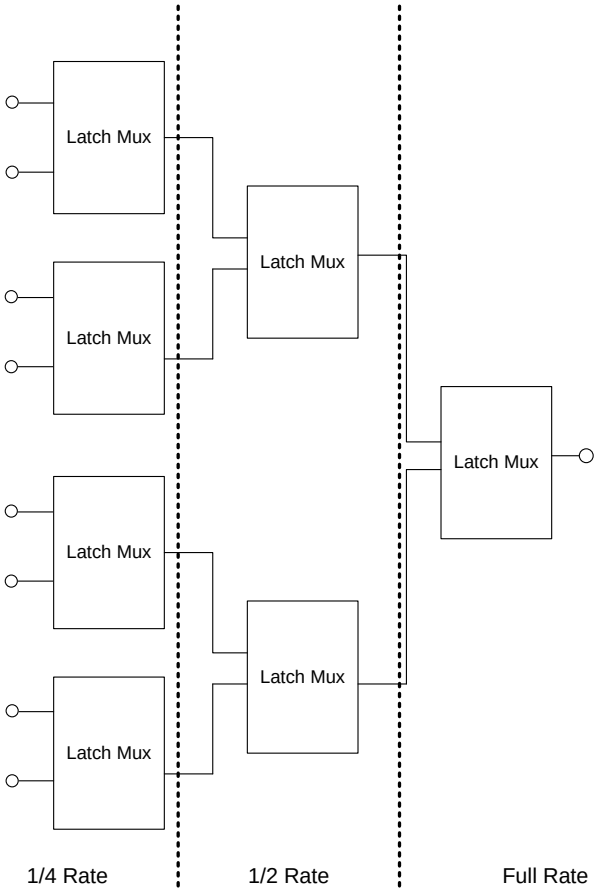


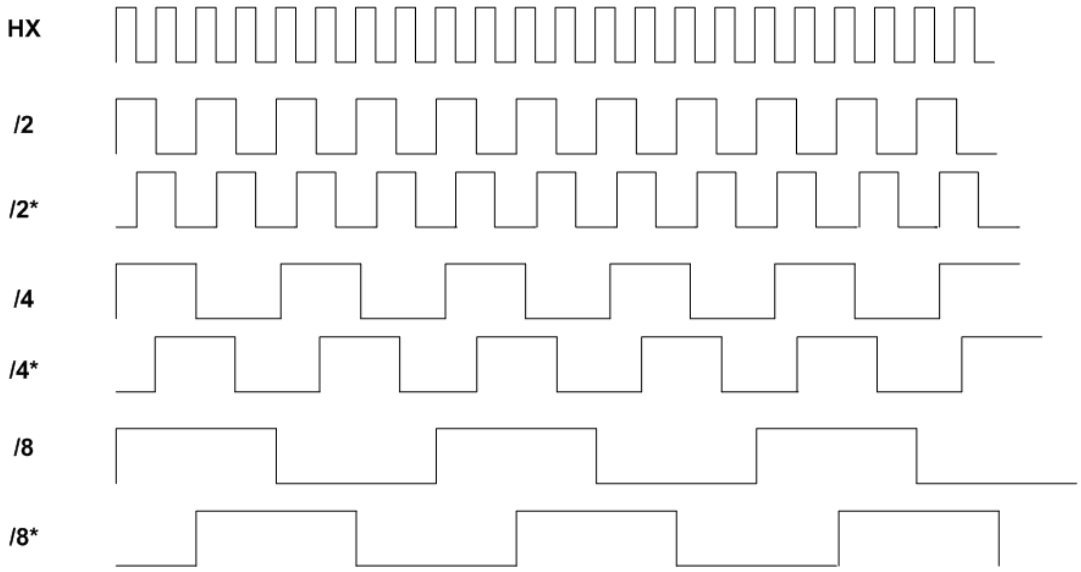
Transmitter Driver

- Must interface to the receiver
  - Signal swing
  - Common mode
  - AC couple (baseline wander)
- Best signal integrity for the least amount of power
  - Double termination to reduce reflections?
  - Drive strength? Pre emphasis?
- Current Mode Logic (CML) v.s. Single-ended Dynamic-Logic such as Truely-Single-Phase-Clock (TSPC)

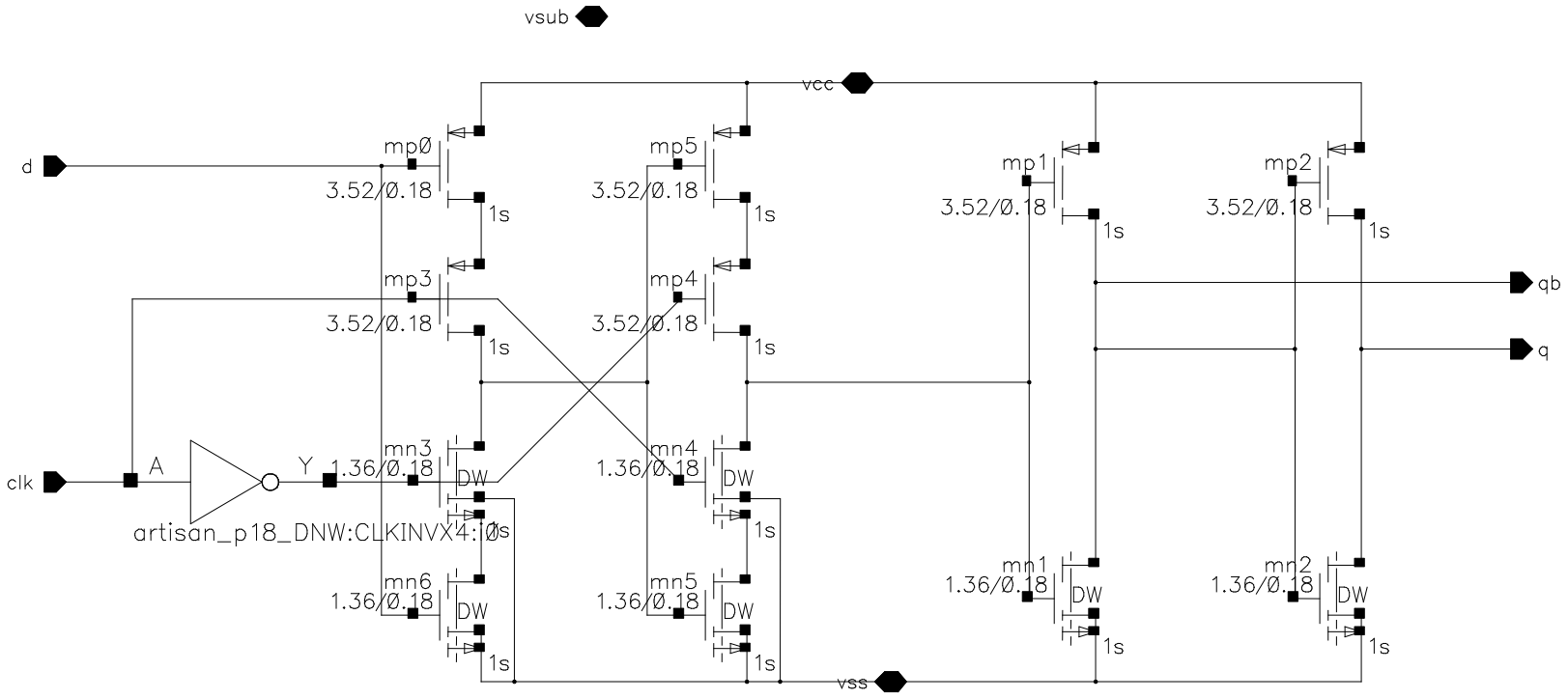
Dynamic-Logic Serializer and Driver

- Dynamic CMOS gates (TSPC), no CML logic.
- “Christmas Tree” architecture (recursive).
- Poly phase clocking maximizes timing margin (speed).

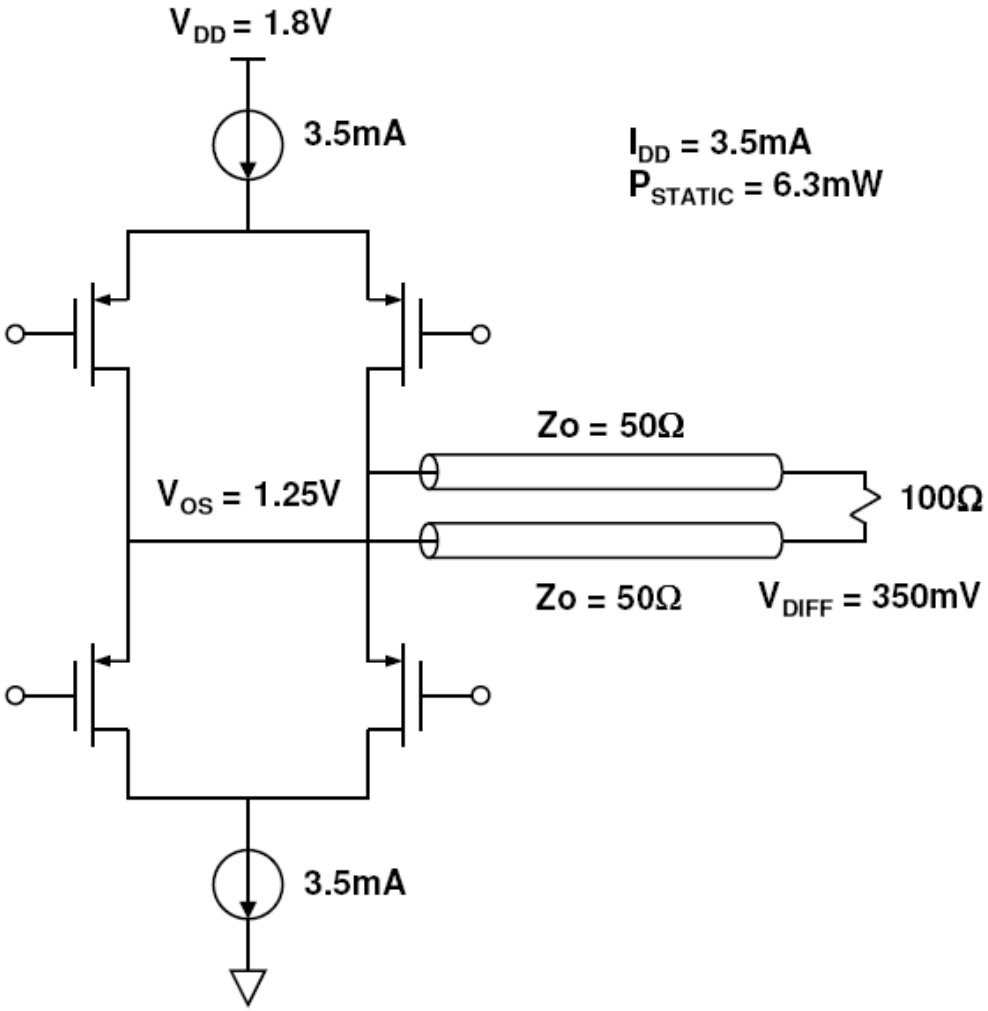




Dynamic CMOS – TSPC (Truly Single Phase Clock)

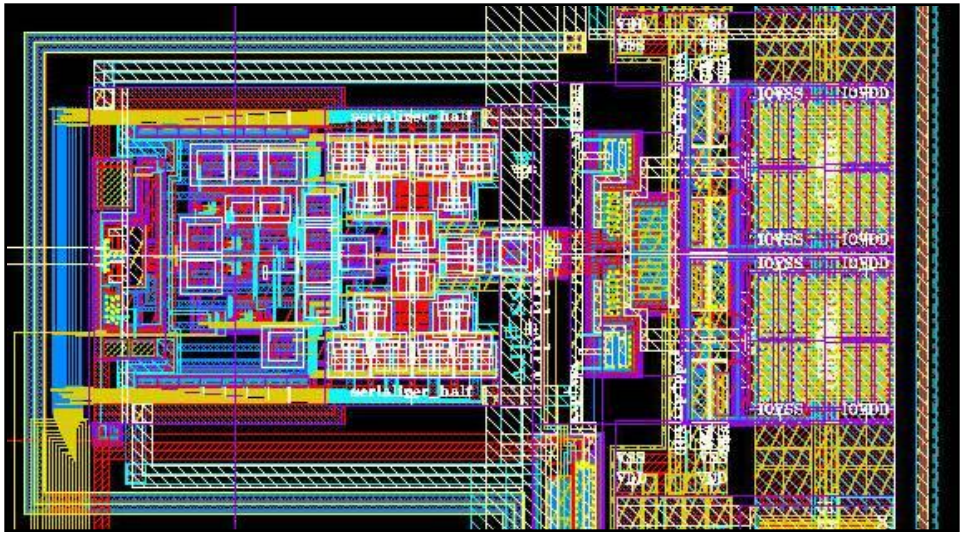


Push-Pull CML Driver for TSPC Serializer



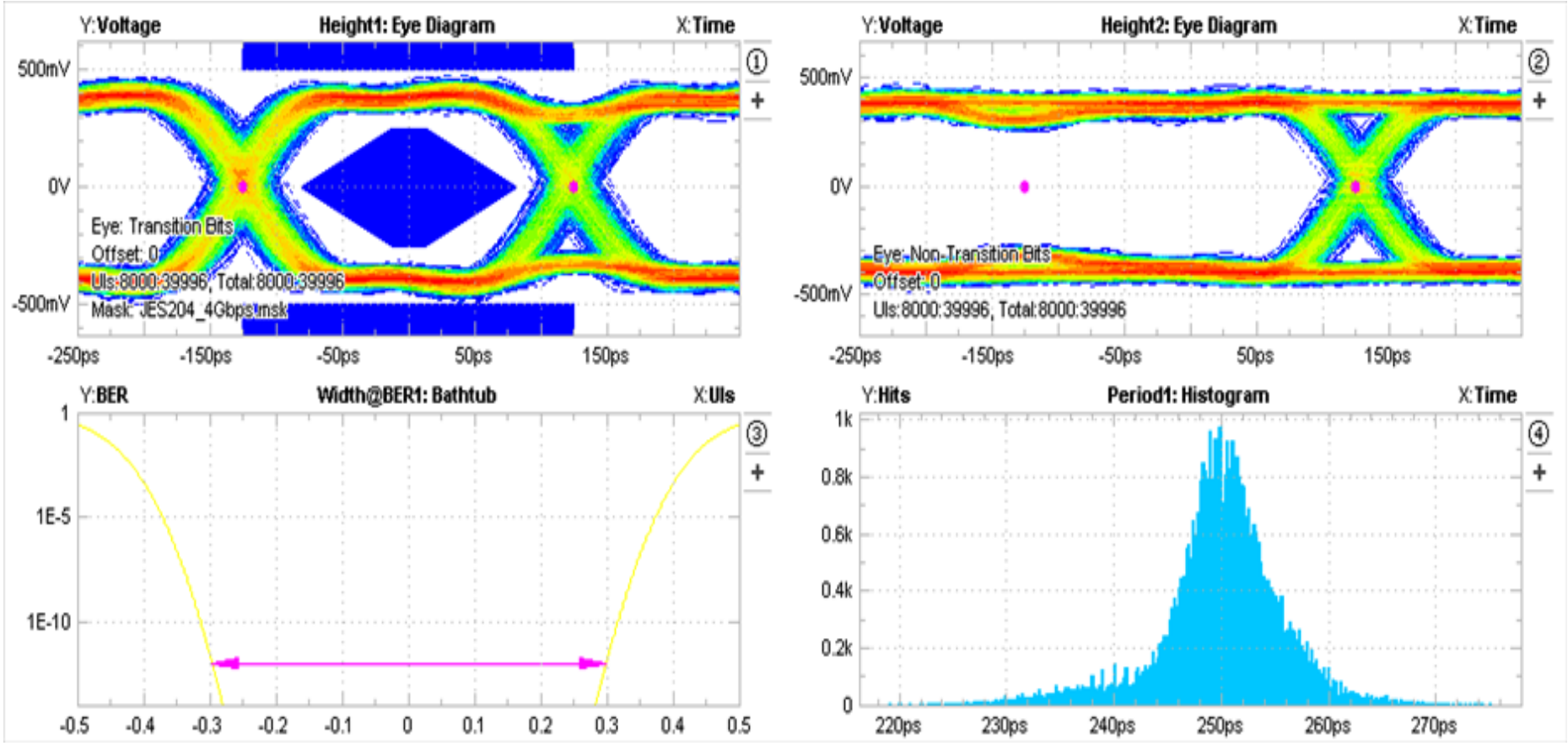
- Push-Pull Operation, Lower power consumption compared to CML
- Differential swing is +/-I_{DD}R, where R=50Ω
- Bandwidth is 1/(RC)

Dynamic-Logic Serializer and Driver Layout

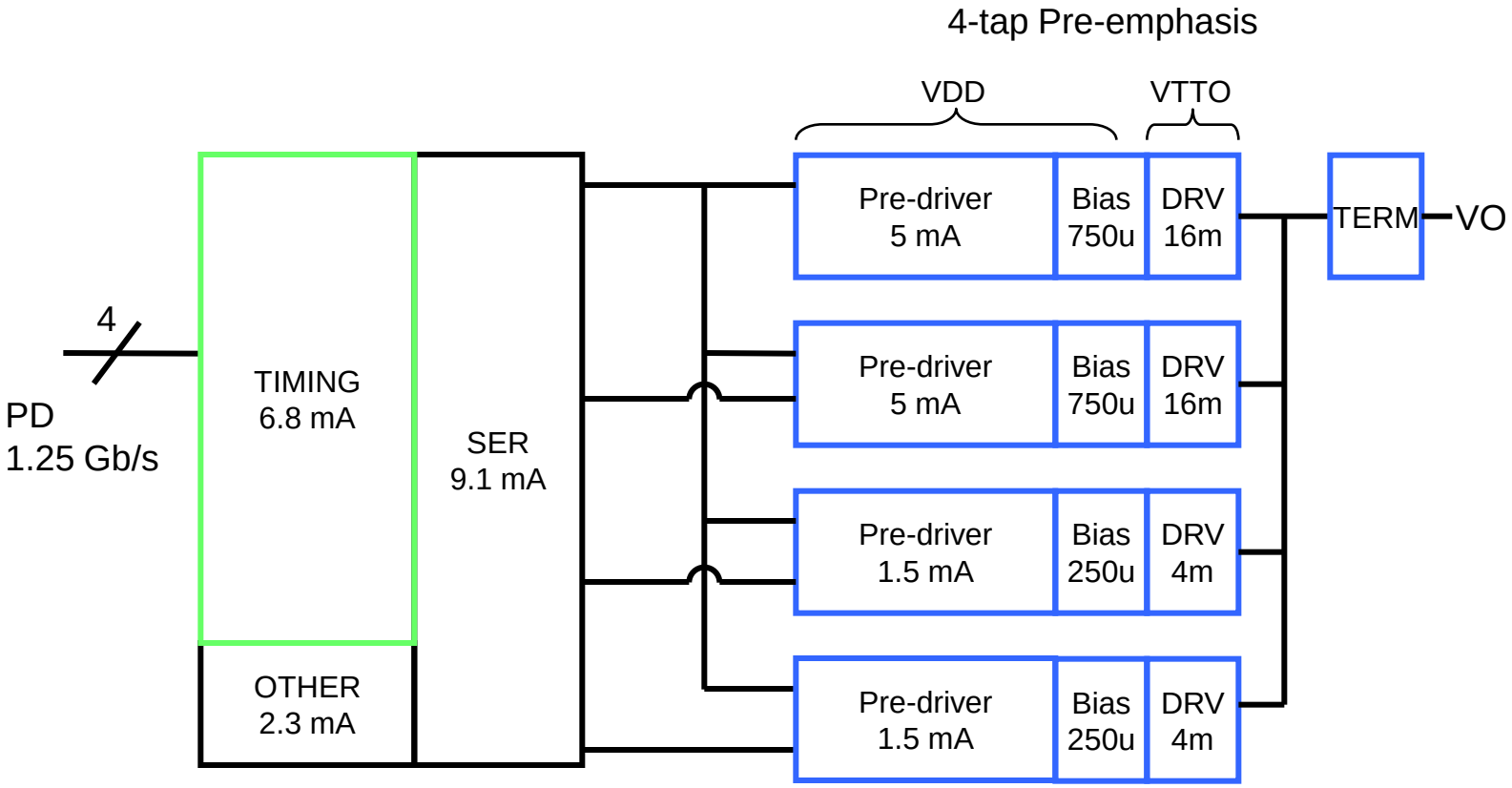


Serializer, Driver, and Pre-Driver	
Power @ 250MSPS (2G high speed clock)	34 mW
Area	400 µm x 160 µm

Eye Diagram of 4Gbps 0.5inch FR4

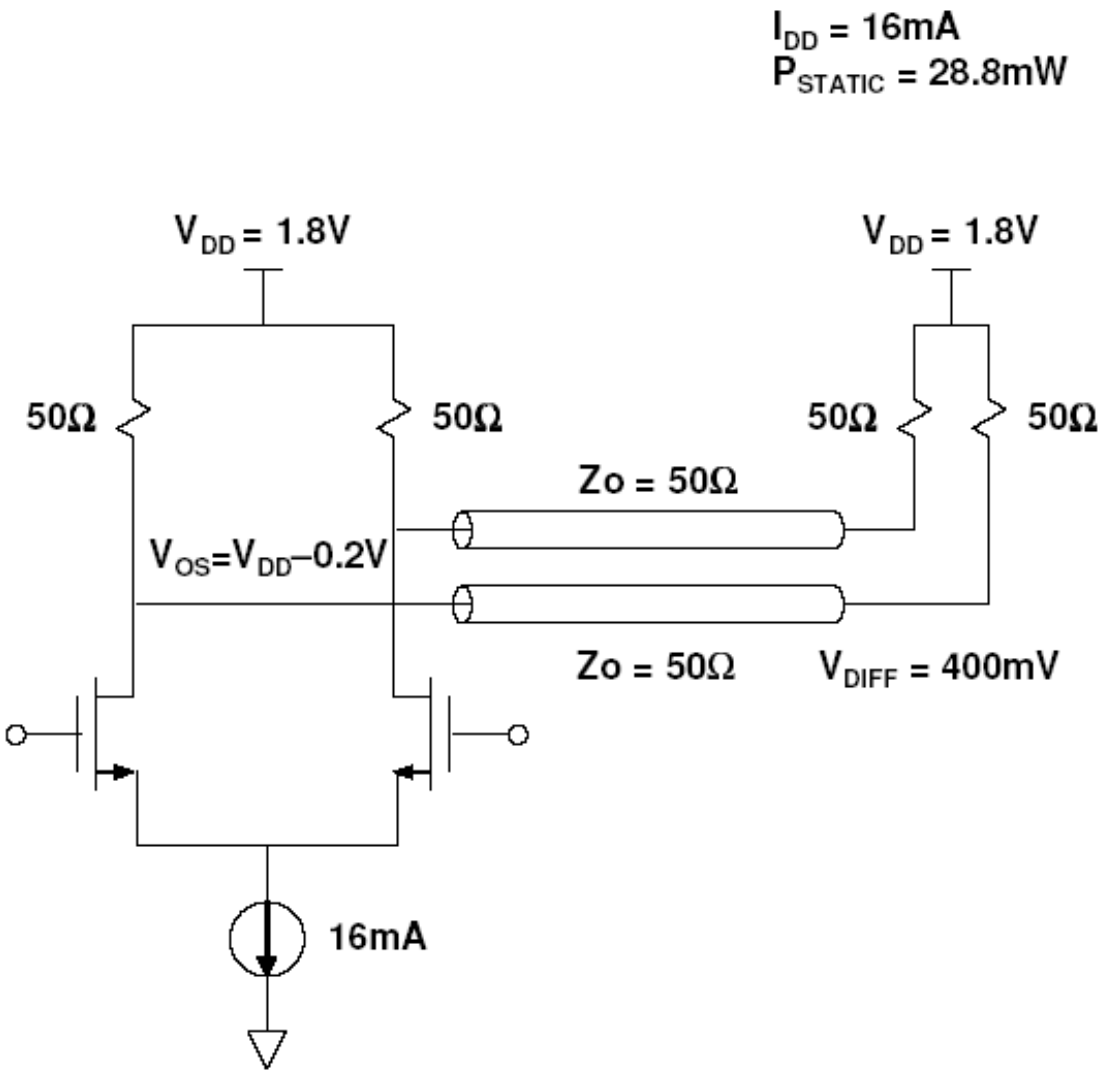


CML Serializer and Driver



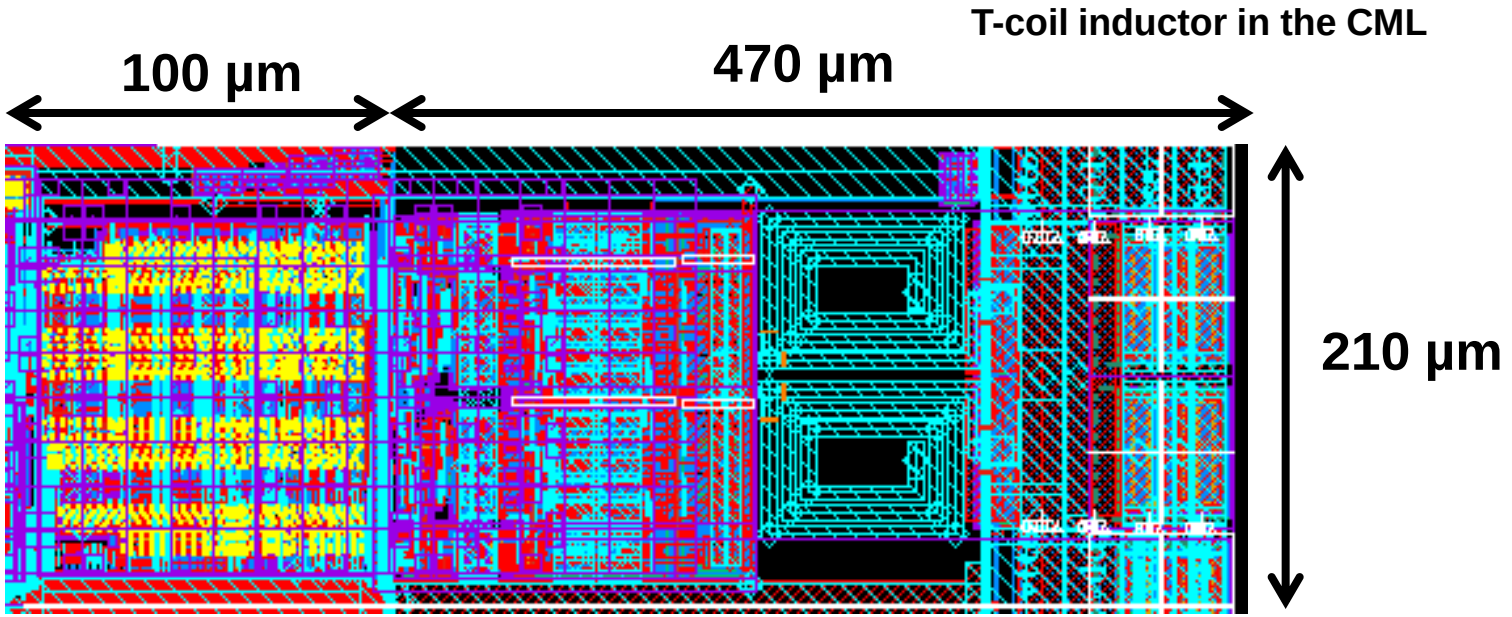
Synchronous TX (excluding serializer, etc.)	Power	Power (No PE)
Timing: bit alignment, sign swaps, etc.	12.2 mW	4.1 mW
Driver power (VDD)	27.0 mW	10.3 mW
Output power (max DC, max PE) (VTTO) (40mA max)	72.0 mW	25.6 mW
Total	109.2mW	40 mW

CML Driver



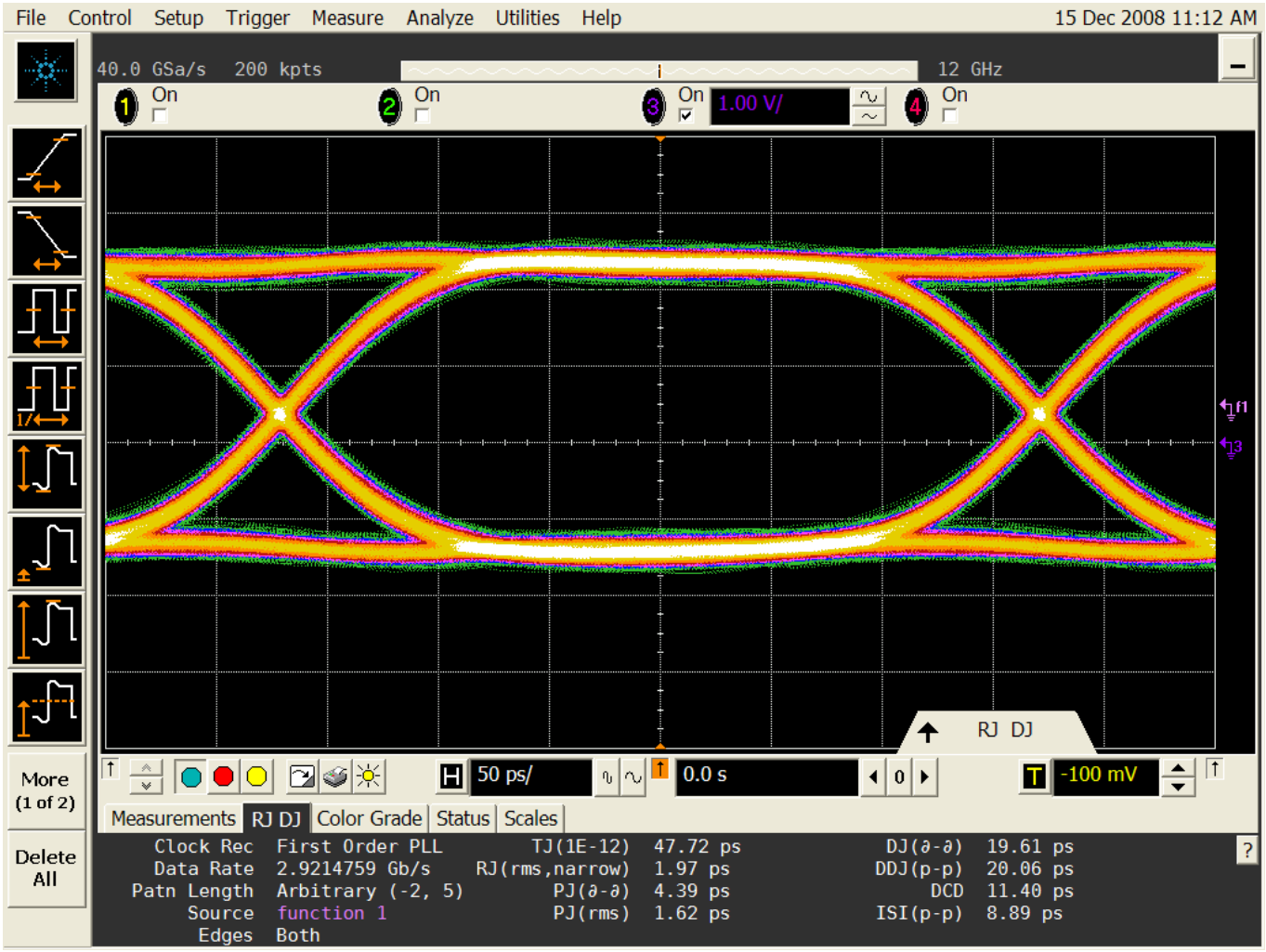
- Resistive Internal termination absorbs reflections.
- High Power. Class A operation. Power dissipated in internal termination wasted.
- Differential swing is +/-0.5I_{DD}R
- Bandwidth is 1/(2RC)

CML Serializer and Driver Layout



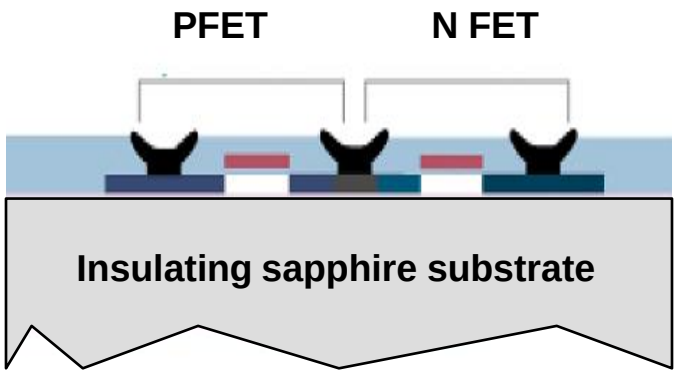
Synchronous TX (excluding serializer, etc.)	Area (⊥ x ‖)
Timing Cell	100 µm x 140 µm
Driver (including inductors and pads)	470 µm x 210 µm

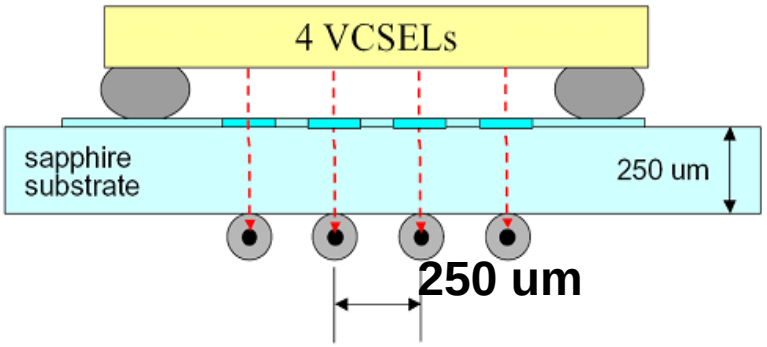
CML Transmitter (3Gbps 2.5inch FR4)



TJ = 48ps pp = 0.15UI pp

Silicon-on-Sapphire CMOS Technology

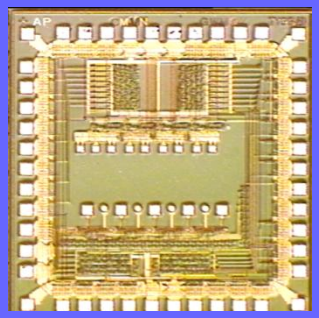




end view

- Insulating sapphire substrate
- A very thin silicon layer (100 nm)
- Reduced parasitic capacitance
  - Low power consumption
  - Minimum crosstalk
  - High integration of RF, mixed-signal, passive elements and digital functions on a single device.
- Optically transparent substrate
- Good immunity to SEEs
- Substrate is a good thermal conductor
- Sustaining low temperature

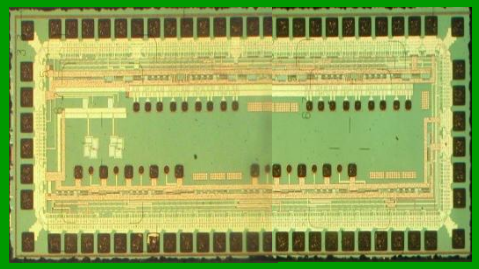
Low Power CMOS OE Transceiver ICs in Silicon-on-Sapphire Technology



Performance:
4-channel optoelectronic transceiver
0.6Gb/s

Innovation:
Dynamic adjust power at the transmitting side

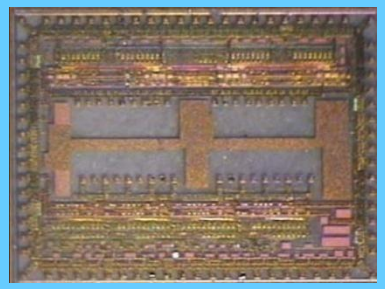
DARPA OE-center



Performance:
4-channel optoelectronic transceiver
2-3Gb/s

Innovation:
Instant power-up/down

DARPA PCA/RATS



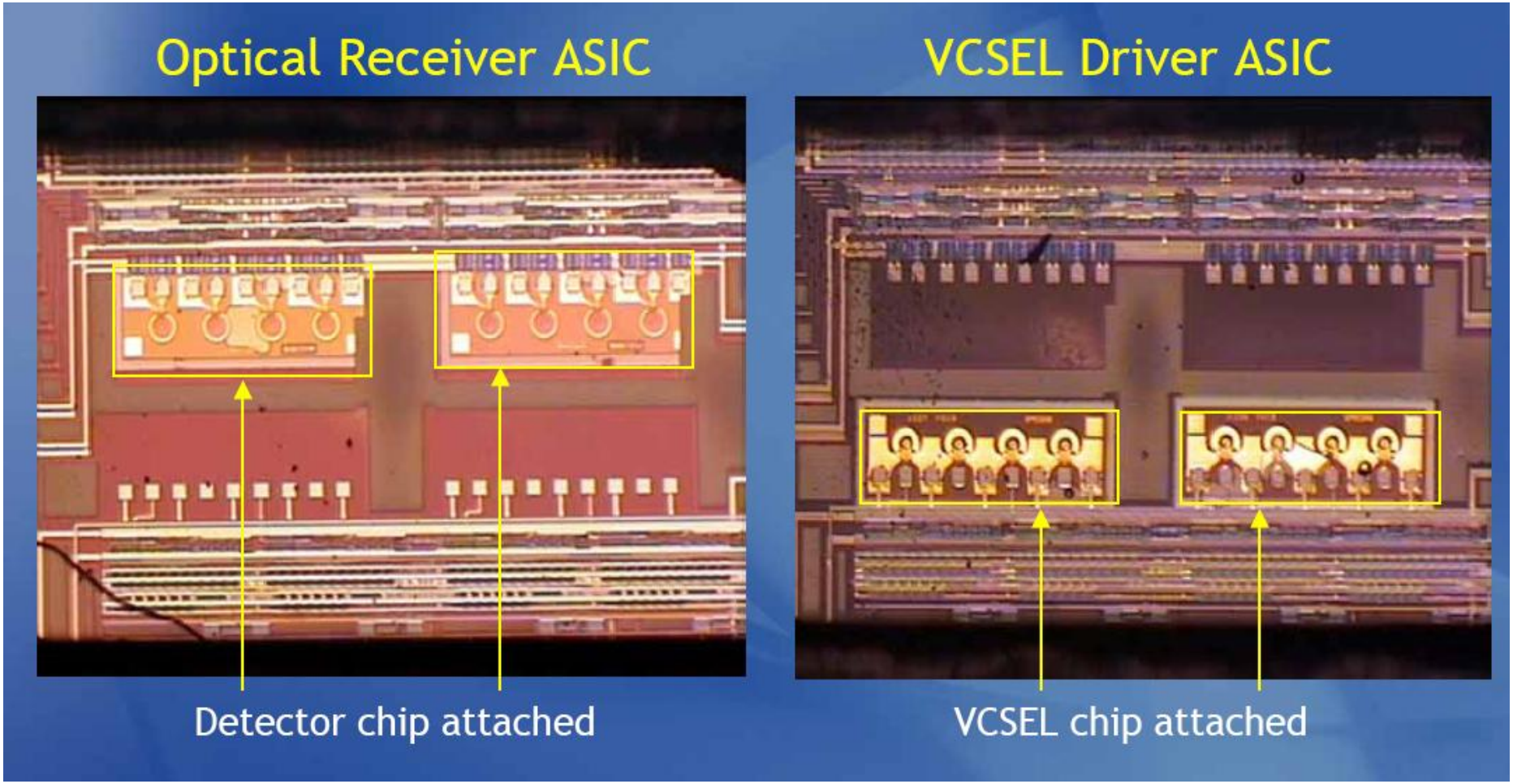
Performance:
4-channel optoelectronic transceiver
3-4Gb/s

Innovation:
Dual-rate (power-performance trade off)

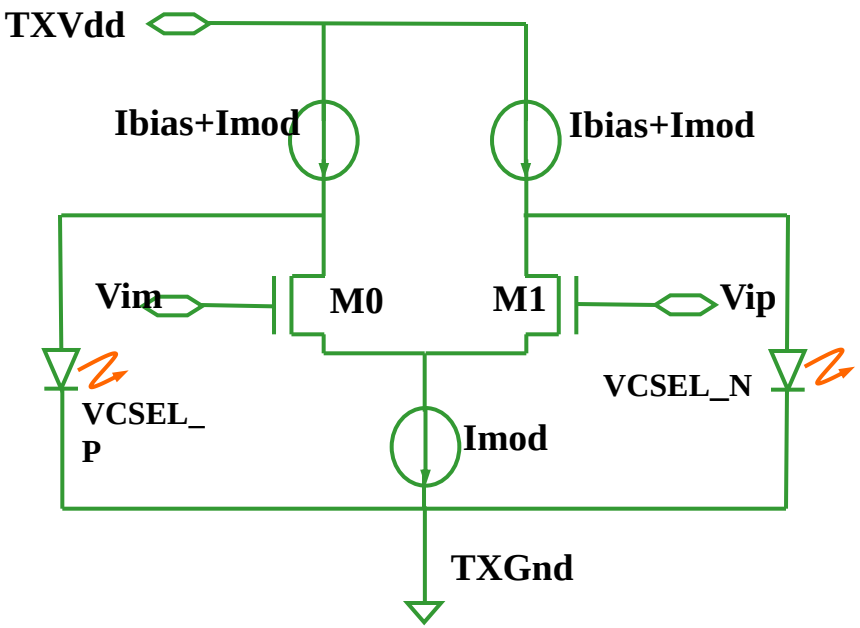
DARPA C2OI

All using 0.5 μm CMOS Silicon-on-Sapphire Technology

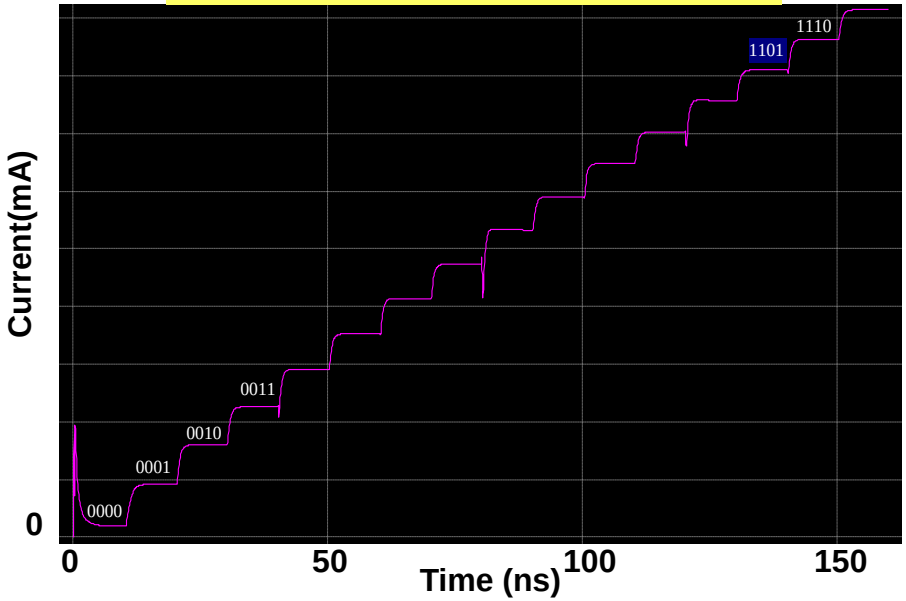
Transceiver IC with OE Devices

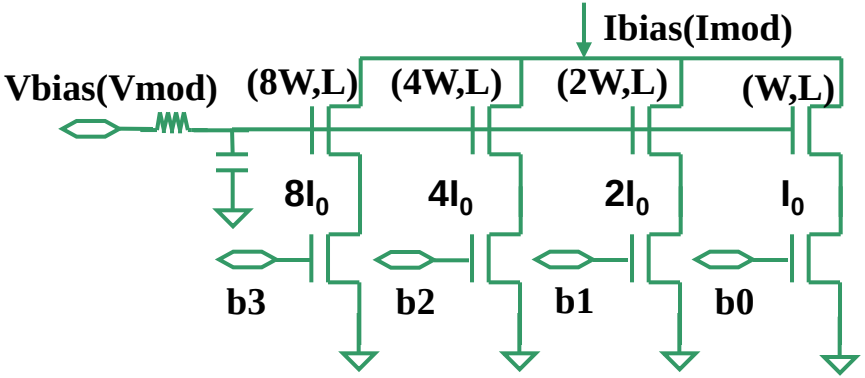


VCSEL Driver Circuit



TX Bias(Modulation) current output

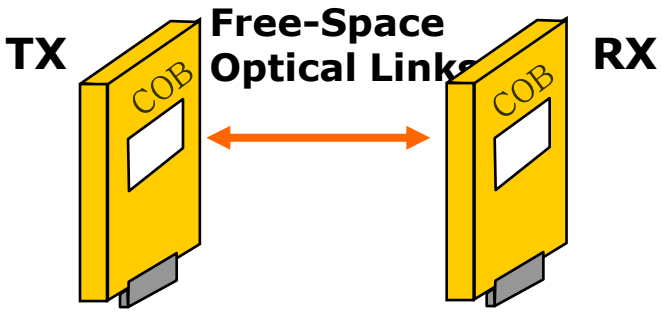


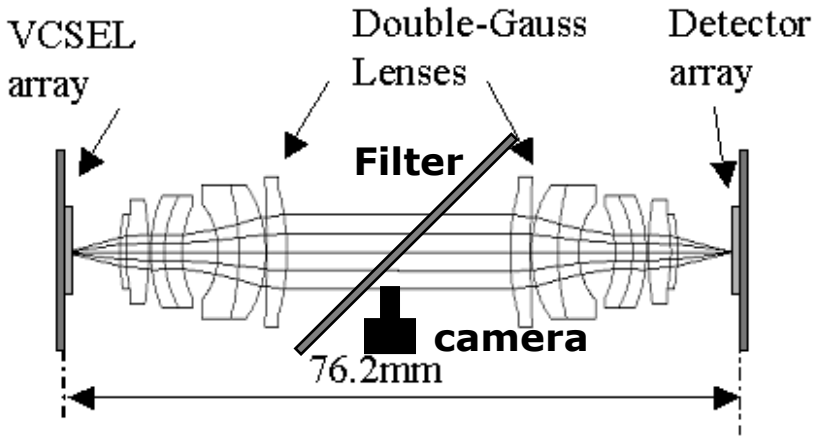


DAC structure for Bias and Modulation Current
b3 b2 b1 b0 are digital control bits

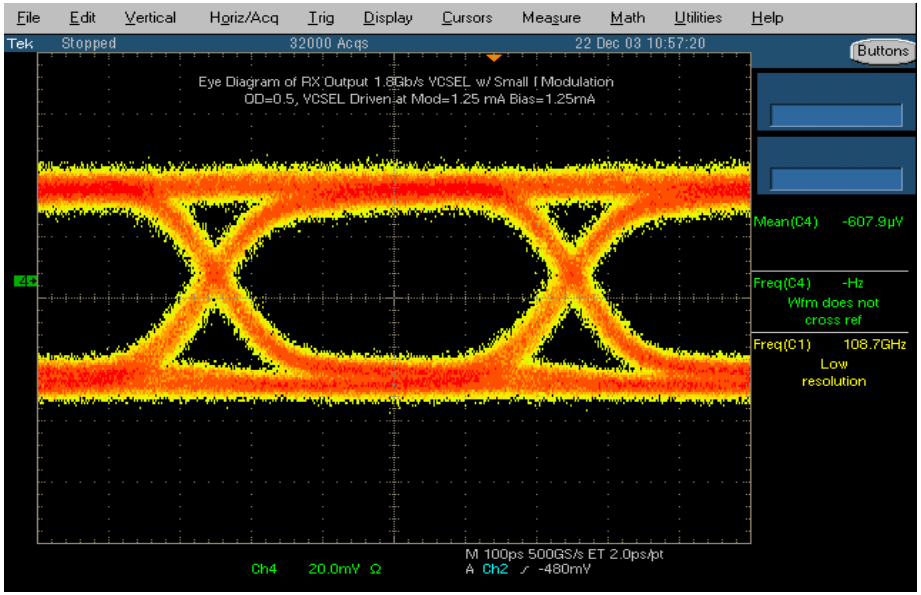
- Digital-to-Analog Converter (DAC) structure allows adjustment of individual Ibias and Imod for greater flexibility.

Laser Driver Eye Diagram



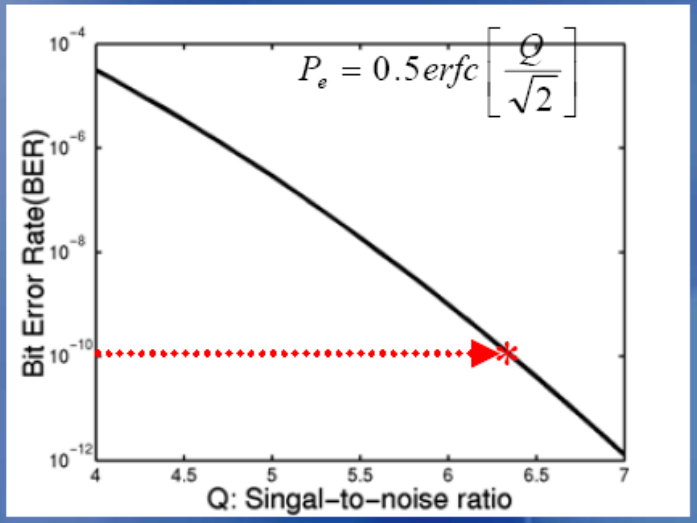


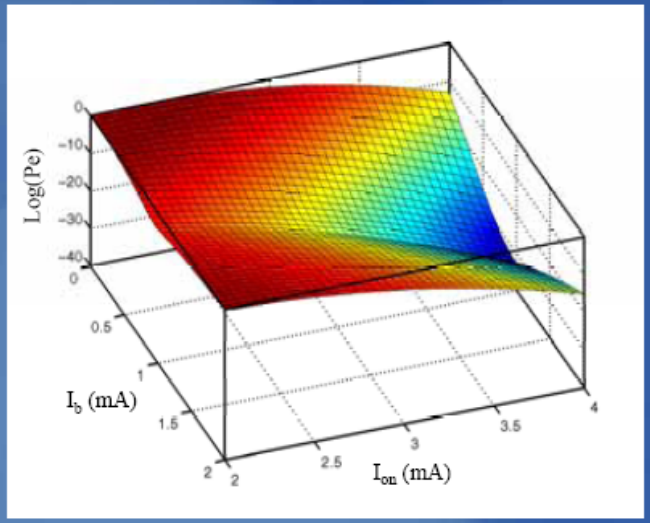
(2^{15}-1 Pseudo random data pattern were used)

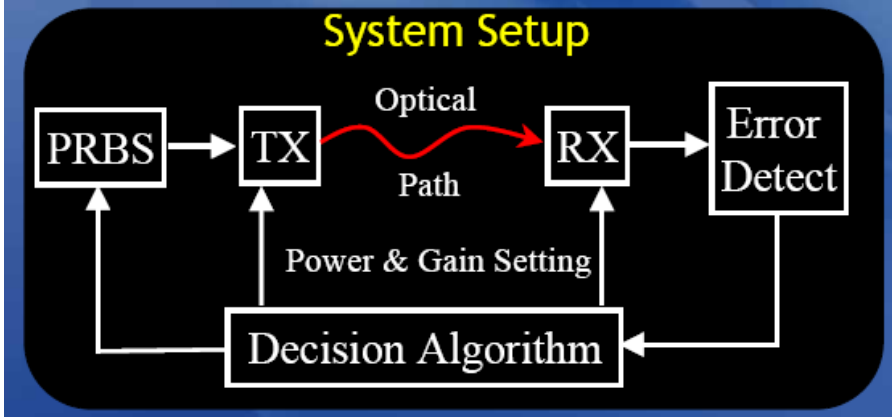


2.0 Gb/s

Dynamic Power Optimization Optical Link





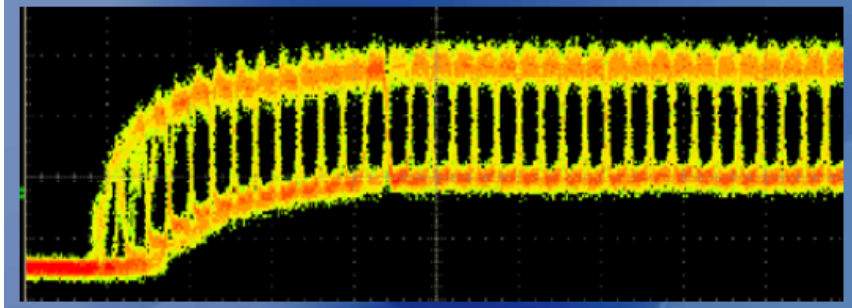


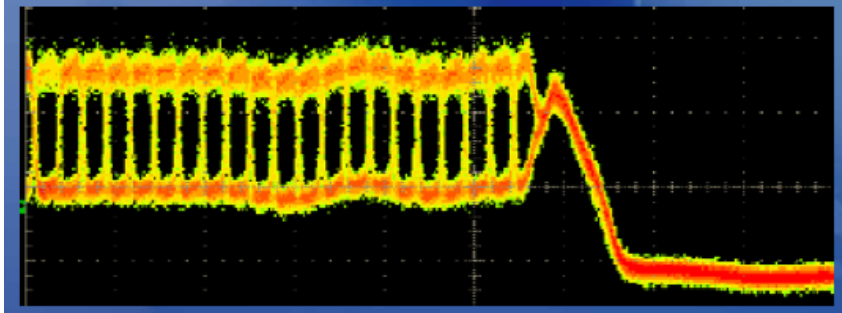
Experiment to Find Optimum Power Setting for VCSEL Driver With and Without Optical Attenuation Filter for 10^{-10} BER

	Receiver Gain Setting	Optimum Power Setting	
		Modulation Current (mA)	Bias current (mA)
Without Filter	Gmax	0.45	1.5
With Filter	Gmax	0.75	1.5

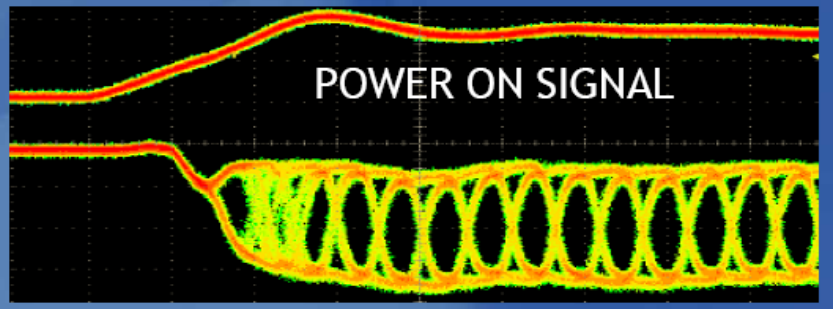
Instant On/off optical link demonstration

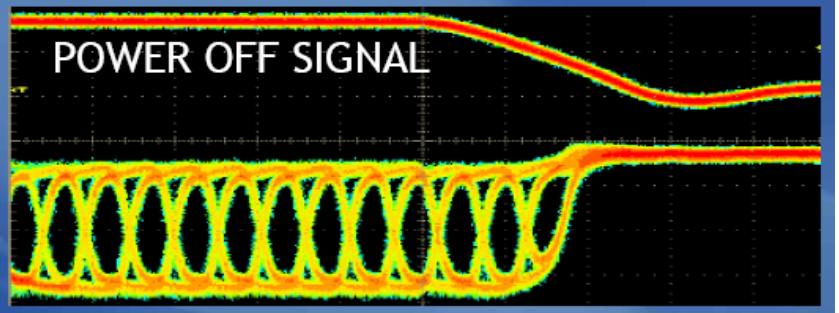
2Gb/s Transmitter Eyes





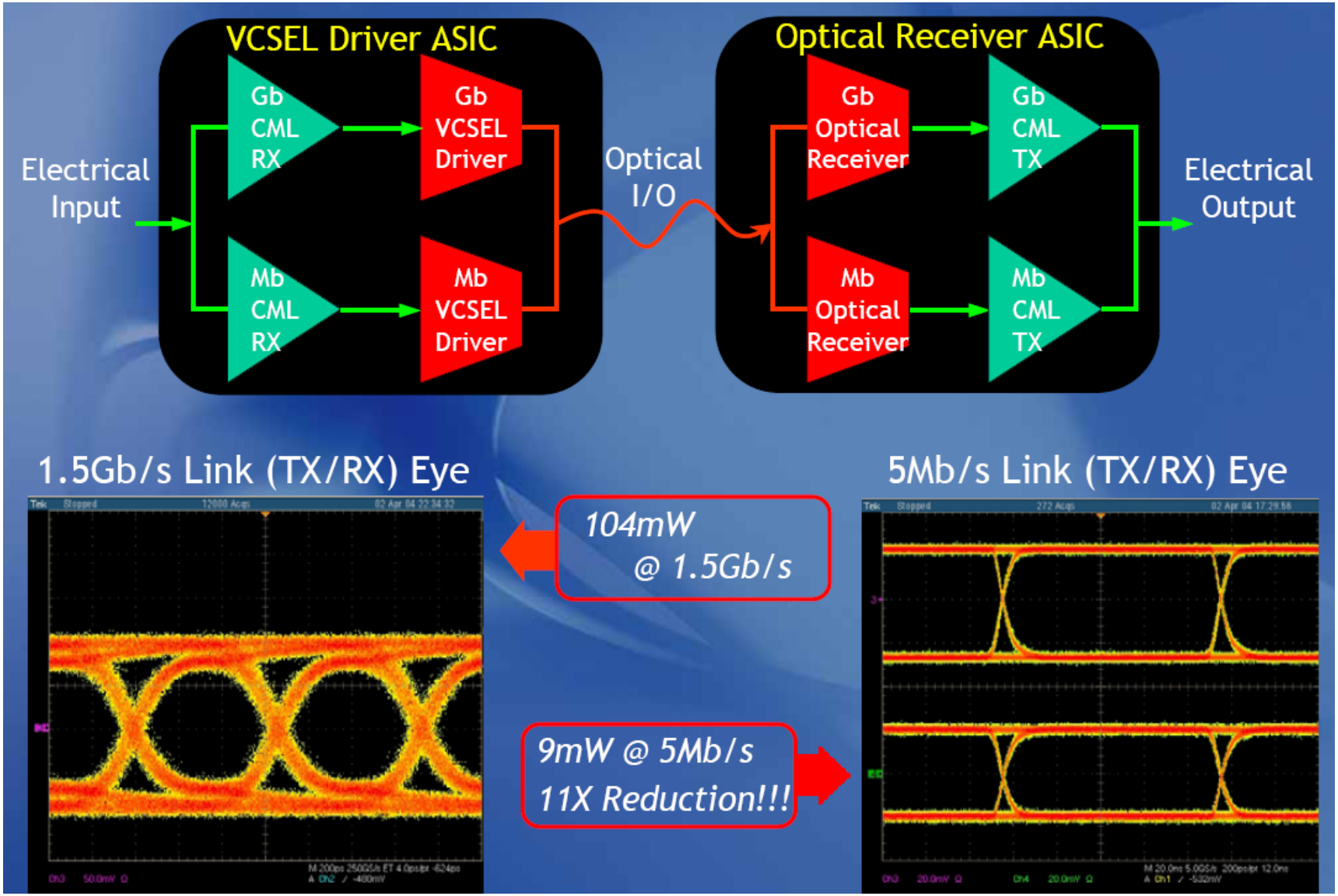
2Gb/s Link (TX+RX) Eyes



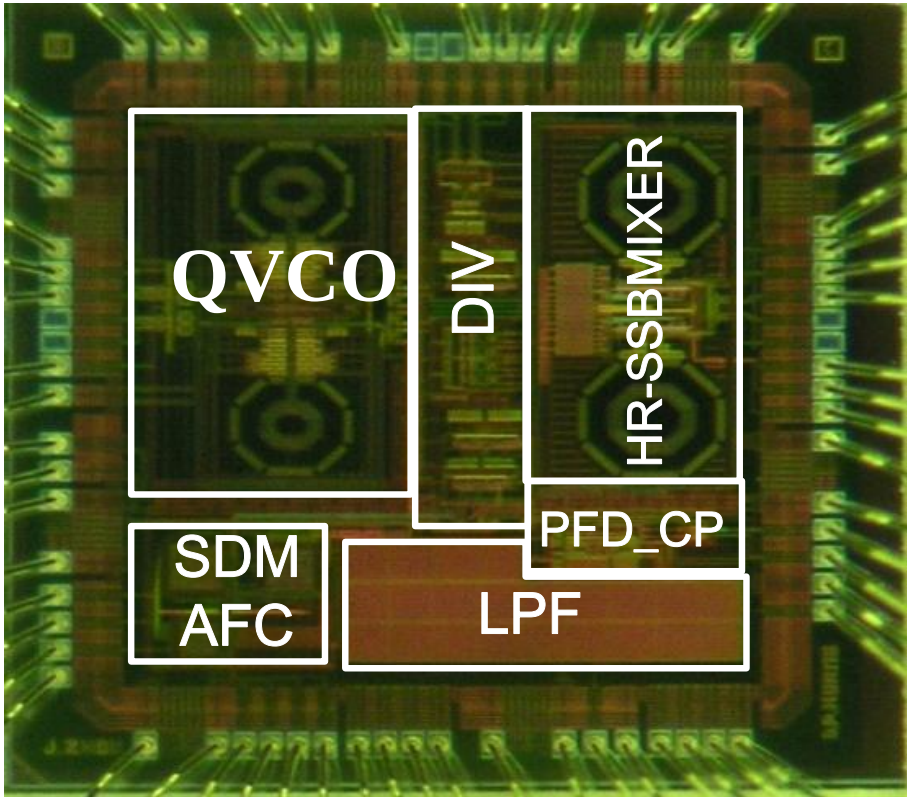


Complete power cycling (on/off) for a gigabit optical link demonstrated at 5-10nSec.

Dual Rate Optical Link



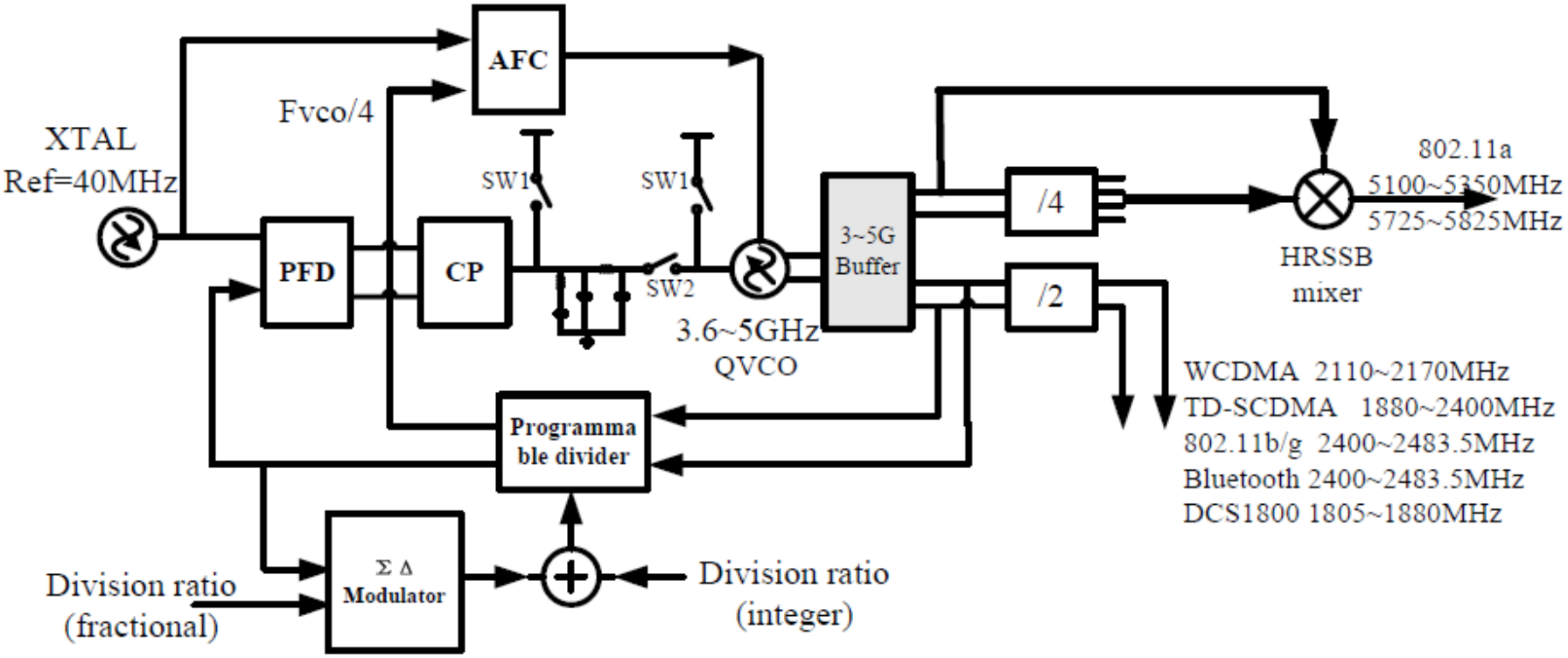
Low Phase Noise, 0.2 to 6 GHz Wideband LC Fractional-N PLL



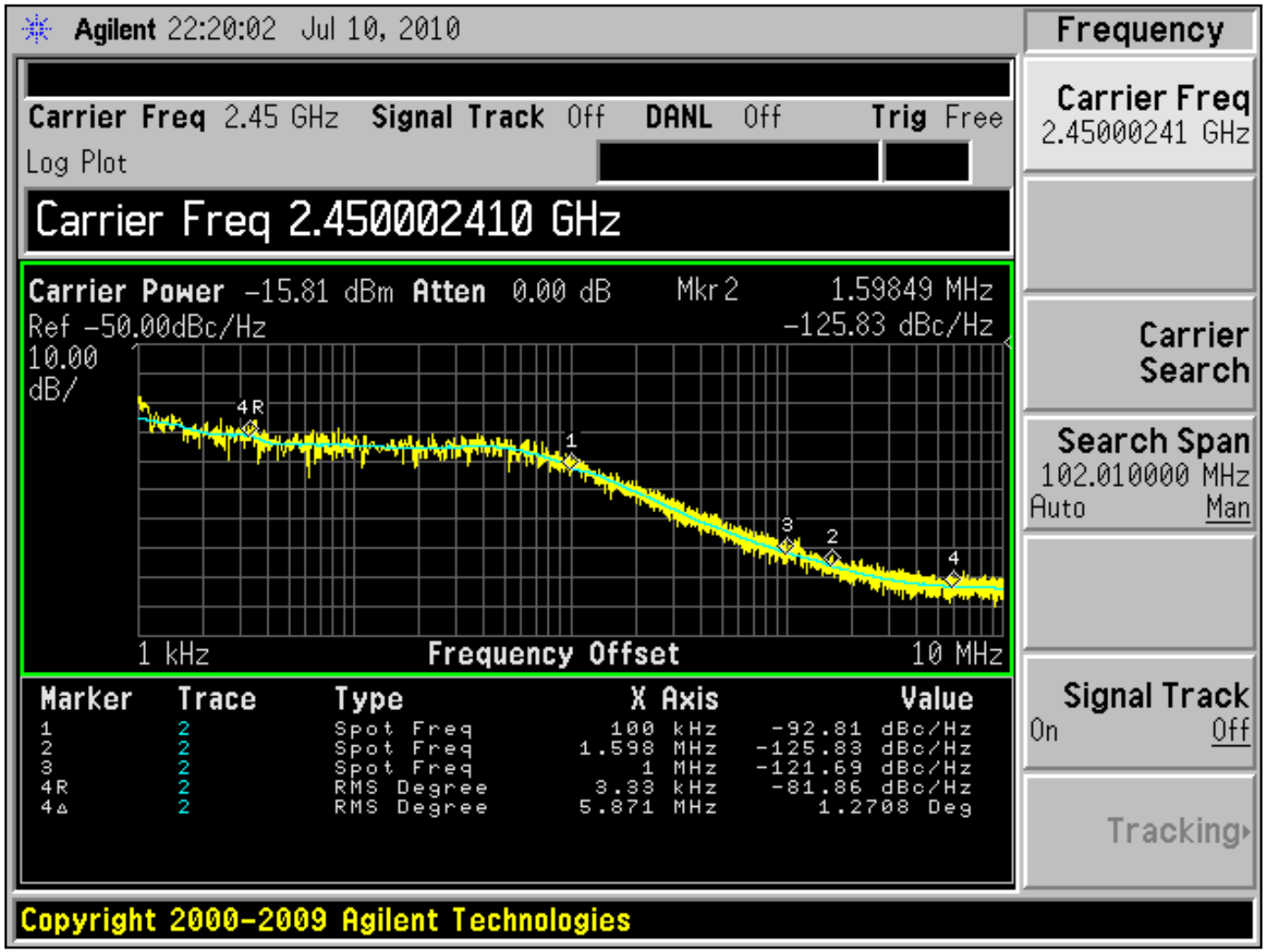
- TSMC 0.13 µm CMOS
- Frequency range: 0.2 to 6 GHz
- I and Q outputs
- Phase noise: -122 dBc/Hz @1MHZ offset (2.4 GHz band)
- Reference spur: better than -69 dBc@40MHz
- Fractional spur: better than -73 dBc@1MHz
- Die area:1.36 mm ×1.37mm
- Power: 35.6 ~ 52.62 mW
- Supports multi-band wireless communication standards including DCS1800, WCDMA, TD-SCDMA, Bluetooth, 802.11 a/b//g

Frequency Synthesizer Architecture

- QVCO with HR-SSB mixer
  - Two cross-coupled LC oscillator to provide I and Q
  - HR-SSB mixer is used to suppress spurs
  - High frequency VCO with divider is avoided by QVCO
  - Achieves both low power and lower-spur



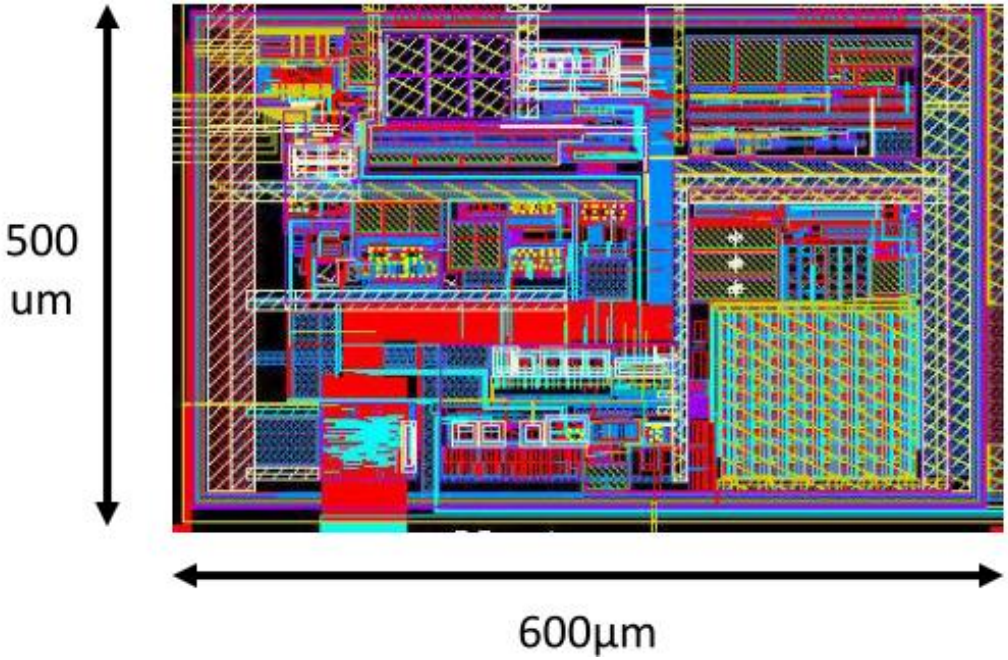
Measurement Results—Phase noise



Measurement Results Summary

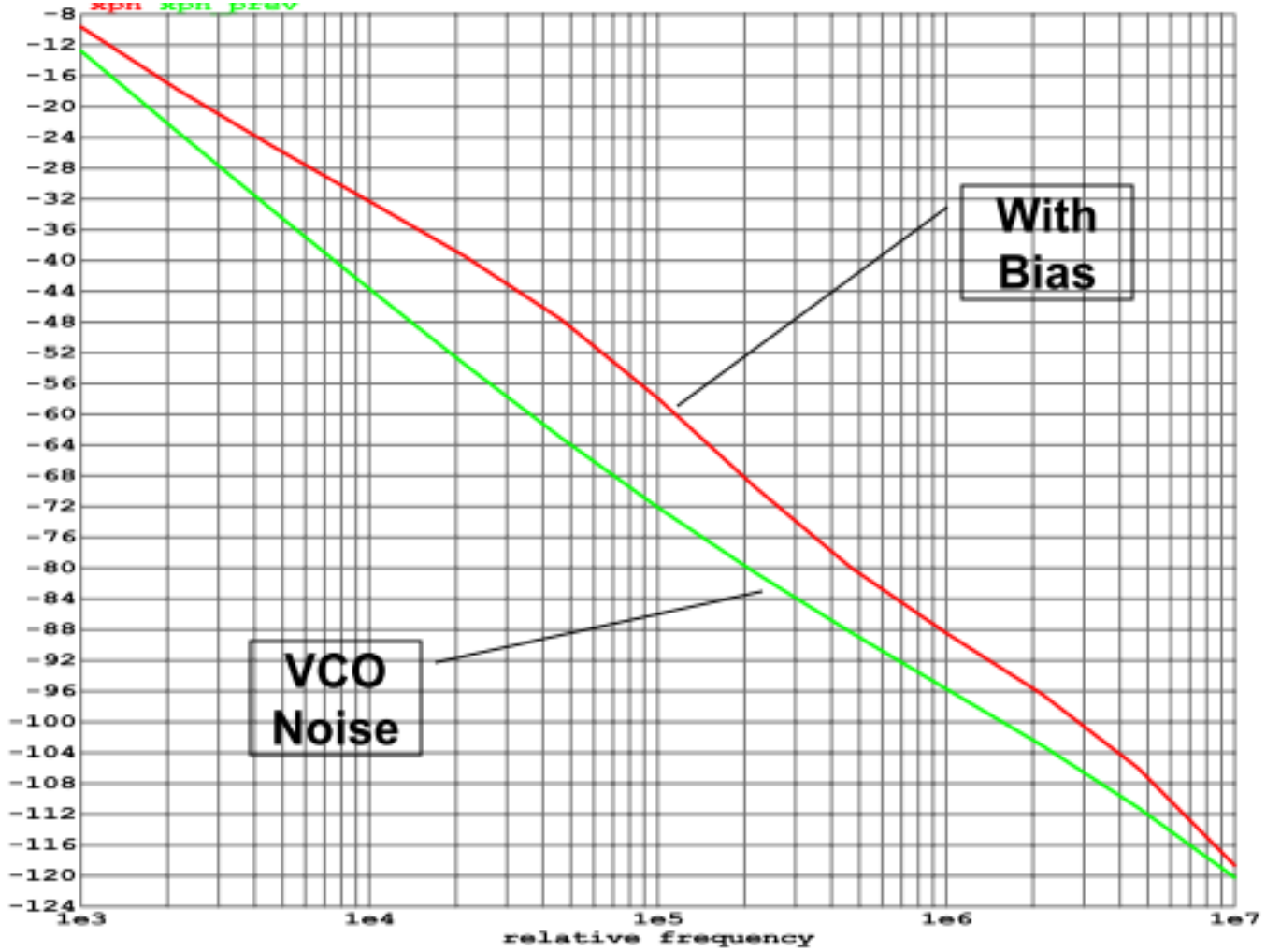
Standards	Phase noise	RMS phase noise
DCS1800 (1805~1880MHz)	-119.18dBc/Hz@600kHz -129.43dBc/Hz@1.6MHz -133.17dBc/Hz@3MHz	0.904°
WCDMA (2110~2170MHz)	-94.72dBc/Hz@100kHz -118.4dBc/Hz@600kHz -124.3dBc/Hz@1MHz	0.975°
TD-SCDMA (1880~2400MHz)	-93.46dBc/Hz@100kHz -122.55dBc/Hz@1MHz -126.29dBc/Hz@1.6MHz	1.789°
Bluetooth (2400~2480MHz)	-92.81dBc/Hz@100kHz -121.69dBc/Hz@1MHz -125.83dBc/Hz@1.6MHz	1.267°
802.11b/g (2400~2480MHz)	-92.81dBc/Hz@100kHz -121.69dBc/Hz@1MHz -125.83dBc/Hz@1.6MHz	1.267°
802.11a (5180~5805MHz)	-85dBc/Hz@100kHz -107.63dBc/Hz@600kHz -114.17dBc/Hz@1MHz	2.65°
Loop bandwidth	60 kHz ~ 90 kHz	
Locking time	<50 μs	
Reference Spur	<-69dBc@40MHz	
Fractional Spur	-72.93dBc@1MHz	
Power	35.6 ~ 52.62 mW	
Die Area	1.36×1.37mm^2(core circuits)	

Ring PLL



- 0.35 µm CMOS
- Area: 600 µm x 500 µm
- Power: 18 mW
- Frequency range: 400Mhz to 2GHz
  - Support data-rate from 800 Mb/s to 4 Gb/s
- Jitter is less than 5 ps rms supporting BER of 10^{-12}
  - VCO phase noise: -92 dBc/Hz at 1MHz offset
  - VCO phase noise with bias circuit: -85 dBc/Hz at 1MHz offset
- CML outputs for efficient chip clock distribution

Ring VCO Phase Noise



VCO phase noise: -92 dBc/Hz at 1MHz offset

Summary

- **Research Experience**
  - **High-Speed Transmitter and Receiver**
    - Serializer, Line Driver and Laser Driver
    - Radiation-Tolerant Optical Receiver
  - **Phase Locked Loops**
    - LC-Tank Based PLL
    - Ring PLL

- **Collaboration with Fermi Lab**

Q & A

- **Thank You!**