SOI Pixel Sensor Process

Lessons Learned from the Development of SOPHIAS, a Sensor for X-ray Free-Electron Laser Experiments

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RIKEN SPring-8 Center

Collaborators

- RIKEN, JASRI

  All members of SACLA members, especially,

  - Togo Kudo, Yoichi Kirihara, Shun Ono, Kazuo Kobayashi, Masahiko Omodani
  - Toshiaki Tosue, Toshiharu Nakagawa, Yoshiro Fujiwara
- Univ. of Hyogo
  - Takeo Watanabe, Nobukazu Teranishi
- KEK

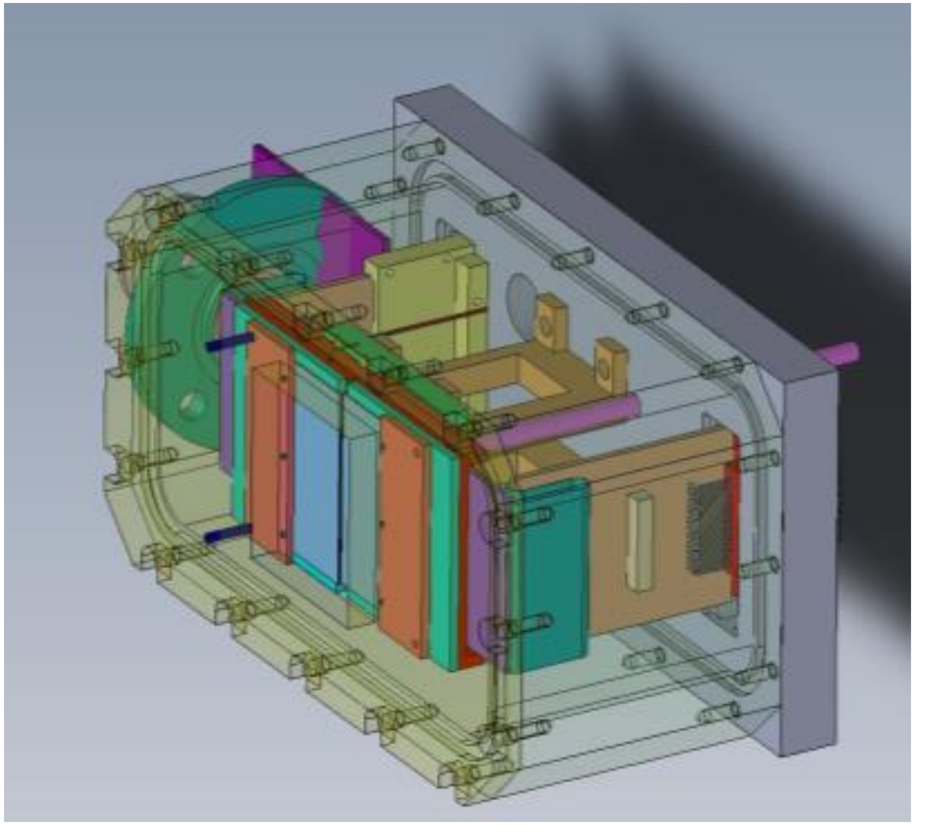
  Yasuo Arai, and SOIPIX collaboration
- Private Sector
  - Lapis Semiconductor, A-R-Tec Corp.
- Detector Advisory Committee
  - Peter Denes (chair, LBNL), Andrew Holland (The Open Univ.), Gregory Deputch (Fermilab), Yasuo Arai (KEK)


SPring-8 (8 GeV SR)
Experimental Hall
SACLA (8 GeV XFEL)
injector
700 m
• 2nd X-ray Free-Electron Laser Facility after LCLS
• Shortest wavelength lasing achieved
• Compact XFEL facility
T. Ishikawa et.al., Nature Photonics(2012)

SOPHIAS

- CMOS sensor with Thick Silicon Photodiode
  - 500 μ m thick

- Schedule
  - Fall 2014
    - in-house test campaign
  - Dual Sensor Detector
    - 3.8 Mpixels
  - Target:
    - Coherent X-ray Imaging



SOPHIAS Sensor

Specifications	SOPHIAS	MPCCD
Pixel Size	30 μm	50 μm
Pixel Number	1.9 M	0.5 M
Frame Rate	60 frame/sec	60 frame/sec
Noise	150 e-rms	300
Peak Signal	7 Me- 16-20 Me-/100 μm□	4-5 Me- 77 Me-/100 μm□

Raw ADC output : 56 bit/pixel
6.4 Gbps/sensor → 12.8 Gbps/ 2 sensors

This can be reduced by calibration on FPGA, down to 7.3 Gbps/2sensors

Components that can handle 10-20 Gpbs is under developments

What we want to MEASURE ?

In Realiz

Quantum beam

- X-ray, (electron, proton, ion, ….)

On

- Arrival Position
- Arrival Time
- Particle number
- Internal quantity
  - Energy
  - Charge
  - mass
  - Spin
  - Vector
  - .
  - .
- Correlation

Parti

Integration

Pixel

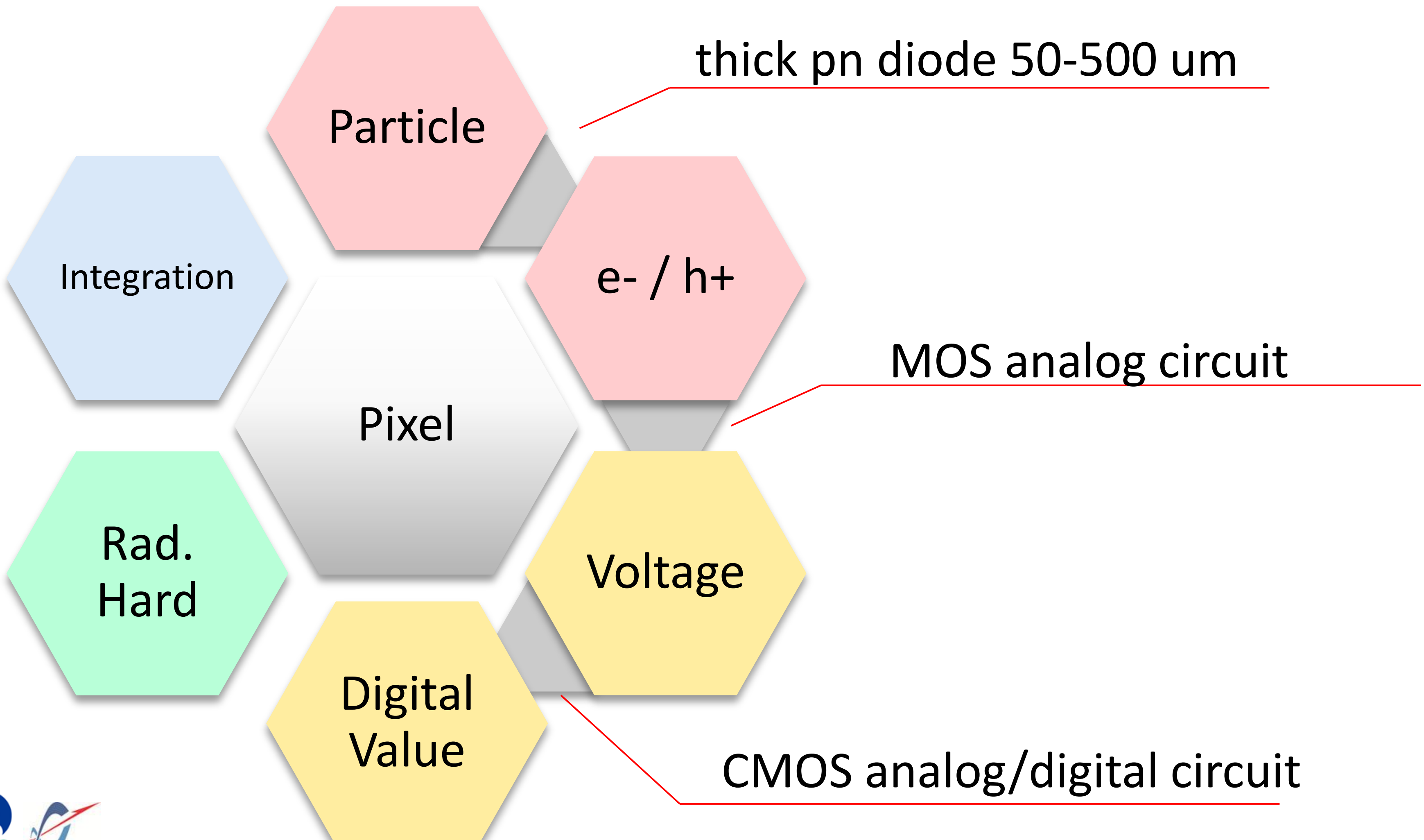
Rad. Hard

Voltage

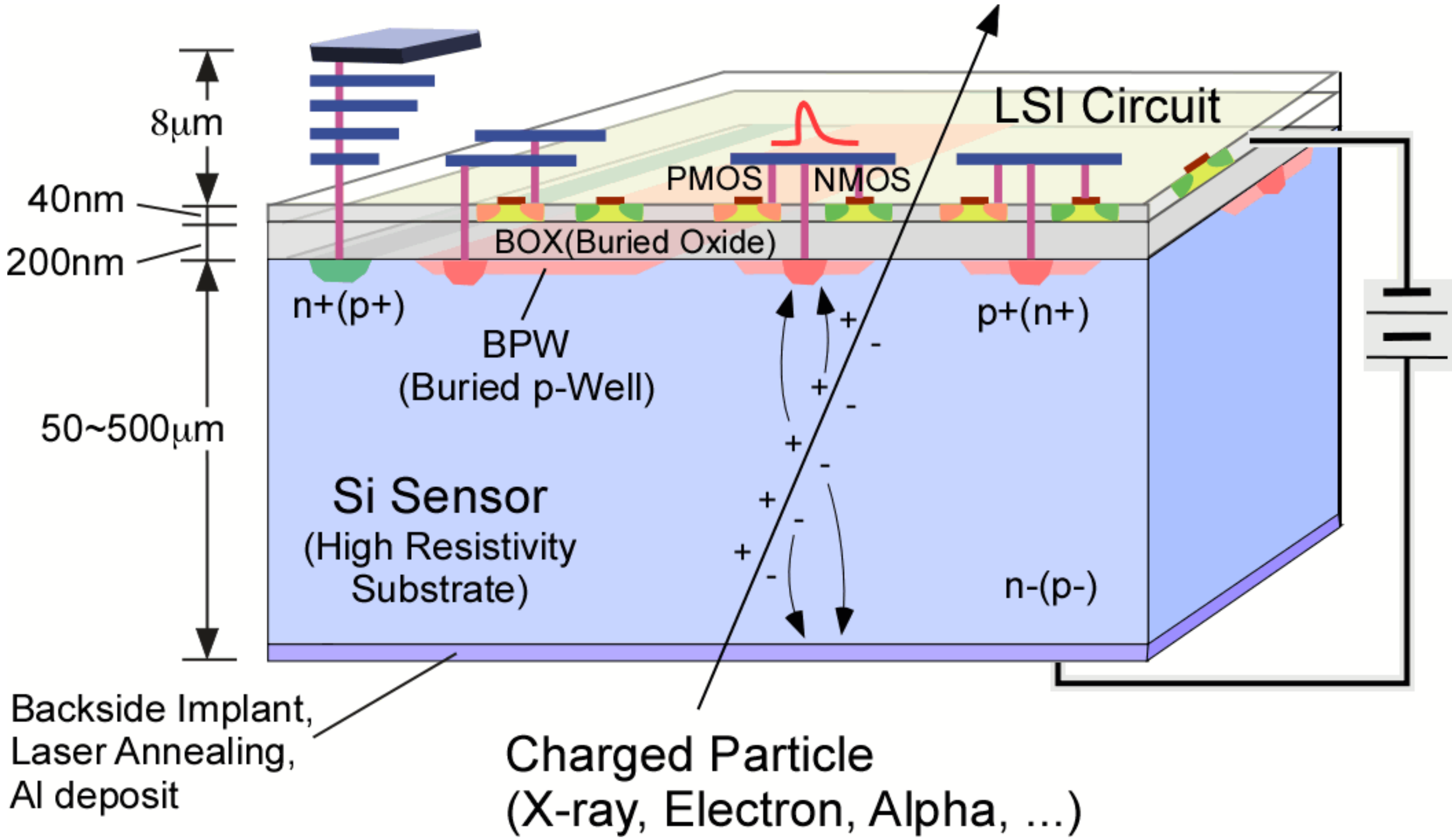
Digital Value

What we want to MEASURE ?

In Realization

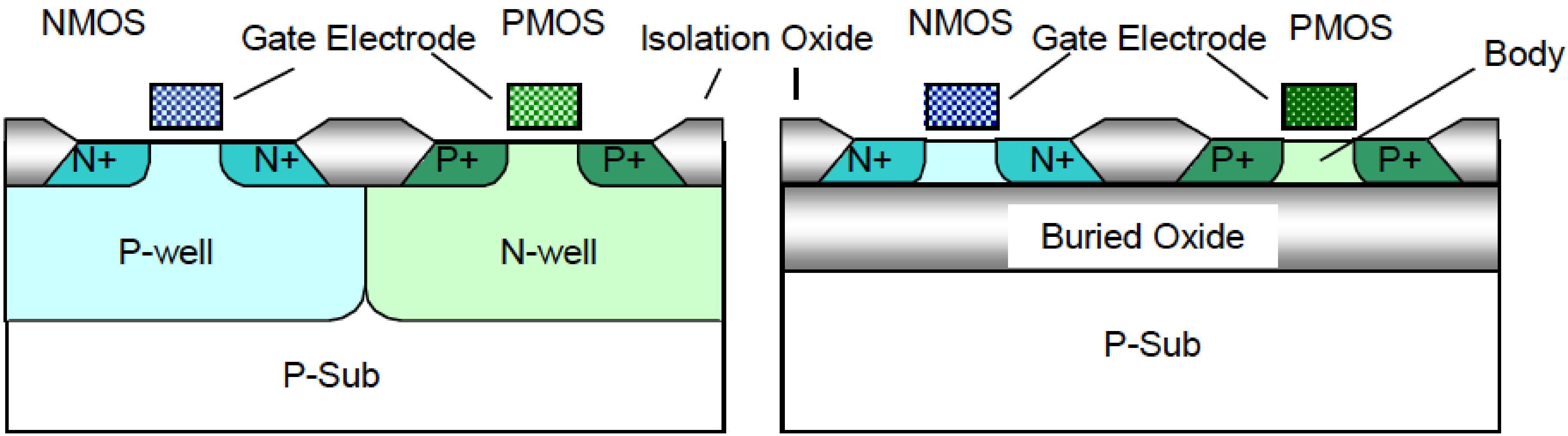


SOI Pixel Detector: an Overview



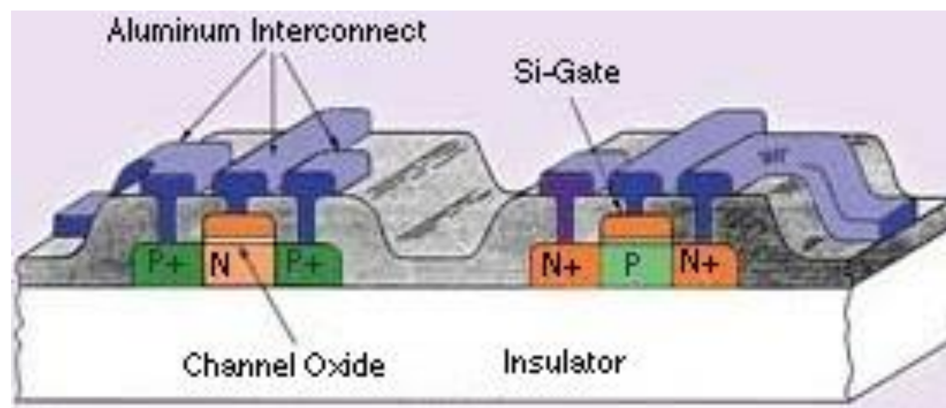
CMOS + Thick Silicon *pn* diode

Bulk CMOS vs. Fully depleted SOI CMOS



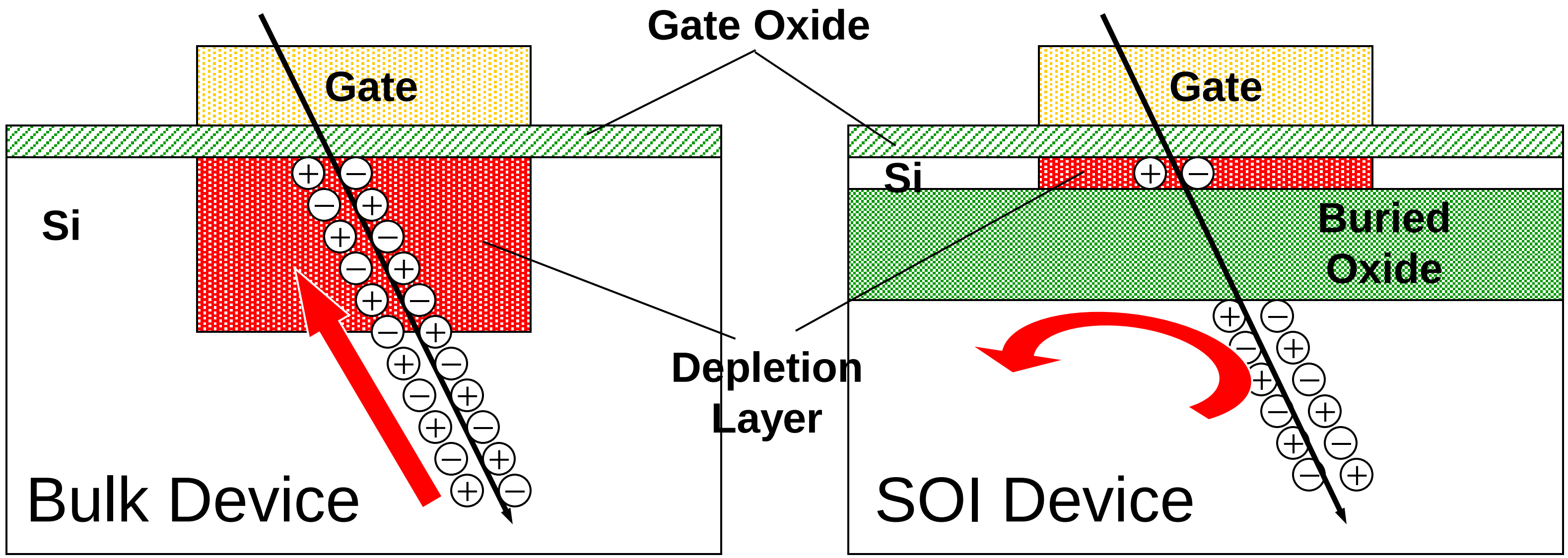
Bulk CMOS **SOI CMOS**

In SOI, Each Device is completely isolated by Oxide.

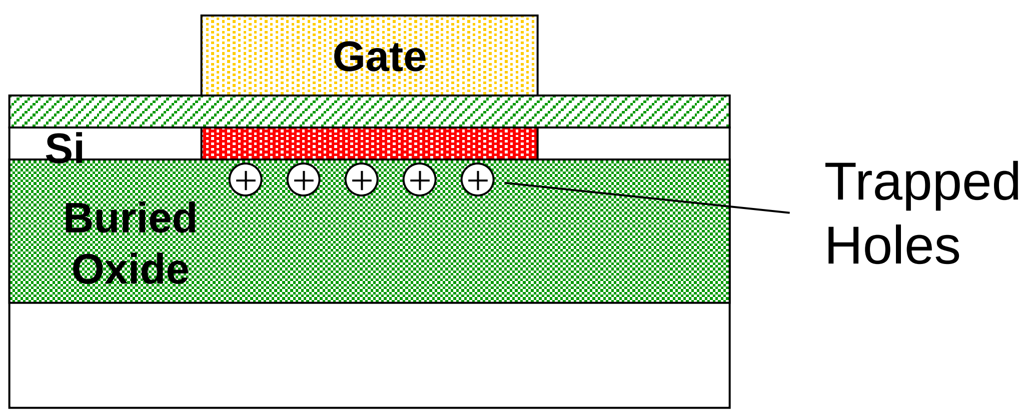


Radiation Tolerance

SOI is Immune to Single Event Effect

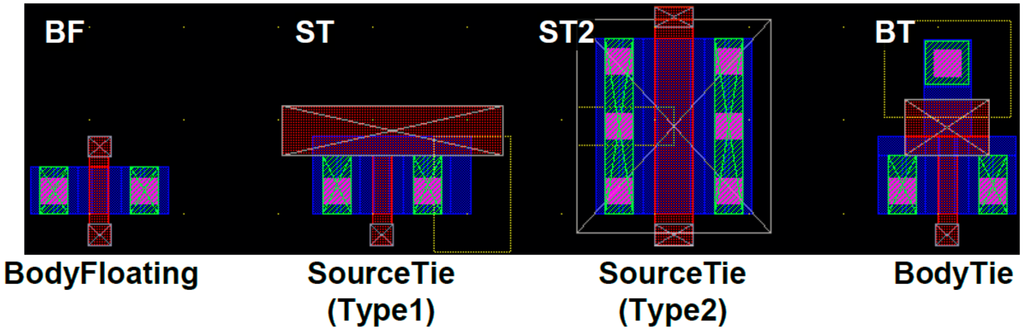


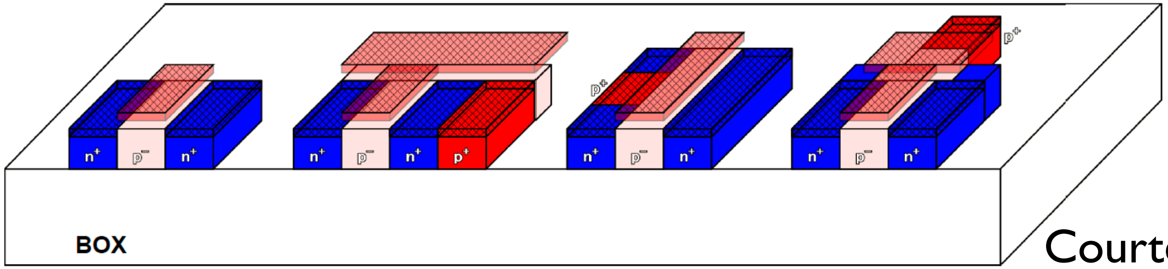
But rather weak for Total Ionization Dose due to thick BOX layer



Introduction of new devices

- Fully Depleted SOI Transistor (FD-SOI Tr):
  - Body Floating Tr
    - Large 1/f noise due to body floating
- Source Tie/Body Tie Transistor
  - Pcell has been introduced.
  - 1/f noise simulation environment has been successfully introduced.
  - Transistor for 2.5 V for high dynamic range sensor

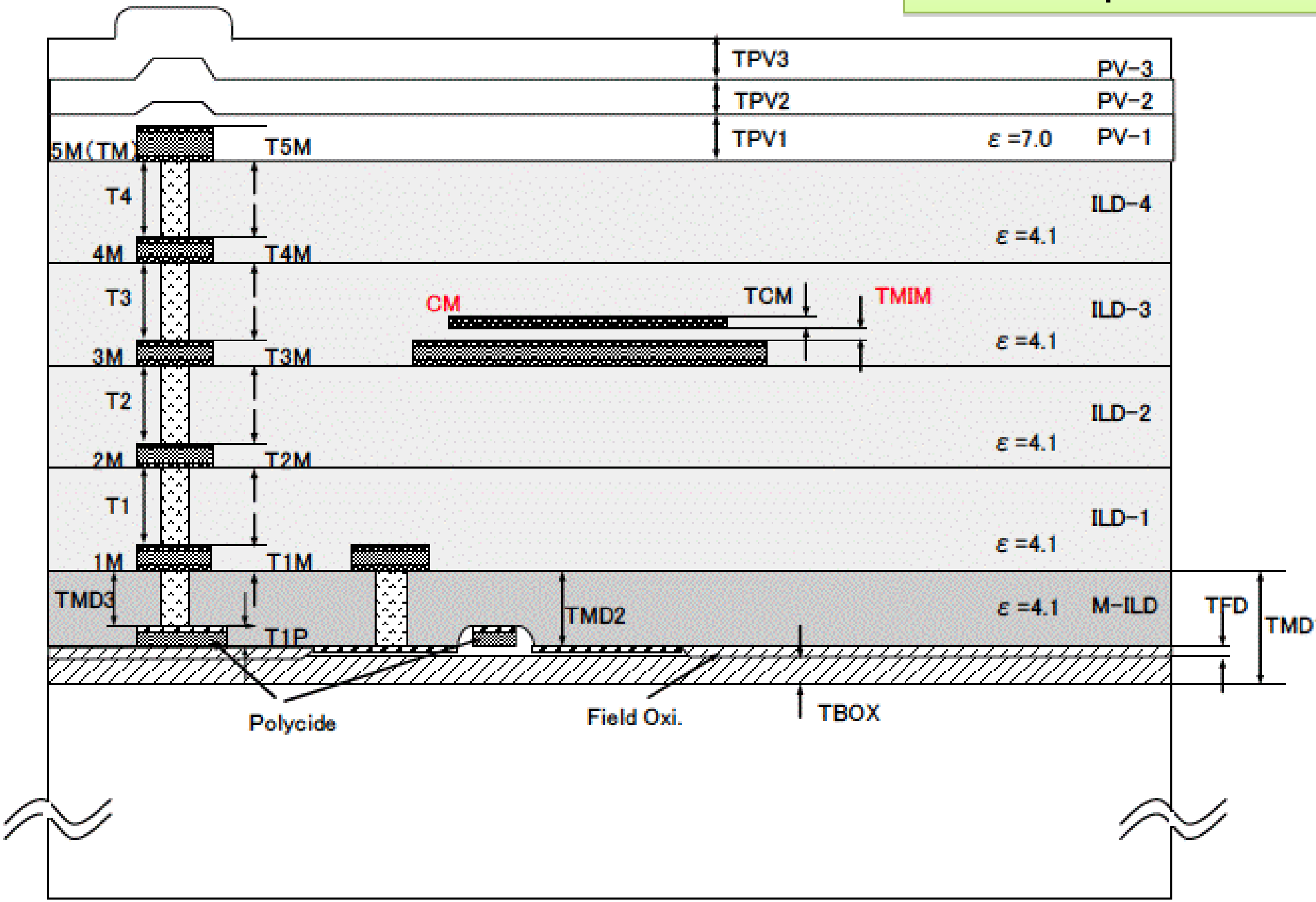




Courtesy of A-R-Tec

Structure of Top Si

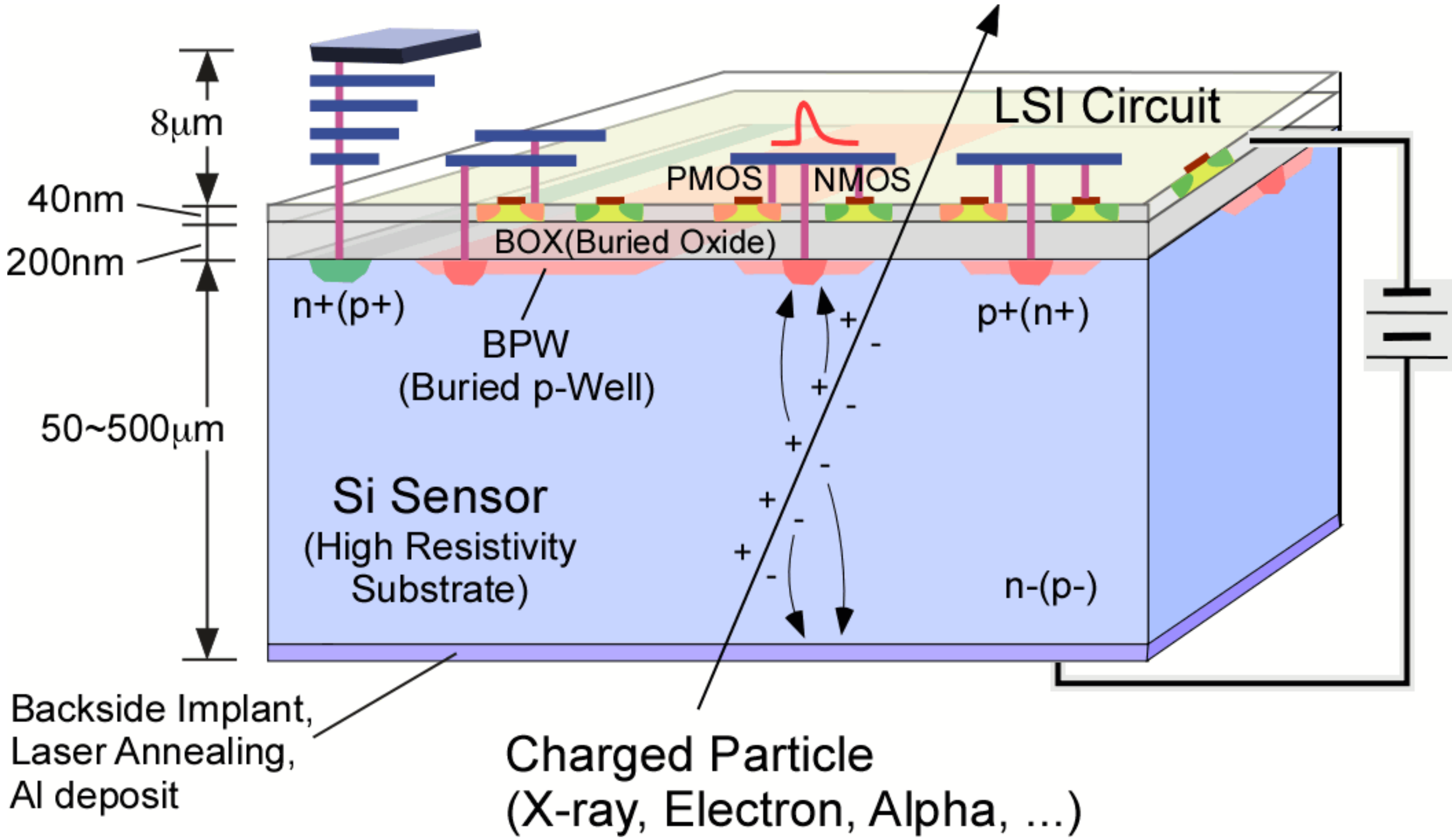
1 Poly + 5 Metal
MIM Capacitor on 3M



Fully Depleted SOI CMOS Transisters

- High Speed / Low Power
- Immune to Single Event Upset
- Low Temperature Operation
- Analog optimized Source/Body Tie Transistors
  - Suppression of body floating.
- 2.5 V Transistor available for high dynamic range sensors
- 5M with MIM Capacitor on 3M
  - For production of large-area sensor

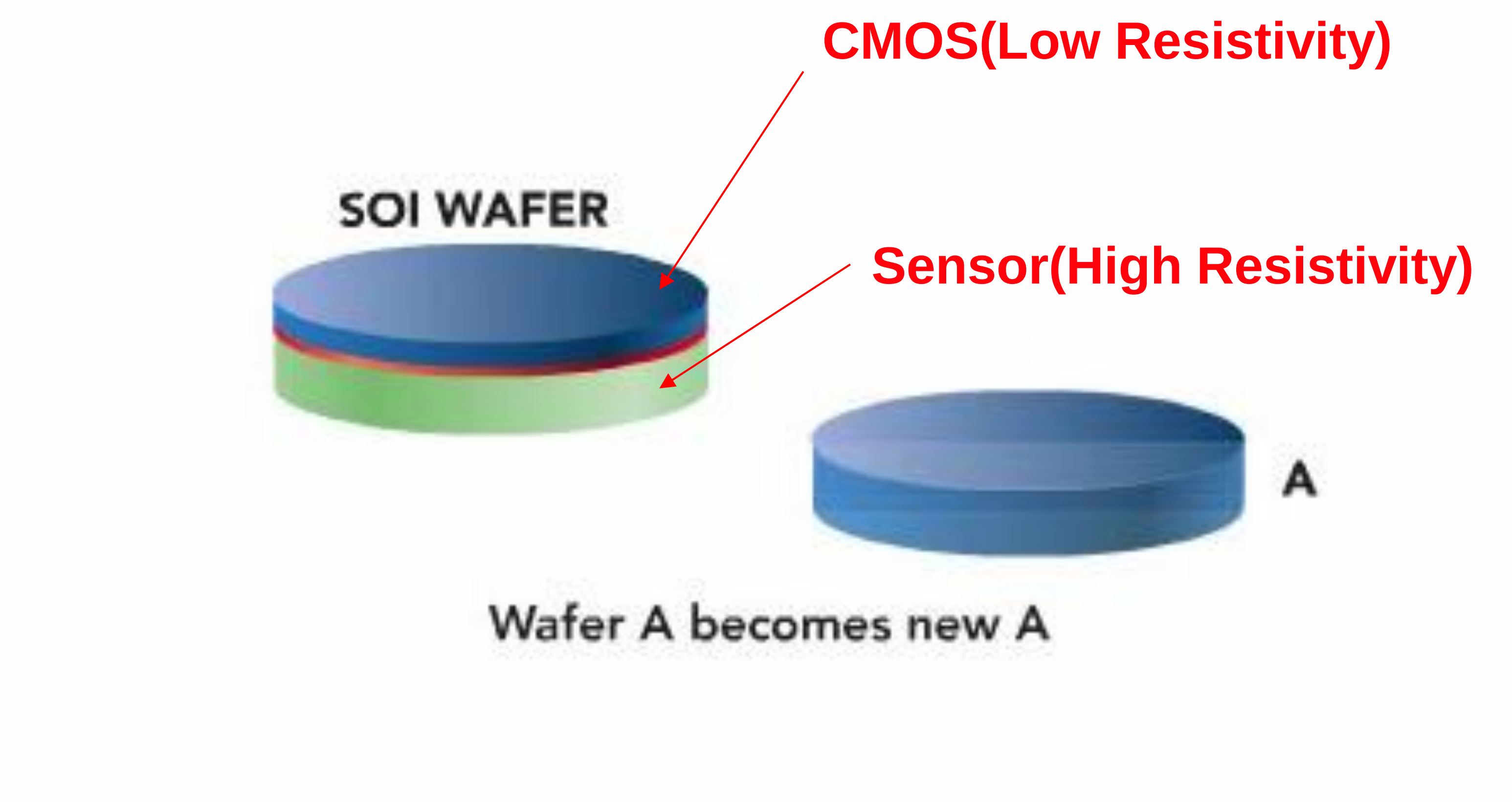
SOI Pixel Detector: an Overview



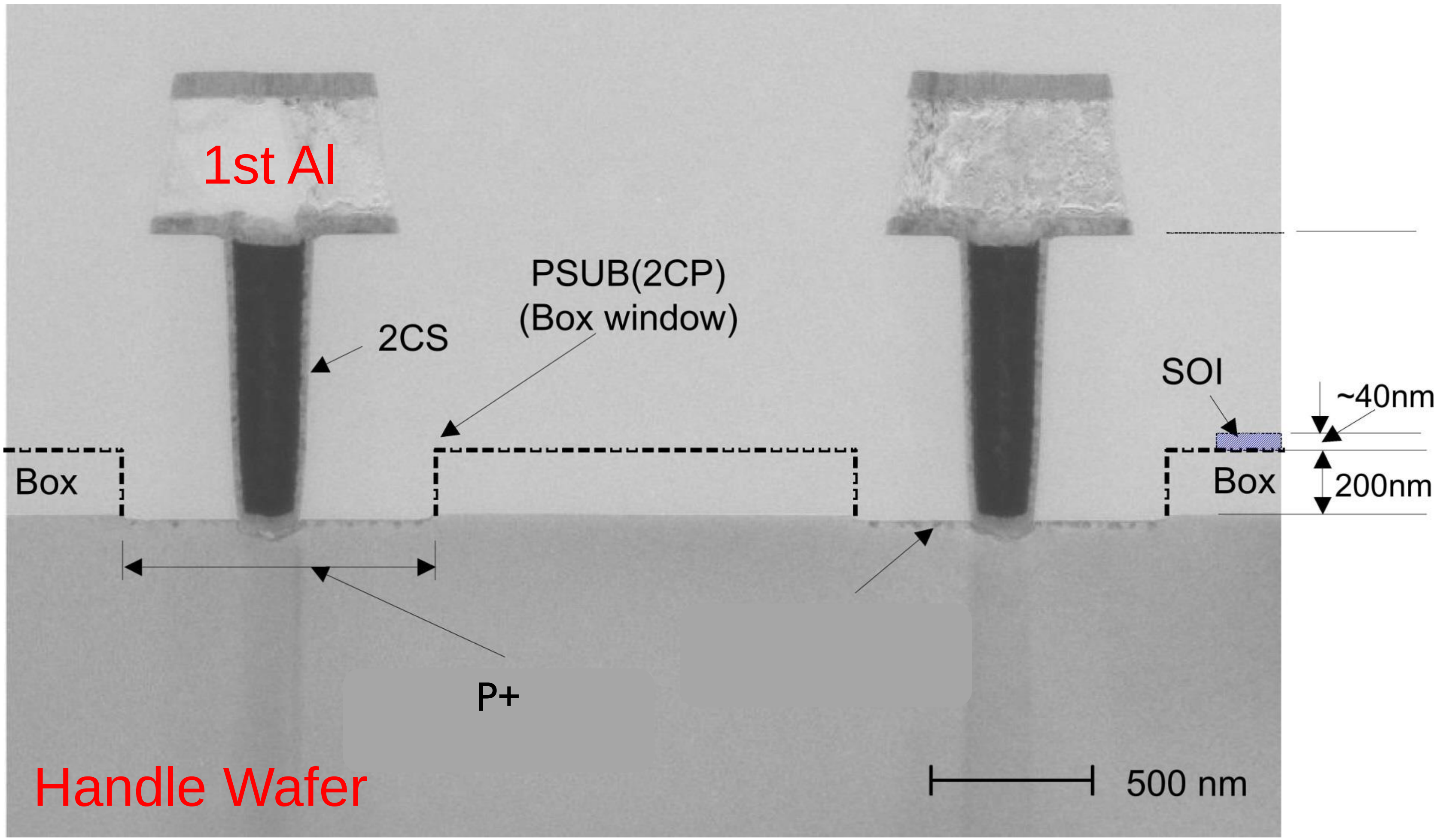
CMOS + Thick Silicon *pn* diode

SOI (Silicon-on-insulator) Wafer

Smart Cut by SOITEC

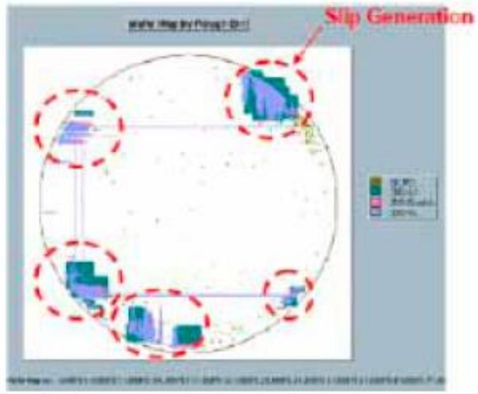
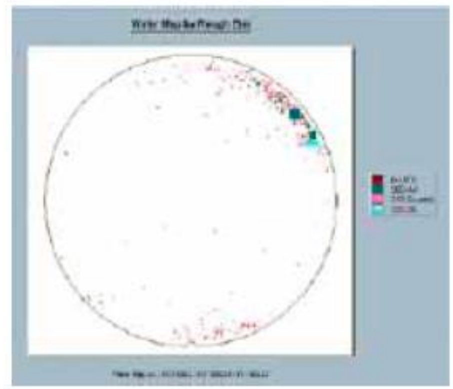
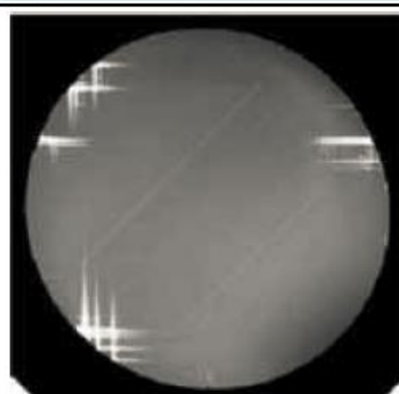


Connection Between *pn* diode and CMOS

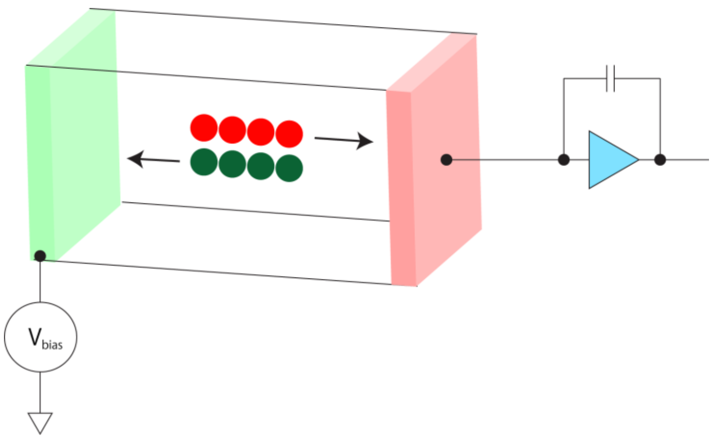


8 Inch Floating Zone SOI wafer for full depletion of 500 um

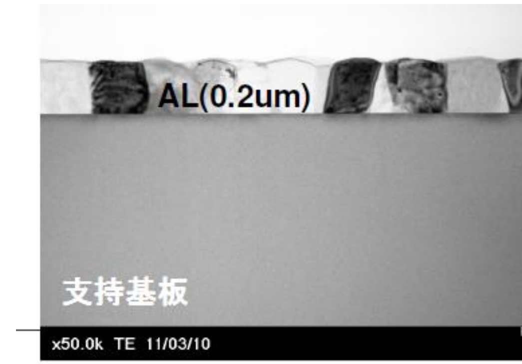
Courtesy of Lapis Semiconductor

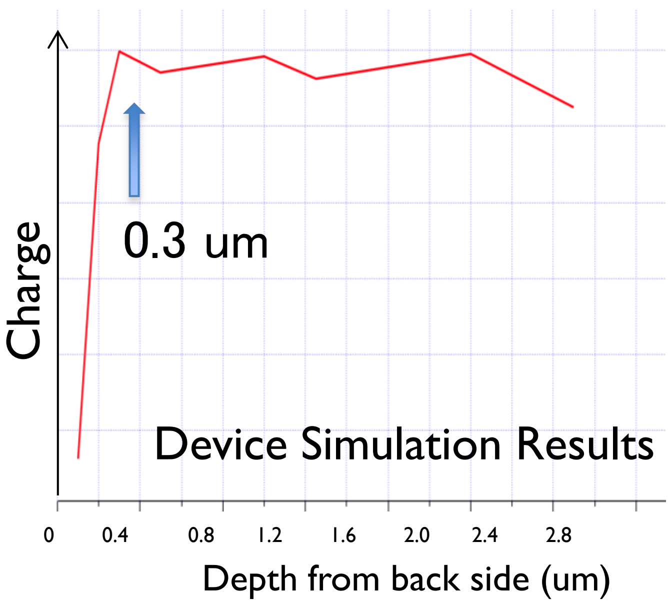
	Conventional Process	Improved Process	tool
SOI wafer fabrication			KLA Tencor SP-1
Pixel detector fabrication			X-ray Topography

Backside processing

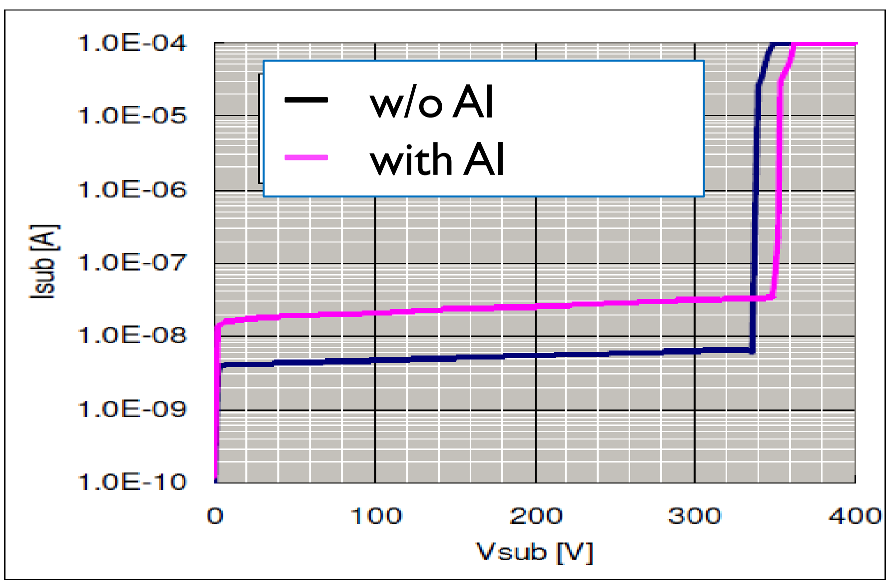


Backside Processing
- CMP
- Wet etching
- Implant
- Laser annealing
- Al deposition





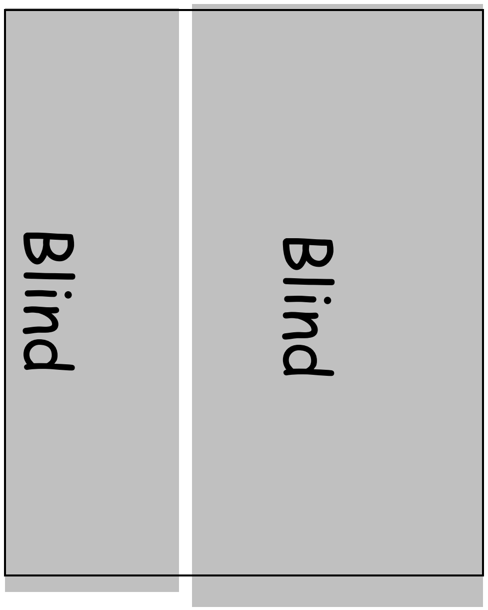
Inverse current

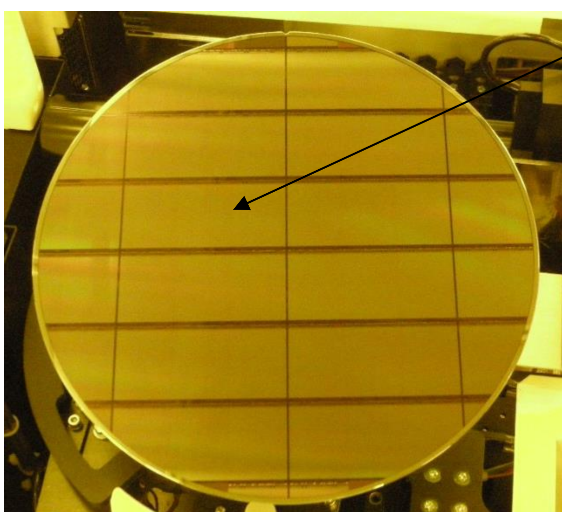


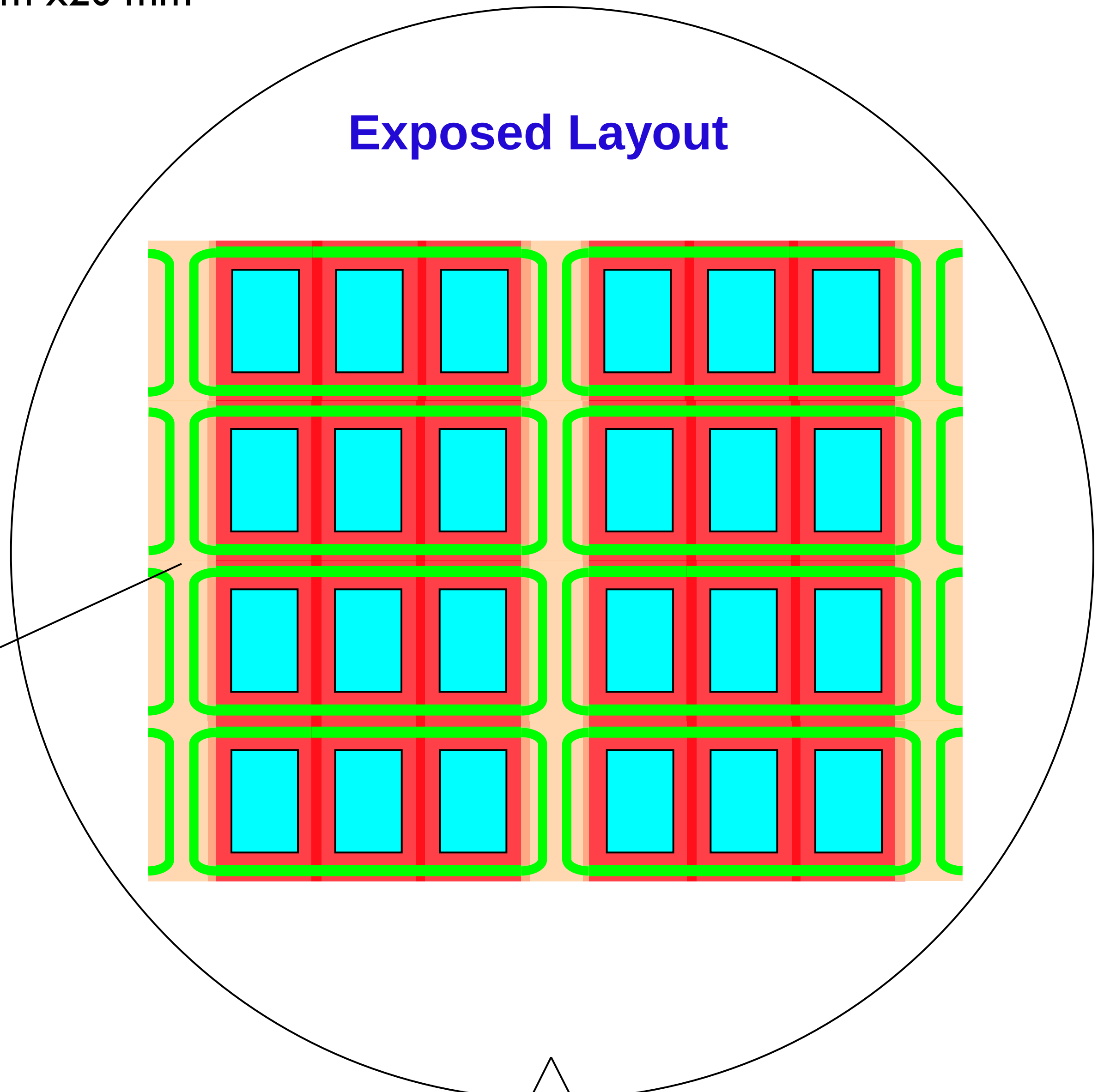
Technology CAD simulation by Kirihara & Hatsui (RIKEN)

Stitching Exposure

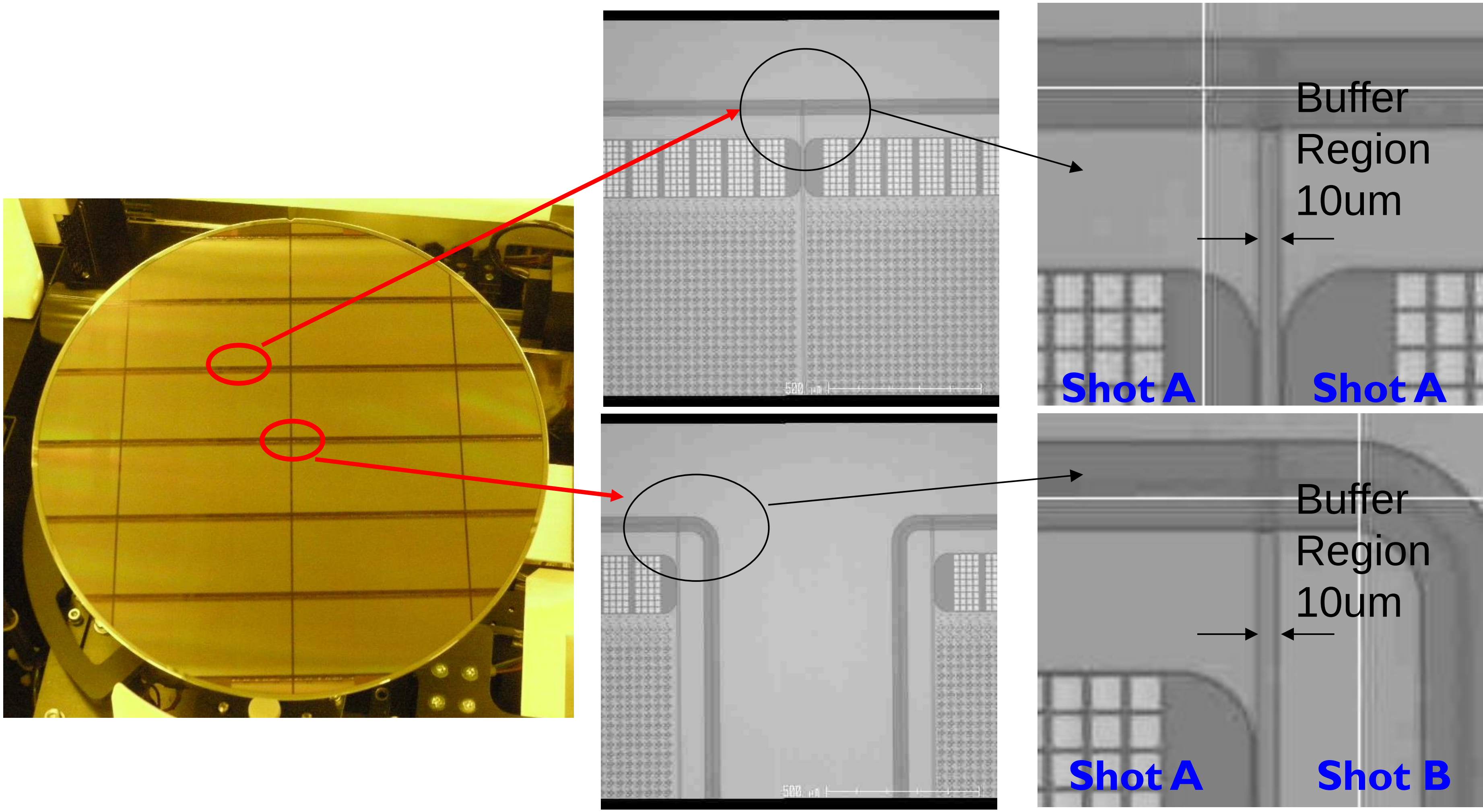
Mask Layout ~30 mm x20 mm





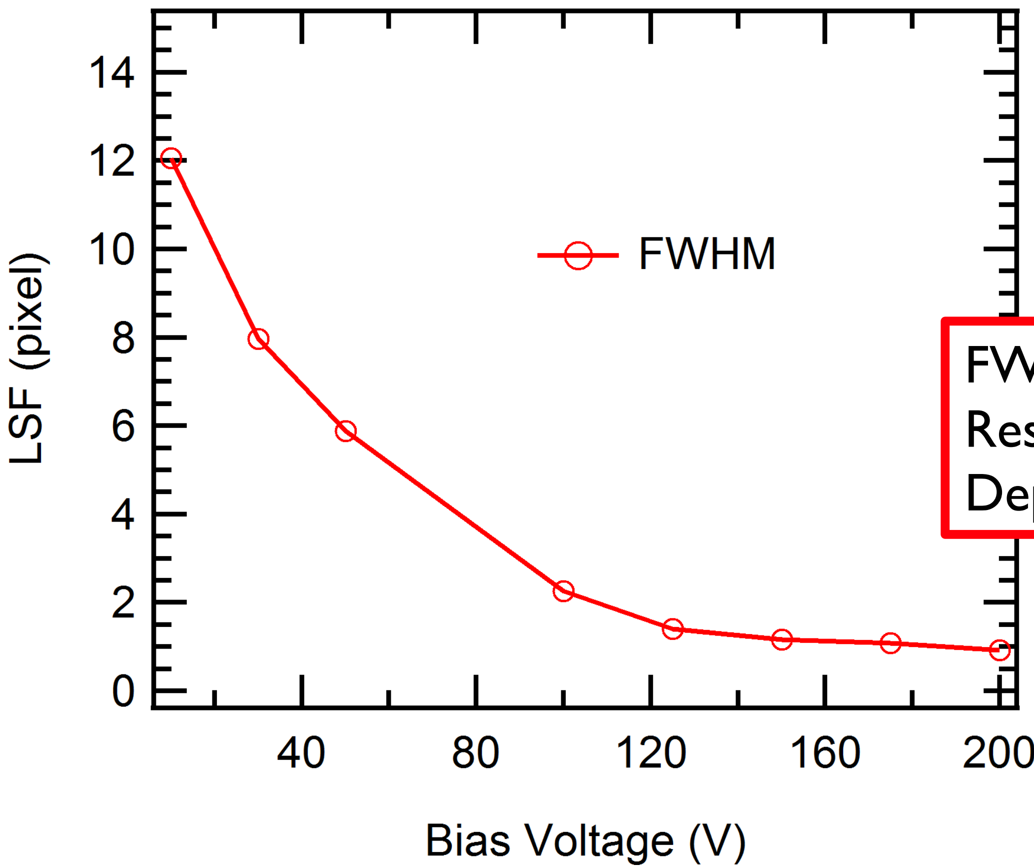


Stiching Accuracy



- Width of the Buffer Region can be less than 10um.
- Accuracy of Overwrap is better than 0.025um.

Line Spread Function against X-ray

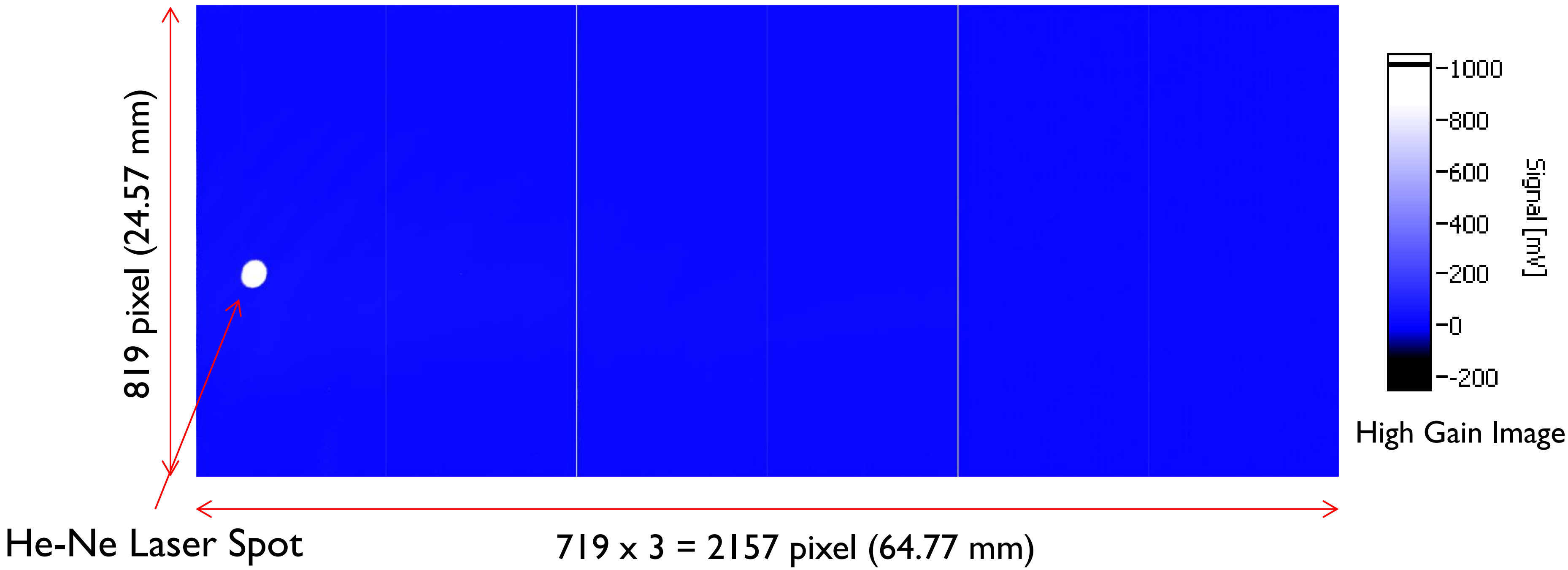


FWHM : 33 μm
Resistivity : ～7 kohm・cm
Depletion of 500 μm with 120V bias

1 pixel = 30 um
Cu Ka irradiation 40 kV 300 uA

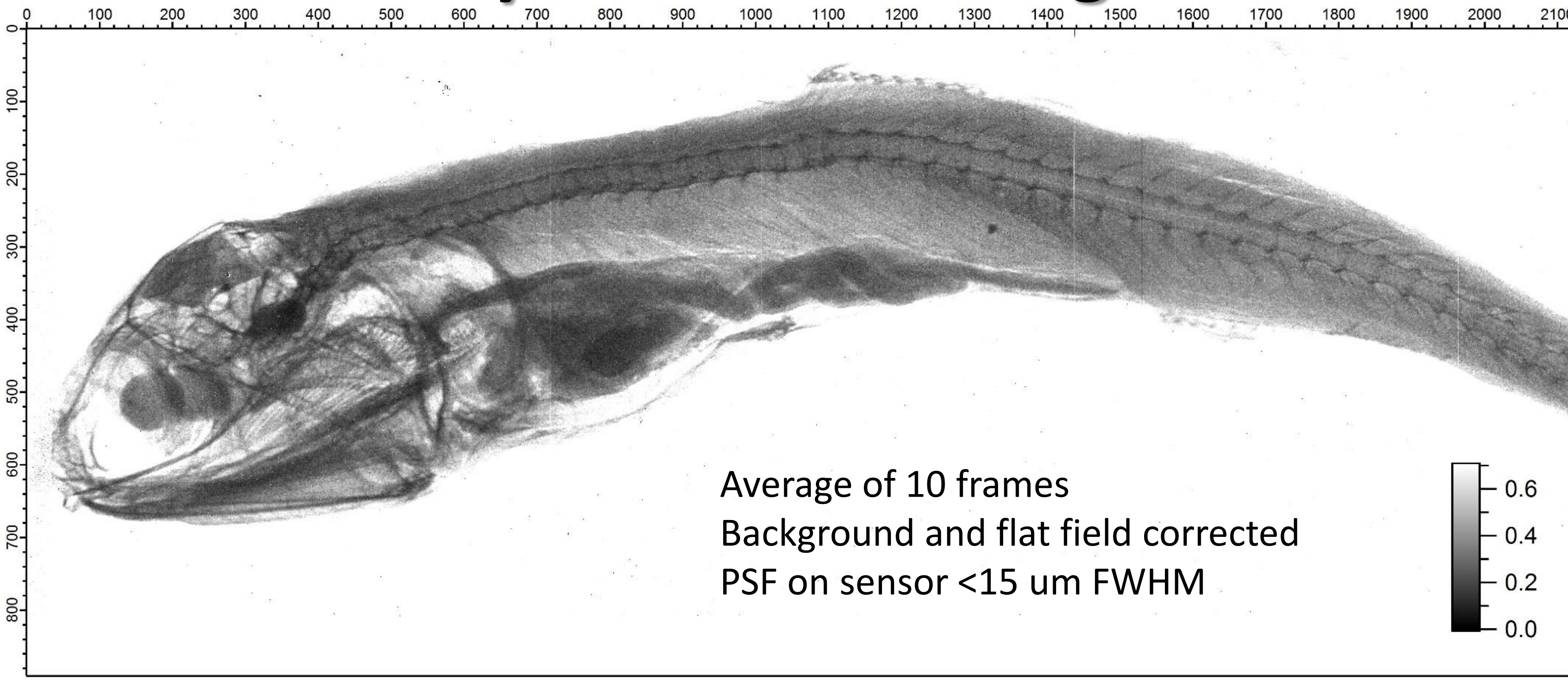
RIKEN SOPHIAS chip

High Reliability in Production



For good chips, defect that do not respond to light: 0 pixel out of 5 chips (9. 5 Mpixels)

X-ray Transmission Image

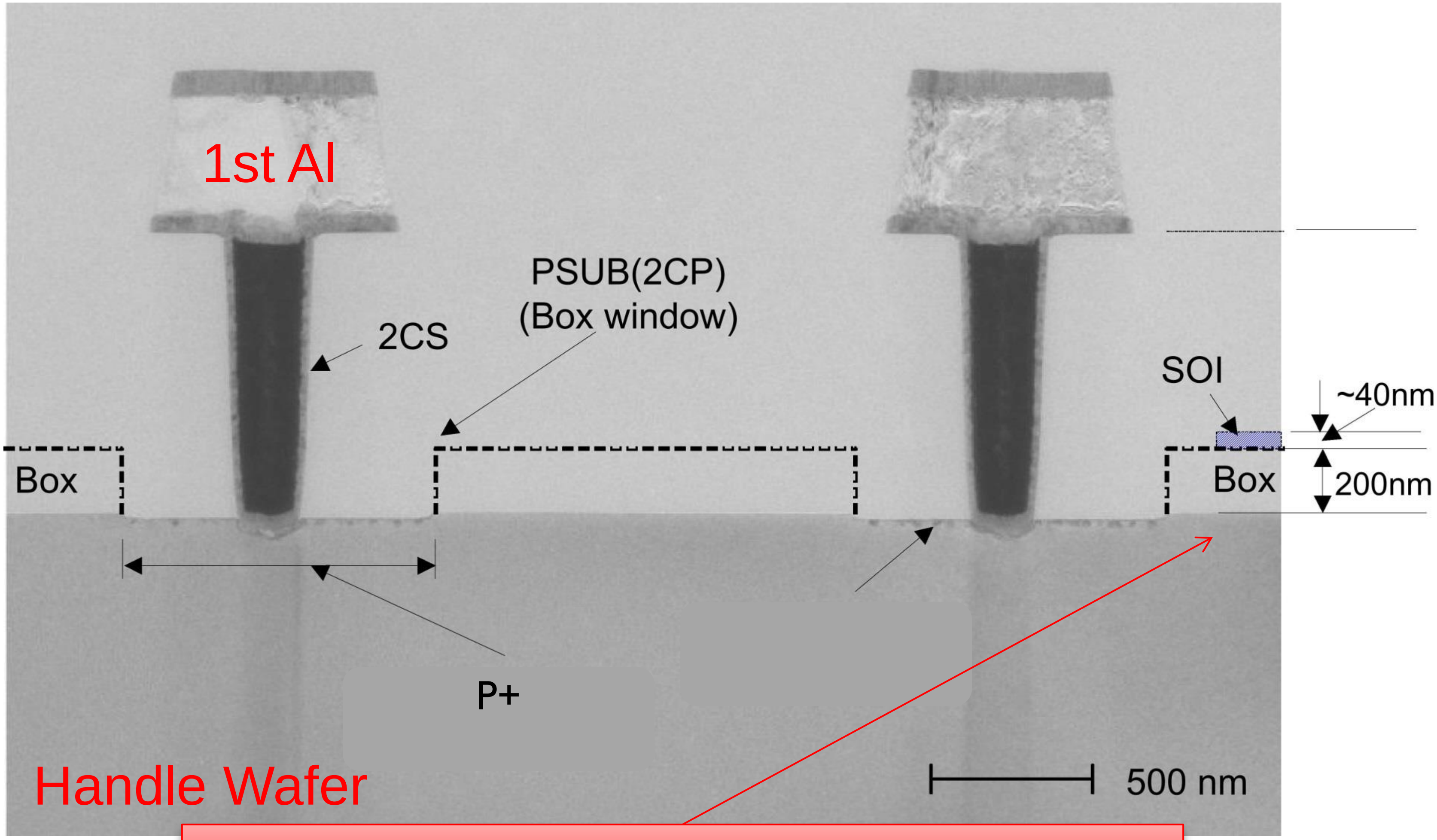


Source-sample	:	200 mm
detector-sample	:	600 mm
X-ray	:	40 kV, 800 uA
Cu target		
X-ray source size	:	～3 um
Exposure time	:	10 msec
Temperature	:	Room Temp.

Features of SOI Pixel Detector Process

- No mechanical bonding.
- Fabricated with standard semiconductor process only, High reliability demonstrated. Low cost expected.
- Fully depleted thick *pn* diode demonstrated. (500 um)
- Low input capacitance.
- Can be operated in wide temperature (4K-570K) range
- Low single event cross section.
- On Sensor processing with CMOS transistors.
- In-pixel processing with CMOS transistors.

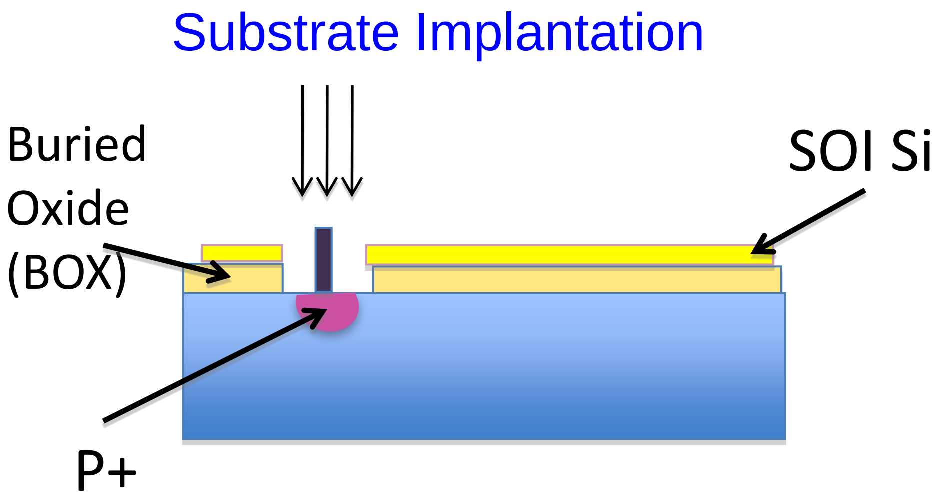
Connection Between *pn* diode and CMOS

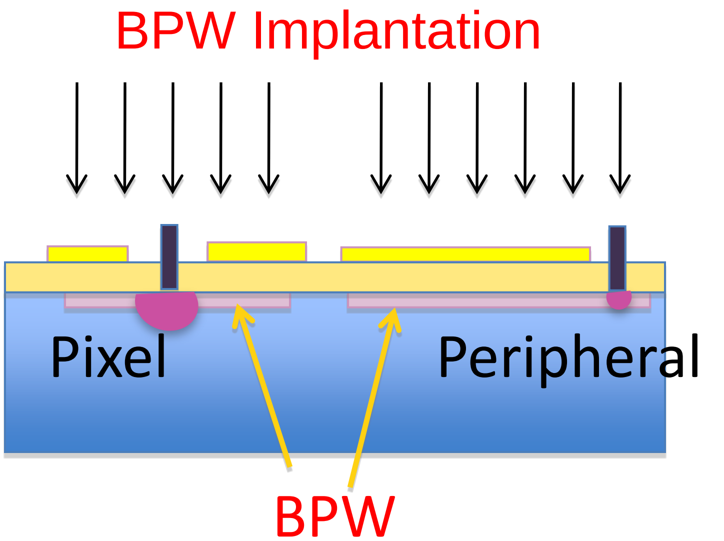


Voltage increase/decrease by biasing

Buried p-Well (BPW)

KEK & Lapis





- Cut Top Si and BOX
- High Dose

- Keep Top Si not affected
- Low Dose

- Suppress the **Back Gate Effect**.
- Periphery circuit
  - All issues are solved
- In-pixel use
  - Increase input capacitance
  - Cross-talk remains

Features of SOI Pixel Detector Process

- No mechanical bonding.
- Standard semiconductor process
  →High reliability demonstrated. Low cost expected.
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- Low input capacitance.
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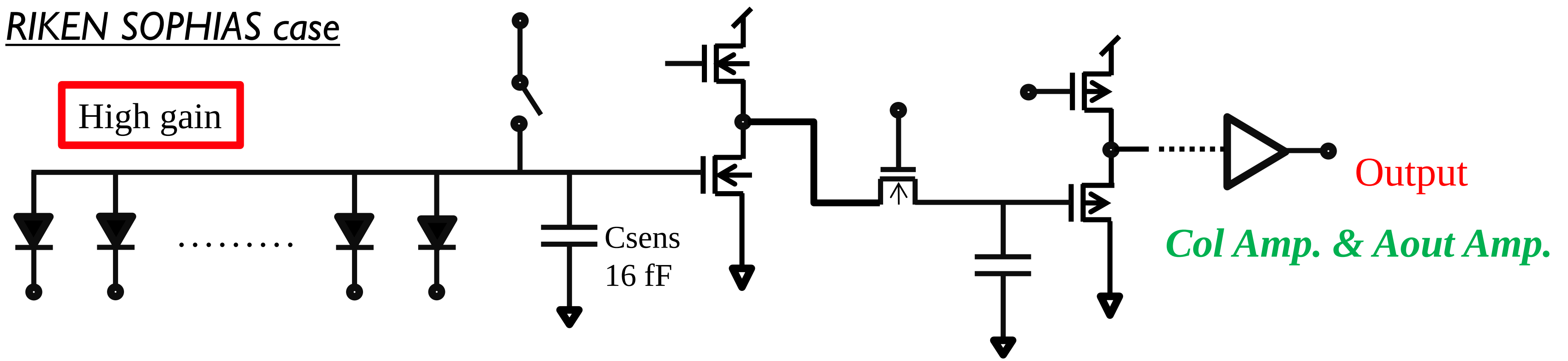
In-pixel Processing



Functionality

- Non-destructive Reading
- Correlated Double Sampling (CDS)

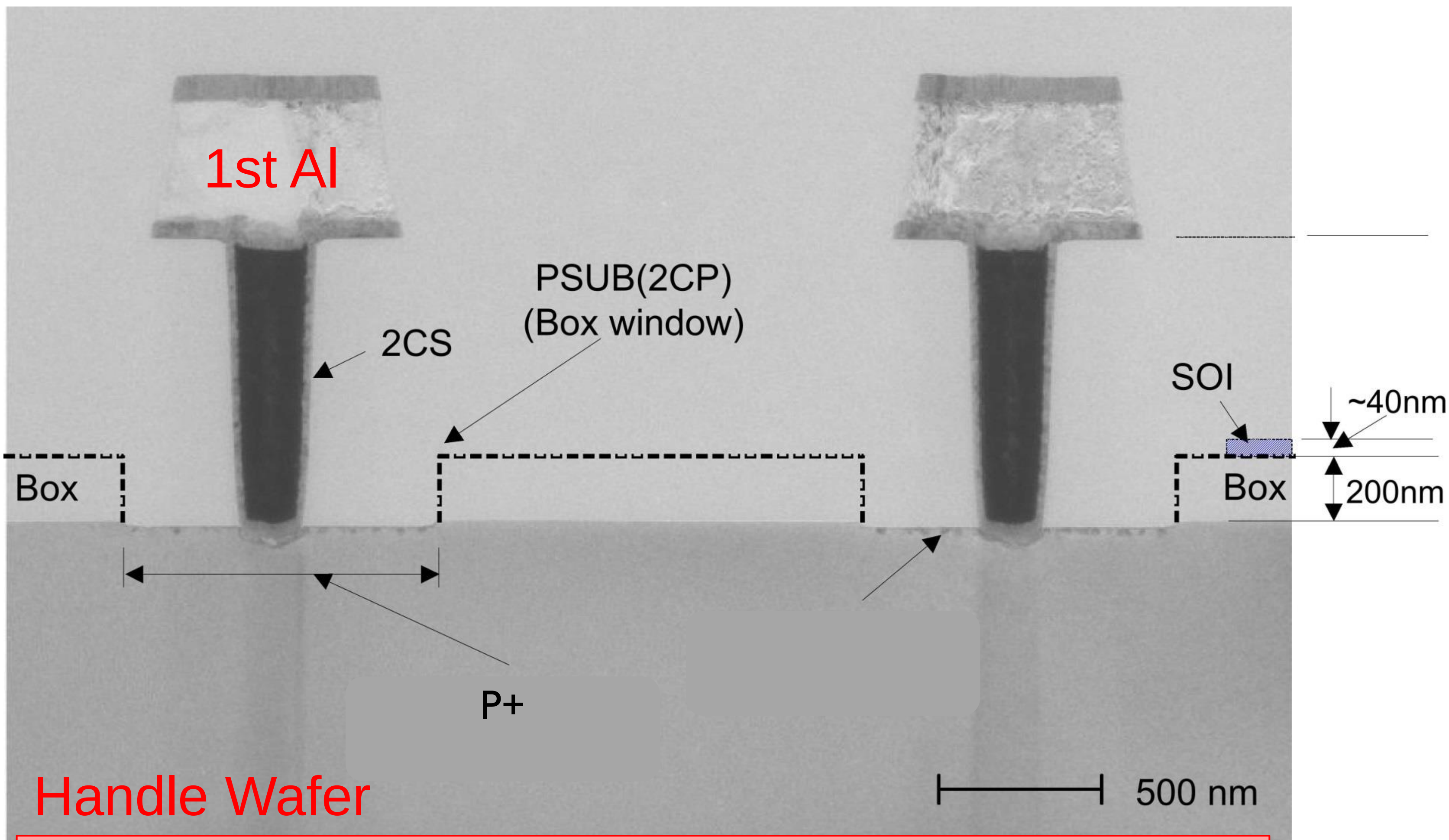
Easy to implement

- Read while exposure
- Pixel/column Correlated Double Sampling (CDS)

R&D Phase

- Complex logic (Counter etc.)

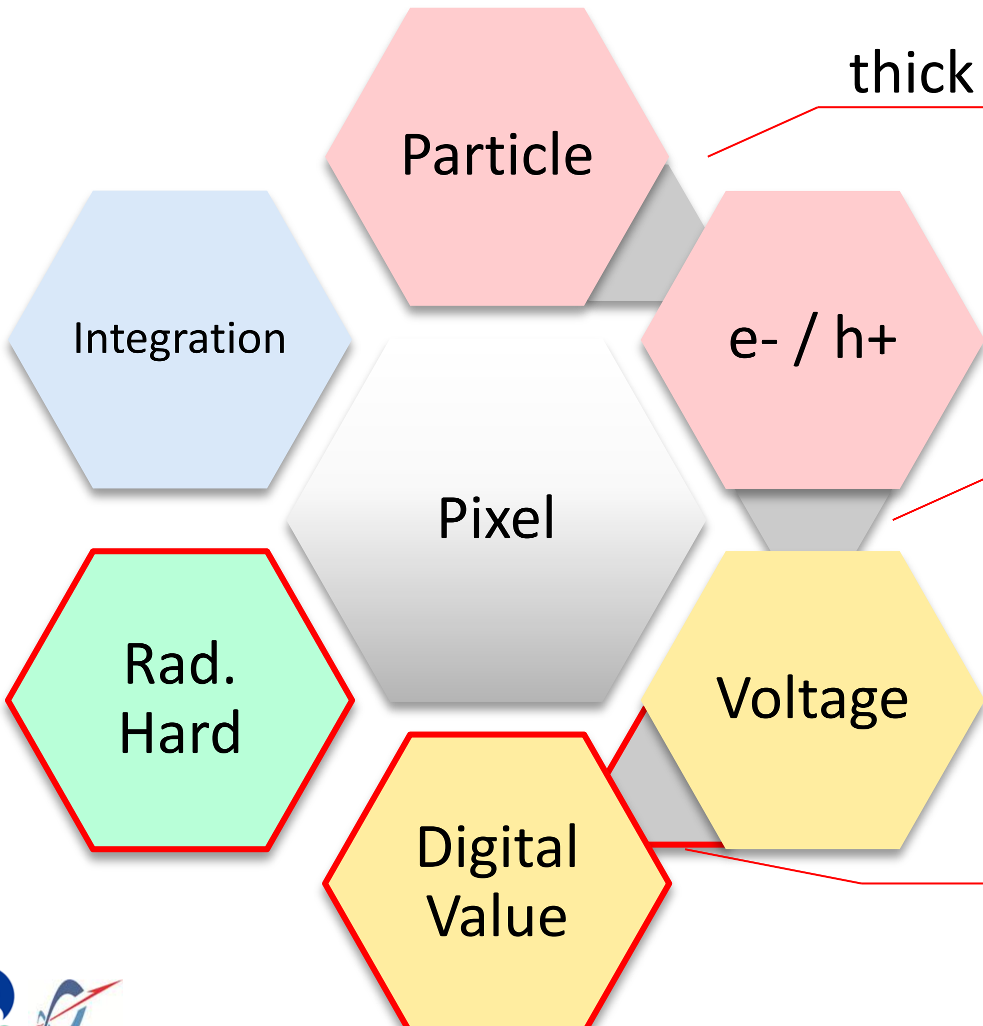
Connection Between *pn* diode and CMOS



Capacitive coupling between diode and CMOS

SOI Pixel Sensor: Current Achievement

In Realization



thick pn diode 50-500 um

MOS analog circuit
with <u>small input capacitance</u>

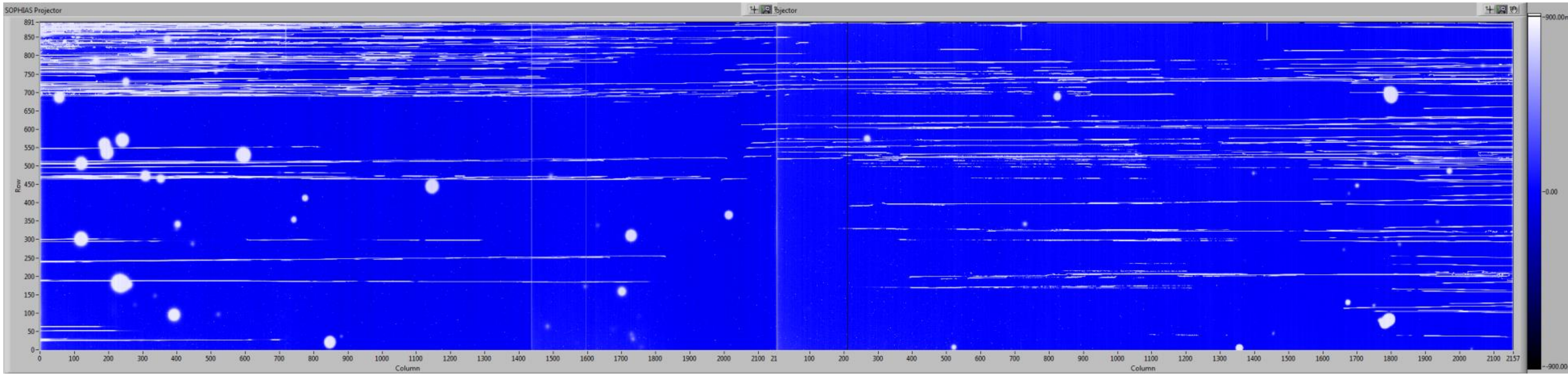
CMOS analog/digital circuit

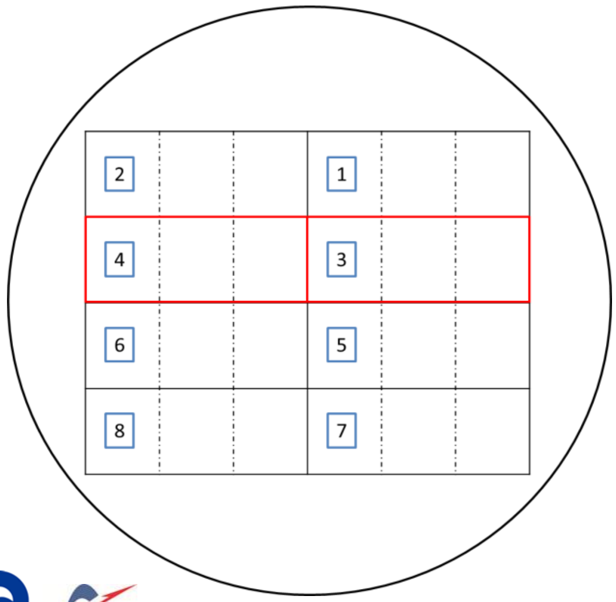
Remaining Issues for SOPHIAS

- Cosmetic Quality
- RTS Noise
- Charge Collection Efficiency
- Yield (VDD-GND leakage)

Cosmetic Quality

L6-W2-4 L6-W2-3

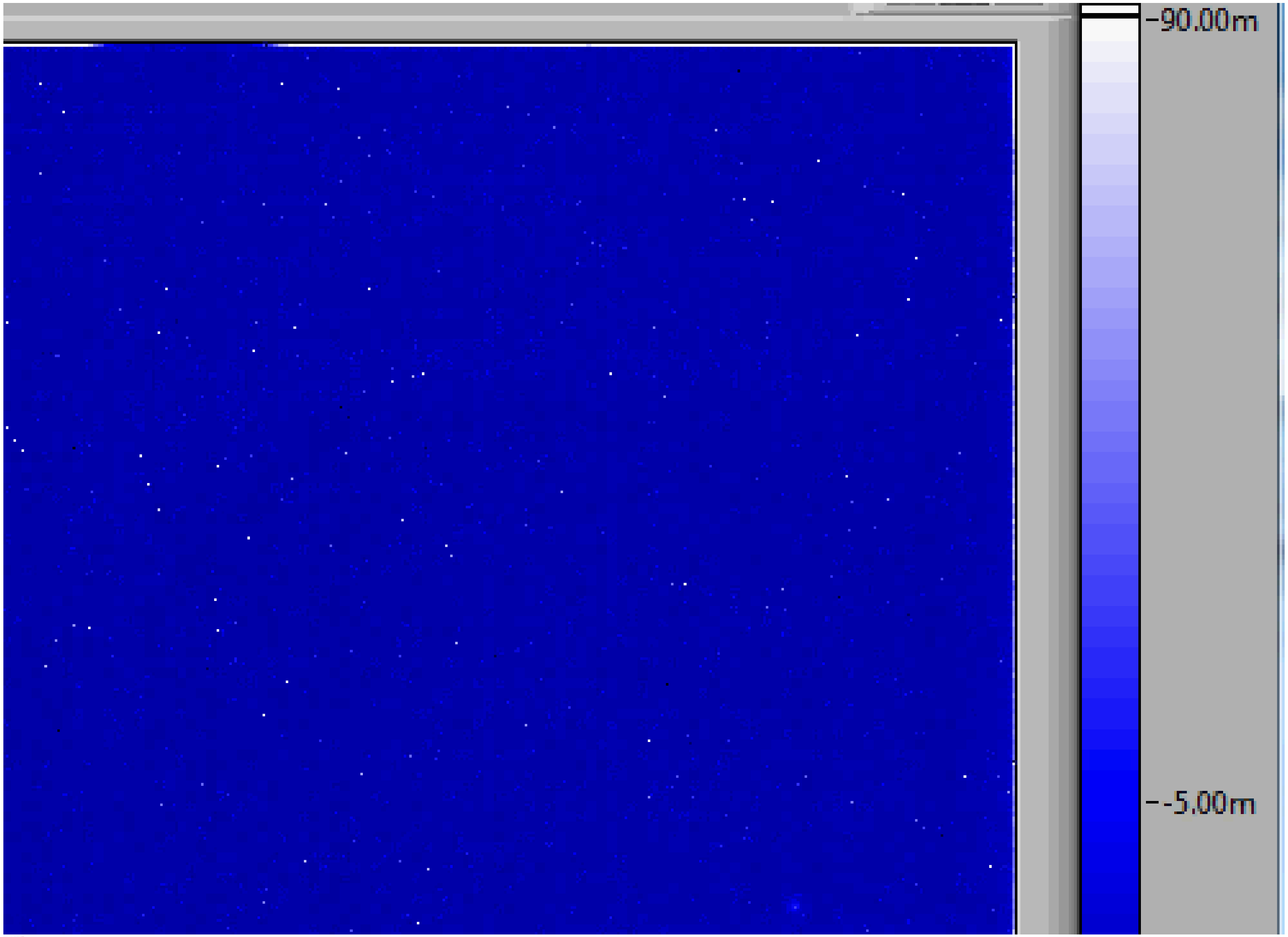




- 3 Types of Defects
  - Horizontal White Defects
    - Implant Induced Damage
    - Insufficient Annealing
  - White Spots
    - Aluminum Coating Defects
  - Round Shape leakage Pattern
    - Source not yet identified

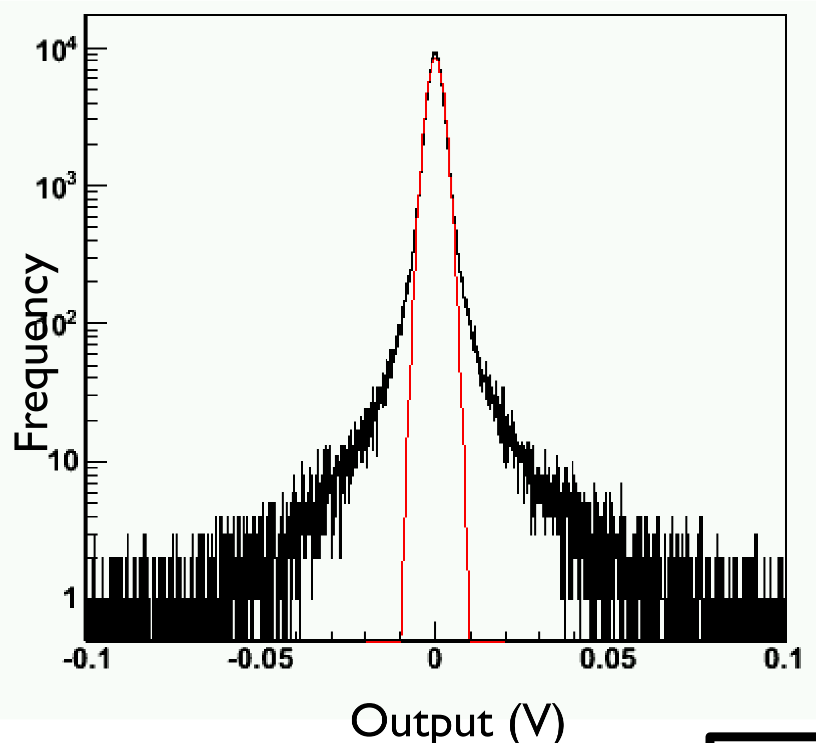
Blinker Pixels/Columns

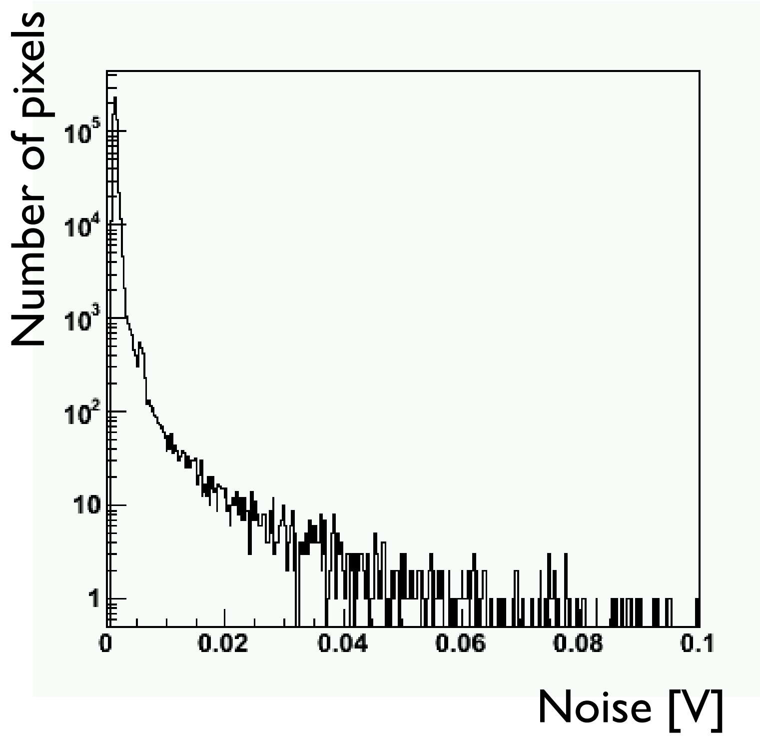
Background Subtracted Image without Correlated Double Sampling



Bad Pixel with High Noise

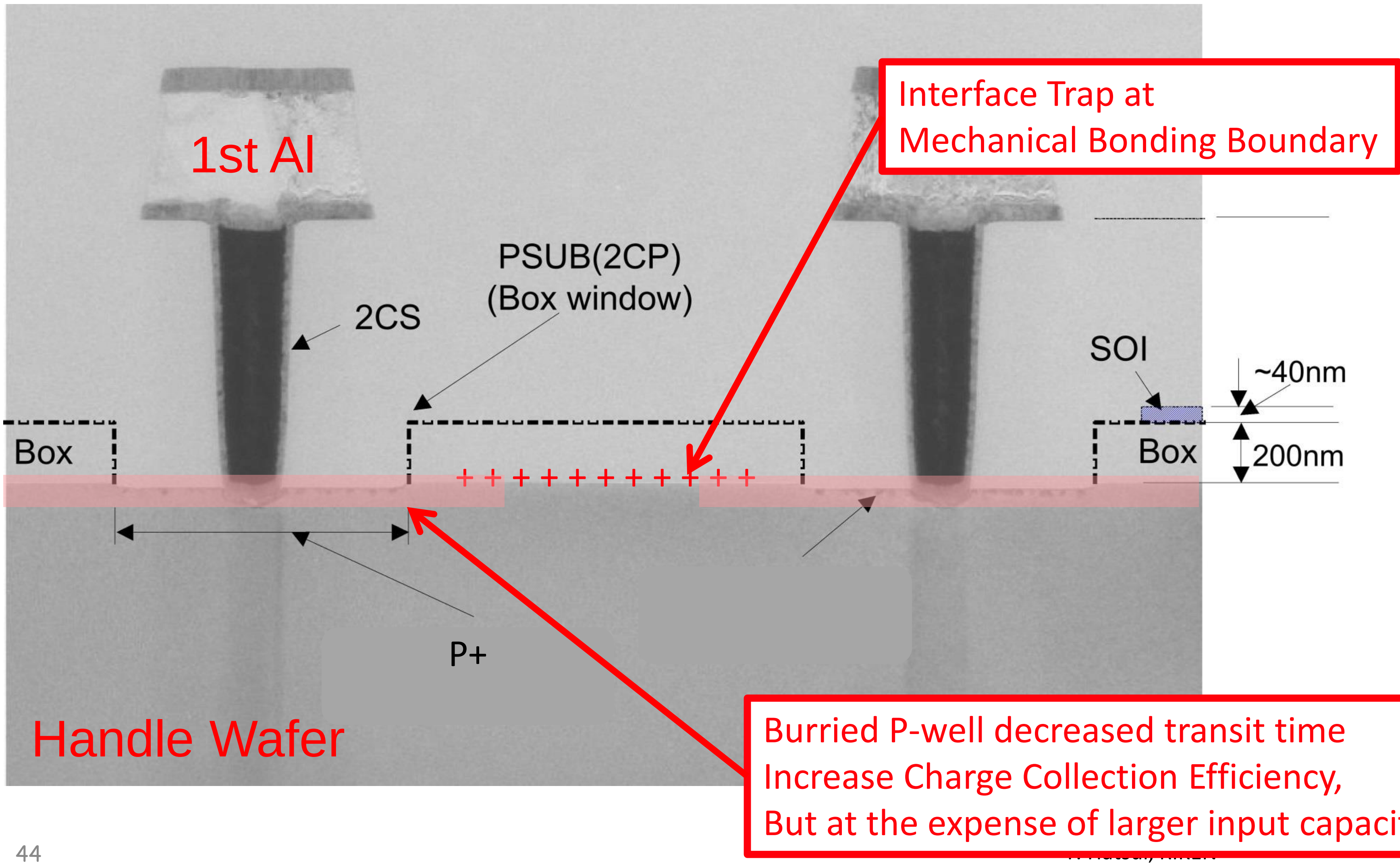
RIKEN SOPHIAS



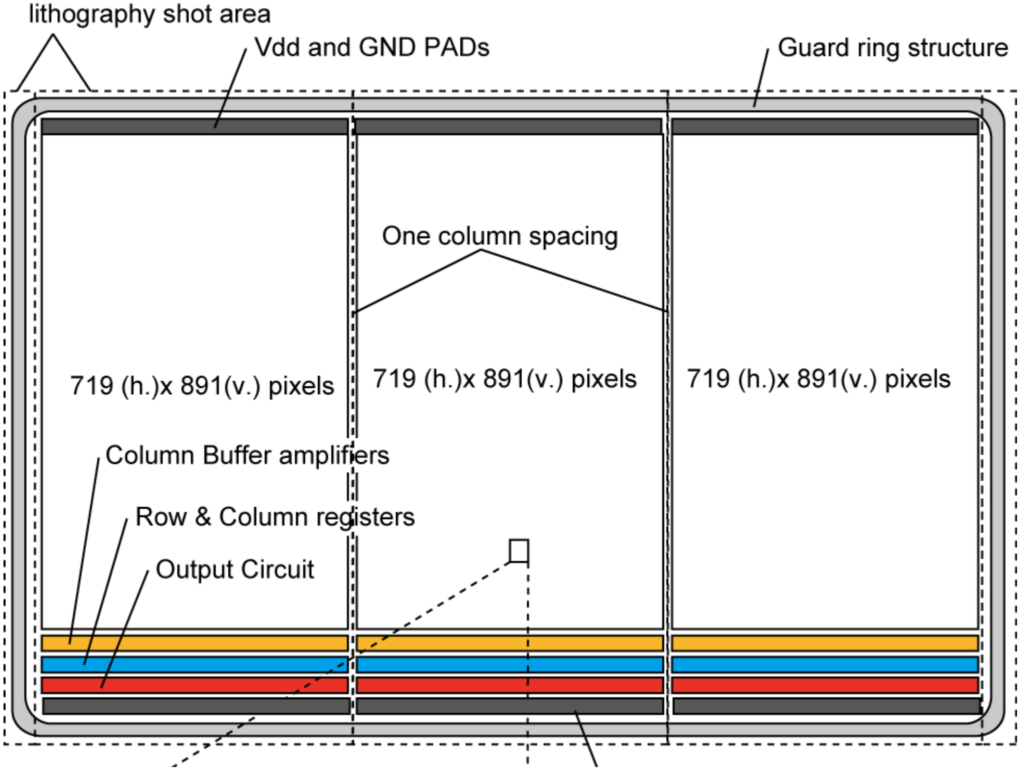


- Non-Johnson noise distribution.
- Radom Telegraph noise is very large when transistor are under backgate effect.

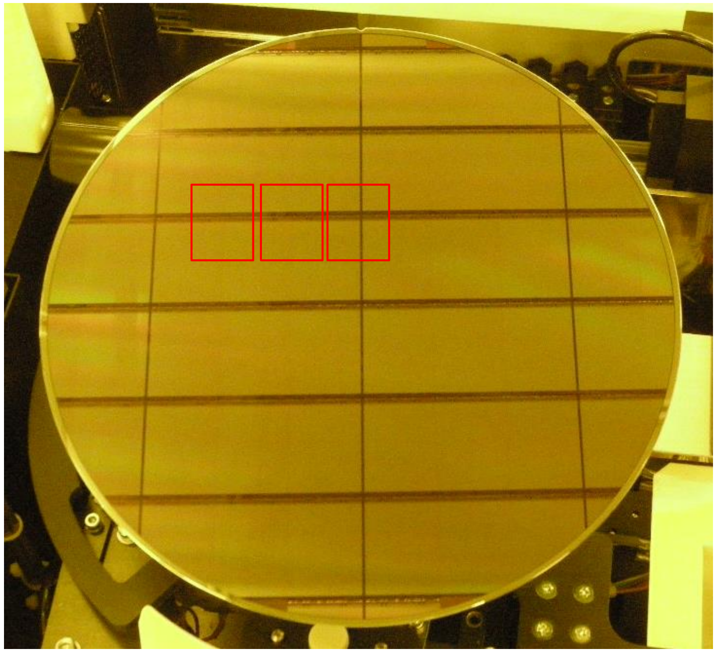
Charge Collection Efficiency



Analog VDD-GND Leakage



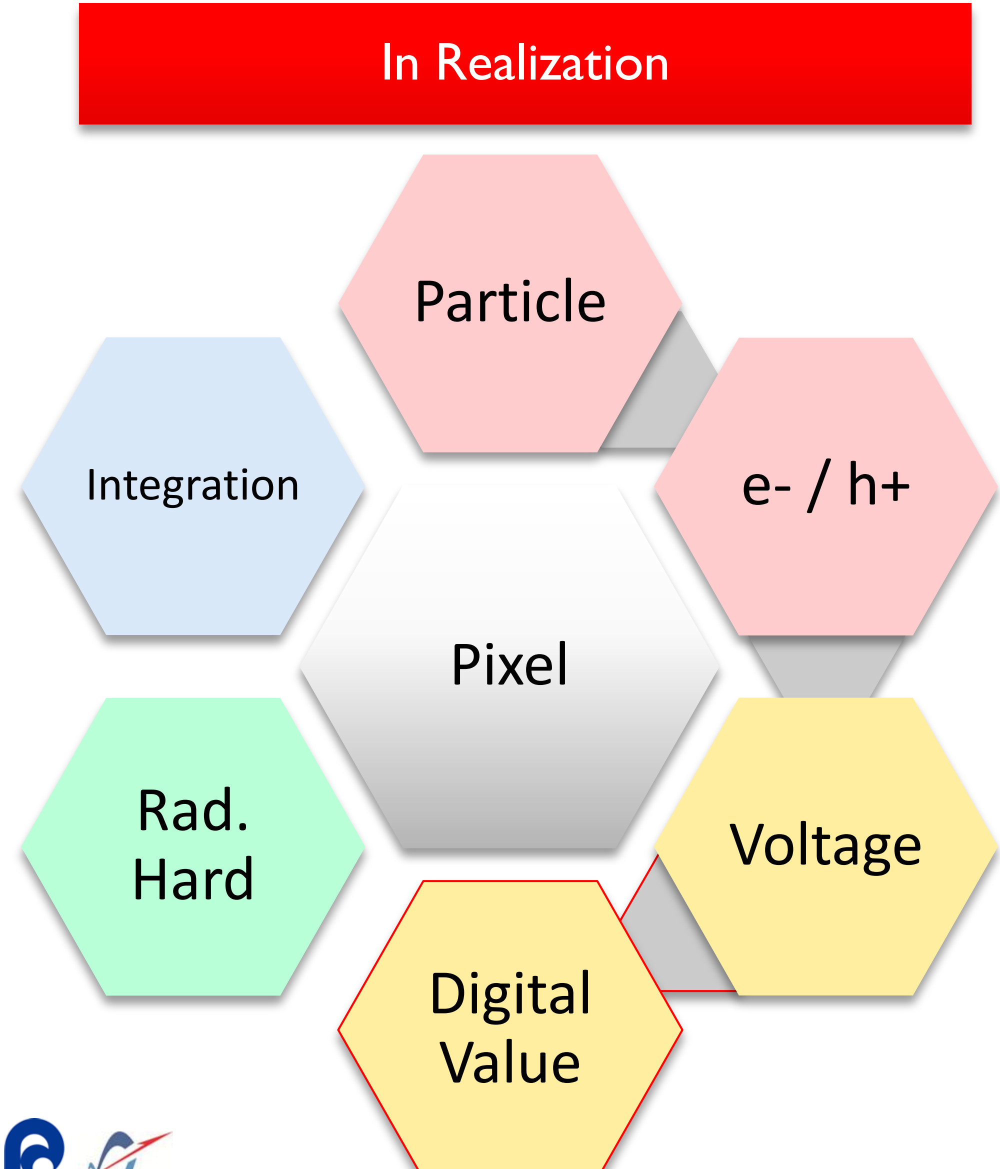
Stitching is done only for the Guard Ring:



Min. 24 Test Results/Wafer

Comparison with other state-of-art Sensors

How to connect thick pn diode and CMOS?



CCDs

from MPCCD for SACLA

LBNL (DALSA)
Hamamatsu
e2v

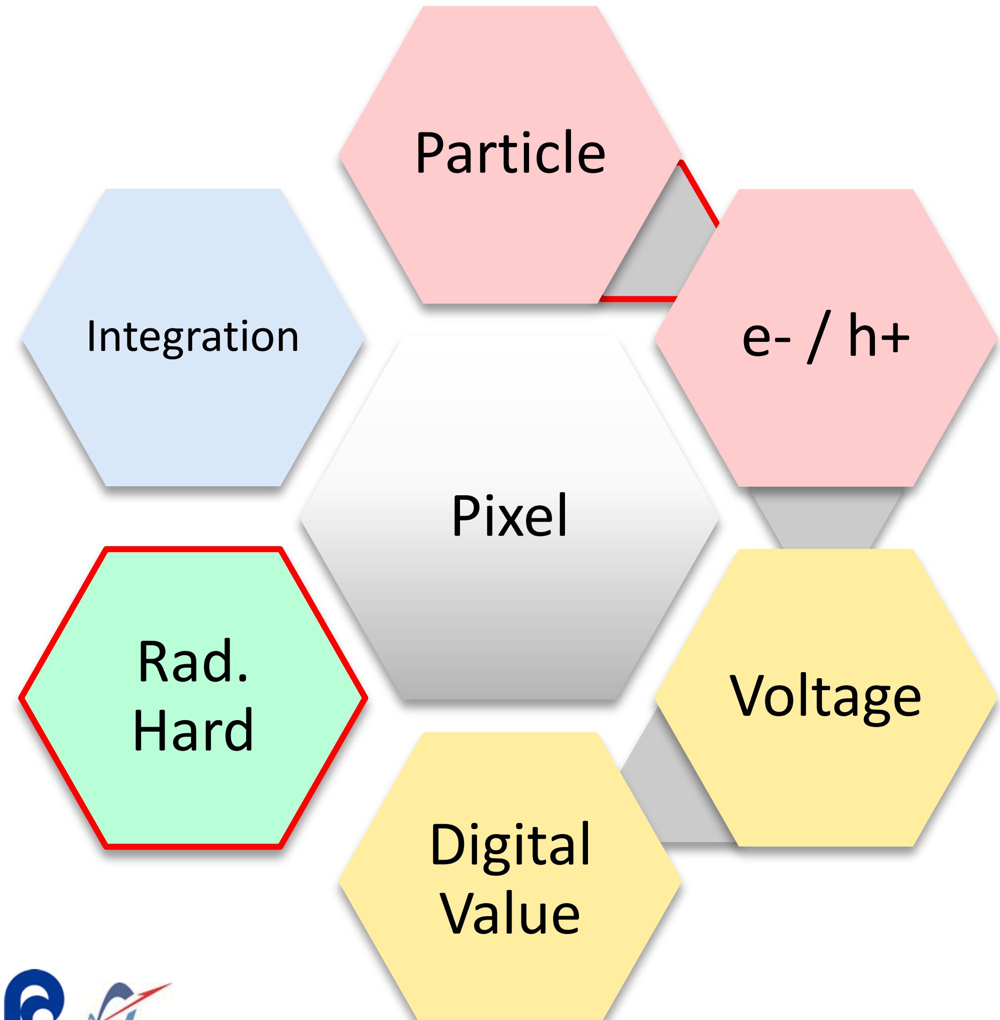
Thick CCDs ～ 500 μm

Many applications.

- Functionality on off-sensor board

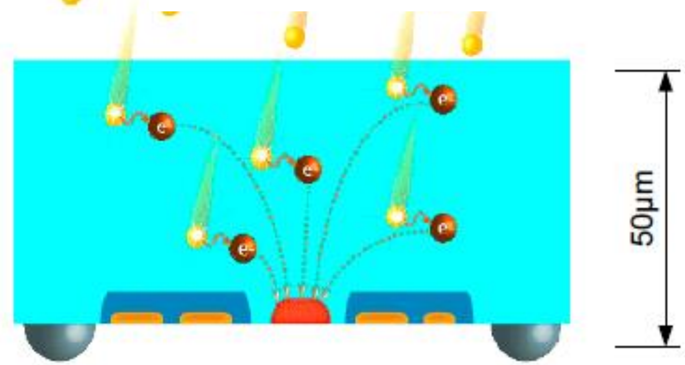
How to connect thick pn diode and CMOS?

In Realization



CMOS Imagers

Back-side CMOS sensor



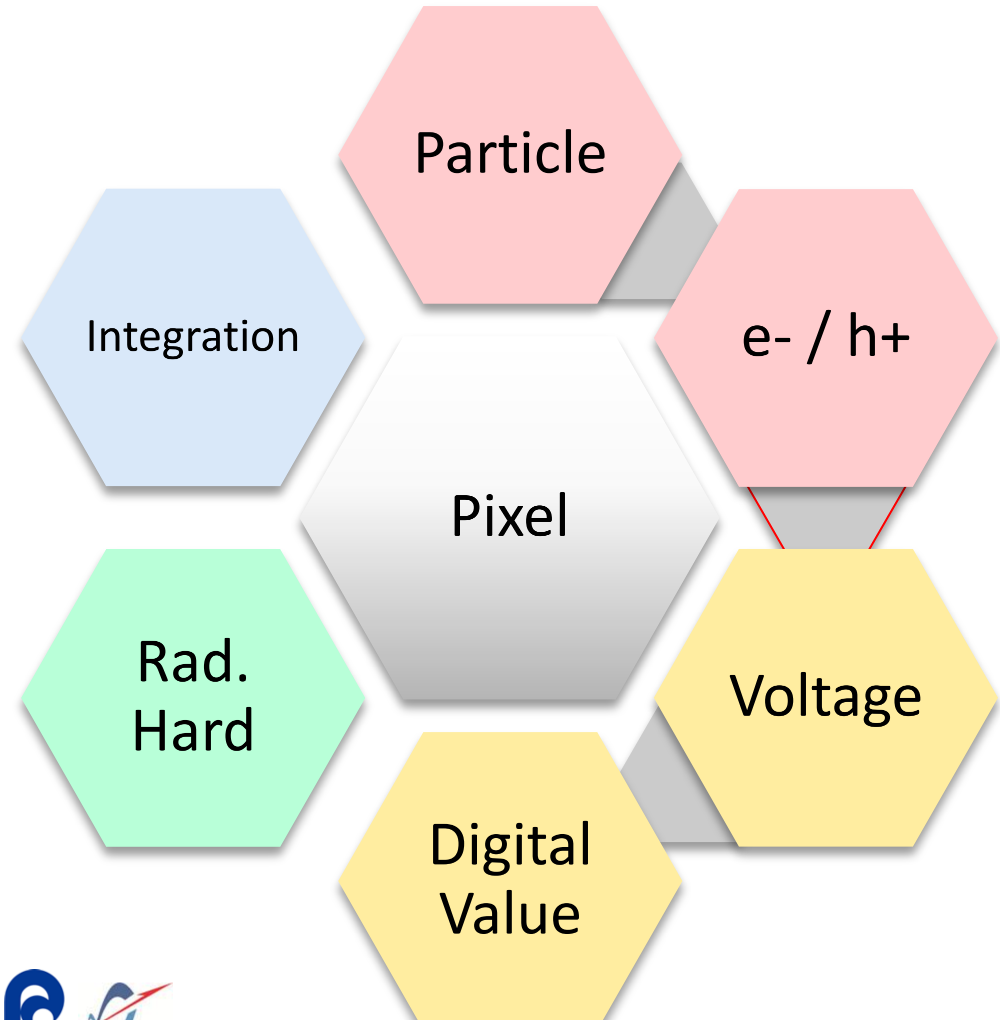
ESPROS Photonic CMOS™

Many consumer/industry applications. Many variants but generally

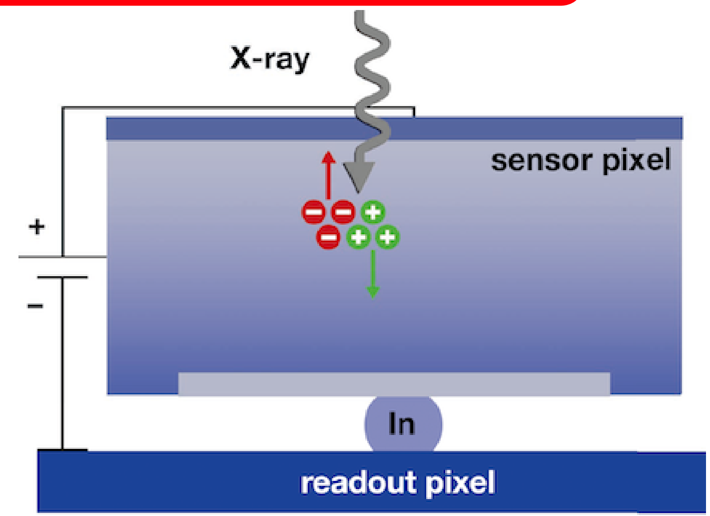
- Thin pn photodiode
- Rad. Hard not proven

How to combine thick pn diode and CMOS?

In Realization



Hybrid Sensor



from https://www.dectris.com/

Many scientific applications
Large input capacitance gives
- Higher Noise floor
- Slow Analog Amplifier

Current Status

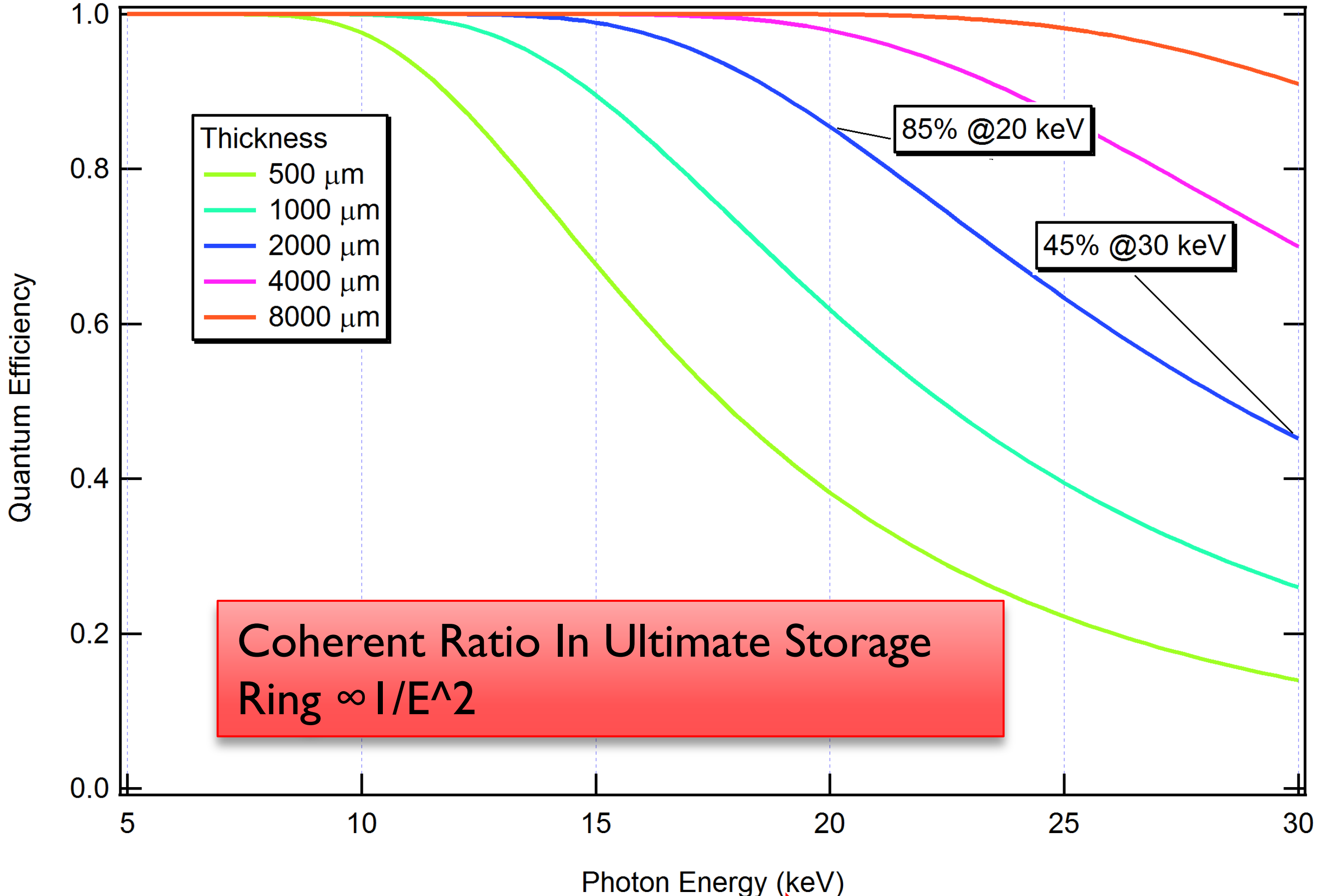
- SOI Pixel Sensor process
  - Process improvements gives reliable performance in many applications.
  - Now it can be deployed for applications with
    - Integration pixel
    - TID < 100 krad on Transistors
  - SOPHIAS for SACLA
    - In-house testing campaign: Fall 2014
      - Cosmetic Quality
      - RTS Noise
      - Charge Collection Efficiency
      - Yield (VDD−GND leakage)

Toward Next Step of SOI Pixel Sensor Technology

New Era of Photon Science

- Coherent X-ray
  - X-ray Free-Electron Laser
  - Ultimate Storage Ring

Si Technology: The High Photon Energy Limit



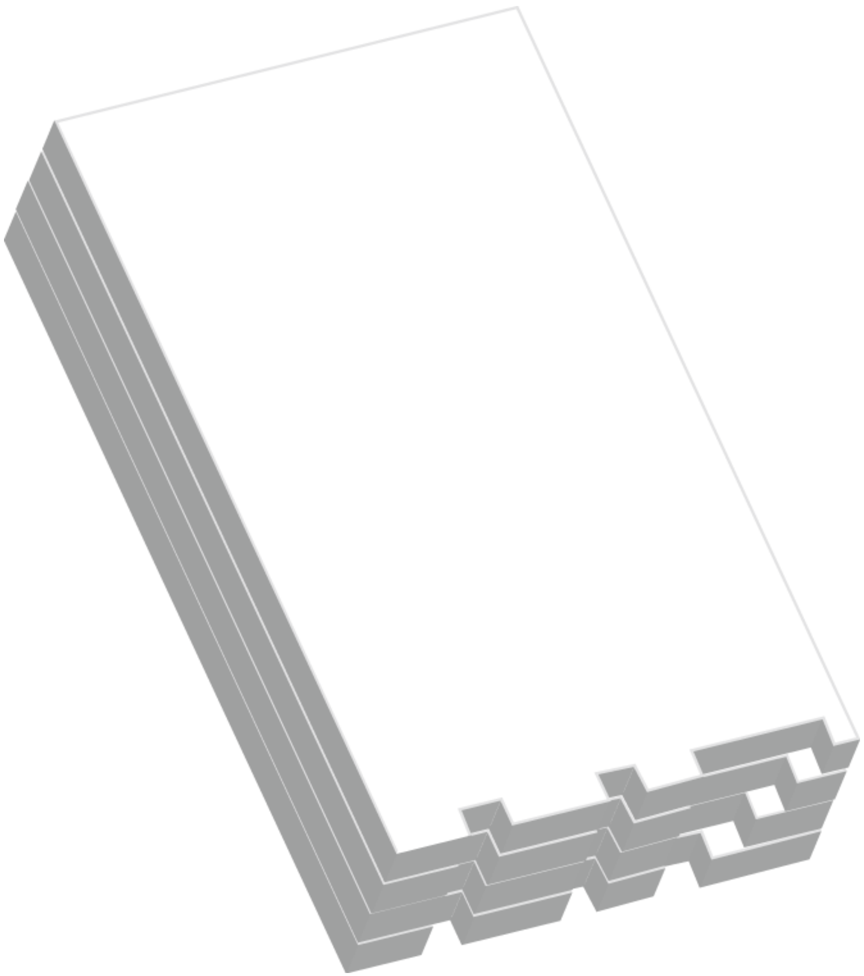
Very Important → Important

What is the challenge in Very Thick Silicon Detector?

Stacked Sensor

- PSF does not degrade because each layer collect signal charge
- Methods
  - Chip with different laser dicing.
  - Wire-bonding to pads on stepped regions
  - TSVs

- CON: Smaller number of pads available for each sensor
- CON: Radiation Hardness



1st Target: 4 Layer Stacked 2 mm Sensor

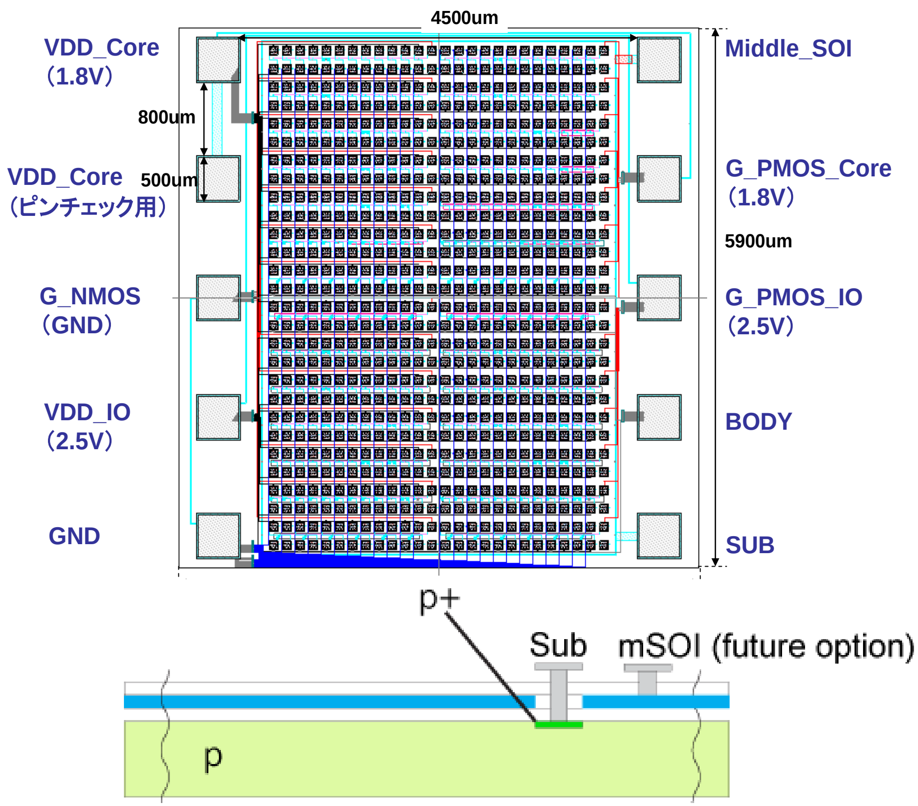
Target TID hardness for Photon Science

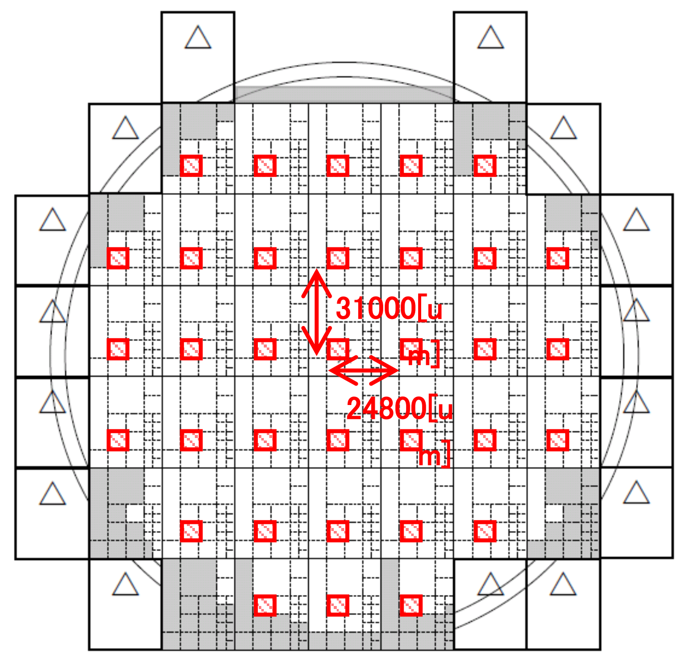
- **<u>Over 100 Mrad</u>** as system is mandatory to compete with other technology, such as hybrid sensors.
  - c.f.) 100 Grad tolerance is European XFEL target.

- Our Goal of TID study
  - **<u>Critical review</u>** of the current SOI devices and sort out possible options by simulation.
  - **<u>BOX implantation of Si</u>** will also be investigated.
  - Study of Double SOI is also examined from this perspective.
- Schedule
  - Report will be issued by Summer 2013
    - Due to issues, it will be delayed to Dec. 2013
  - Milestone: April 2014
    - Internal Go/No Go decision in RIKEN

RadTEG

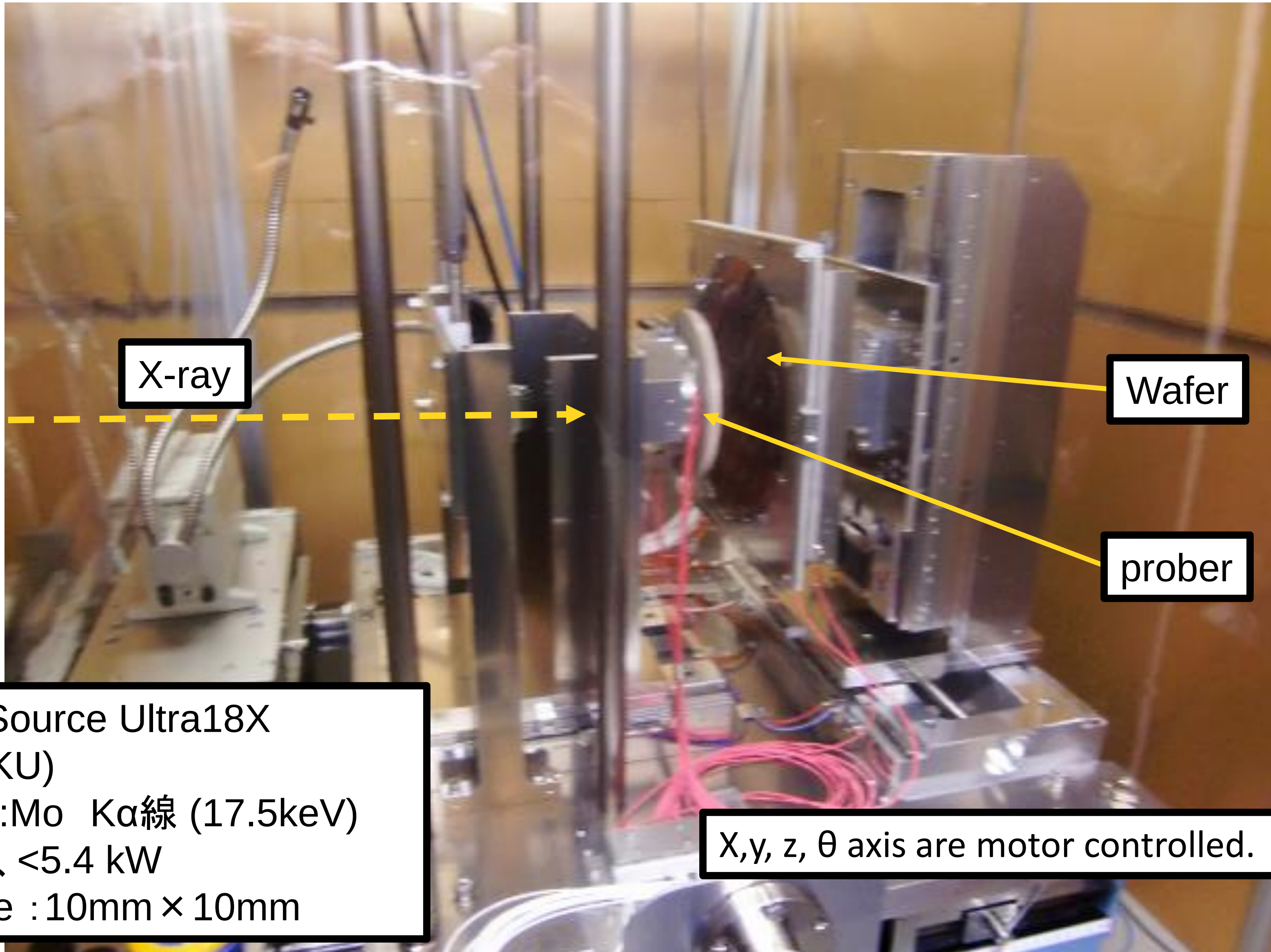
Radiation by Semi-automatic probe-station → Fuse disconnection → Automatic Probing for DC characteristics → Semi-automatic Probing for noise measurement





Semi-automatic Probe-station for TID Study

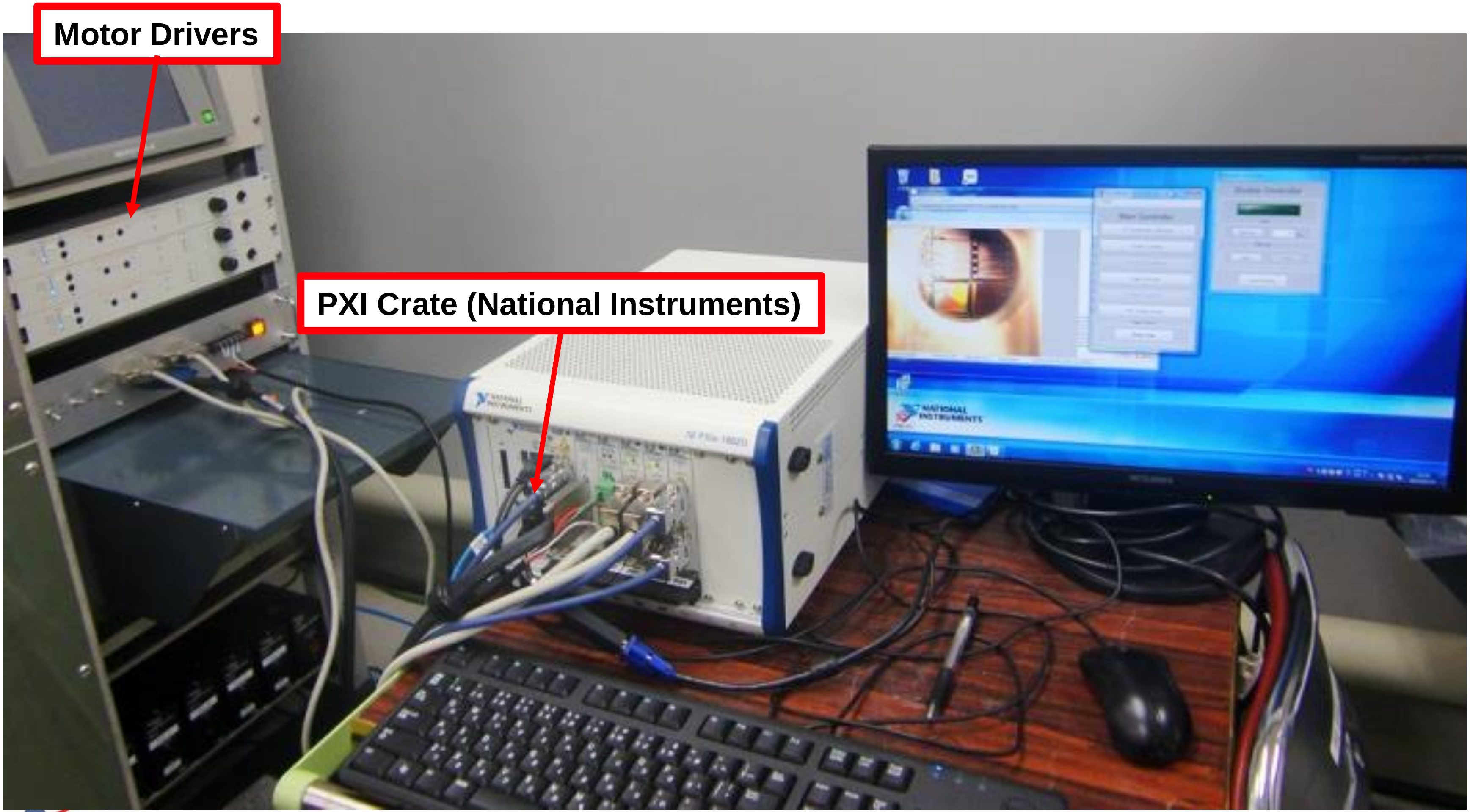
Designed by Hyogo Univ. Developed by Hyogo Univ. and RIKEN.



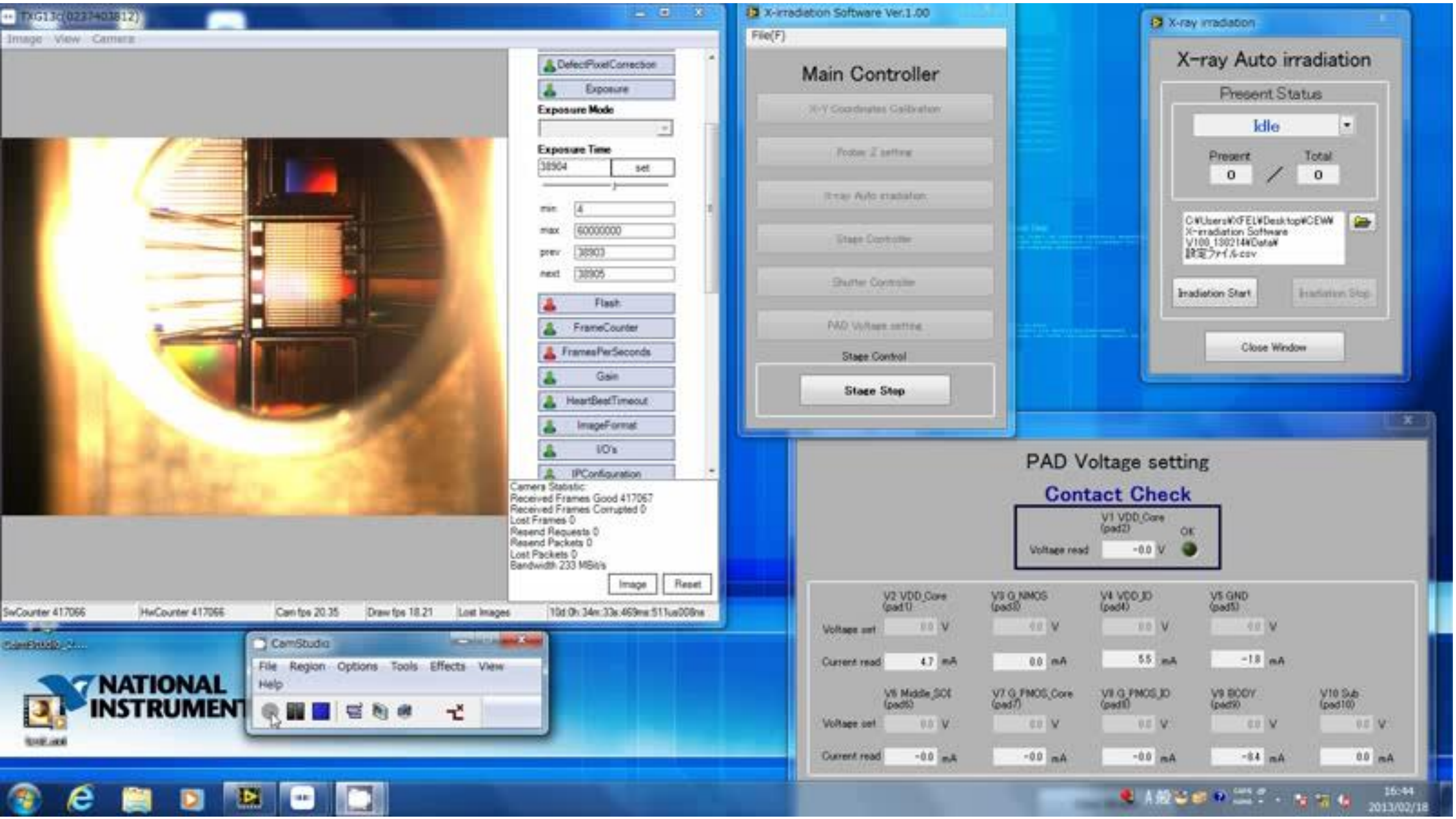
X-ray Source Ultra18X (RIGAKU)
Target :Mo Kα線 (17.5keV)
<60kV、<5.4 kW
Slit size :10mm×10mm

X,y, z, θ axis are motor controlled.

Semi-automatic Probe-station for TID Study: Control



Semi-automatic Probe-station for TID Study: Operation



T. Hatsui, RIKEN

Radiation by Semi-automatic probe-station → Fuse disconnection → Automatic Probing for DC characteristics → Semi-automatic Probing for noise measurement

- **Automatic Prober at Lapis**
  - IV curves
    - 1 week for one wafer with different operation conditions.

Semi-automatic prober for 1/f noise at RIKEN

- Performance
  - -120dBV^2/Hz@1Hz
  - -140dBV^2/Hz@10Hz
  - -160dBV^2/Hz@1KHz
  - -170dBV^2/Hz@100KHz
- Typical Measuring time
  - 1 min for one device.
- Instrument Components
  - Prober
    - SUMMIT 12000B-AP, *or equivalent*
  - Device Analyzer
    - Agilent B1500A *or equivalent*
  - 10 MHz to 7 GHz Signal Source Analyzer
    - Agilent E5052B, *or equivalent*
  - 1/f Noise measurement System
    - Agilent E4725A, *or equivalent*

Rad. Hard SOI Pixel Sensor Process

- Current FD-SOI and its extension (incl. Double SOI) is not proven for High TID applications > 100 Mrad.

  and, simultaneously
  - ***Small Input Capacitance***
  - ***Small Cross Talk***

Current FD-SOI Tr under 1 Mrad regime is just like trees In typhoon

- Systematic Radiation and Testing Tools are under developments.
  - RadTEG
    - Evaluation of current Transistors
    - Test bench for Quantitative Analysis with Simulation
  - Semi-automatic Probing station for radiaiton
  - Automatic Prober for RadTEG at Lapis
    - DC characteristics
  - Semi-automatic prober for 1/f noise at RIKEN

- For these applications, extensive discussion on possible options is mandatory.
  - We welcome your inputs.

Investment on Semiconductor Process

- Wafer Process
- Advanced Post Processing
- Packaging
- ASIC design
- Readout Circuit
- Digital Data handling
- FPGA control logics
- Mechanics
- Software

Long Term Development
Long Turn-over time

Risk in Discontinuity

Closely Connected to
Experimental Design
Short turn-over time

Summary

- SOI Pixel Sensor process
  - Process improvements gives reliable performance in many applications.
  - Now it can be deployed for applications with
    - Integration pixel
    - TID < 100 krad on Transistors
  - SOPHIAS for SACLA
    - In-house testing campaign: Fall 2014
- Toward Next Step
  - Transistor Upgrade
    - Radiation hardness
    - Small Input Capacitance
    - Small Cross Talk

Our Target

- Use minimum "feedback" for radiation hardness
  - Counter measure such as proposed double SOI is not favored in photon science, where
    - Radiation dose pattern not predictable
      - One Tr damaged, the adjacent Transistor is 0 rad
    - Reduction of the maintenance cost is high priority.
- Our target
  - To provide process options that meets
    - TID hard transistors without minimum counter measures.
  - Extensive process/device process simulations to be carried out so to minimize unwanted side effects.

Regular Multi-Project Wafer (MPW) run. (~twice/year)