

Towards sensors for the HL-LHC phase

A. Junkes

Research Techniques Seminar

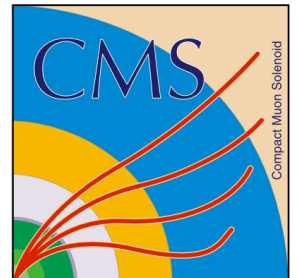
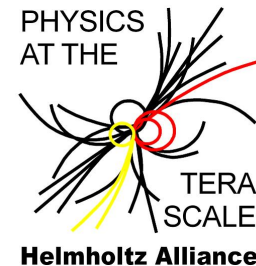
Fermilab

April 14th 2015

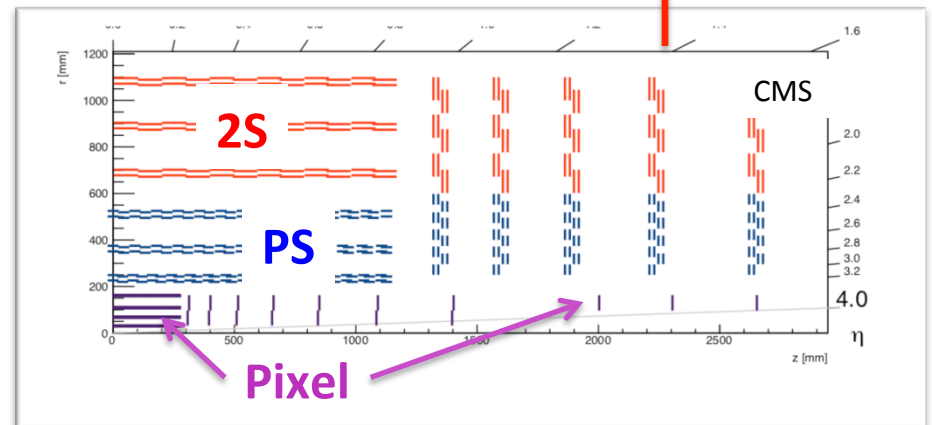
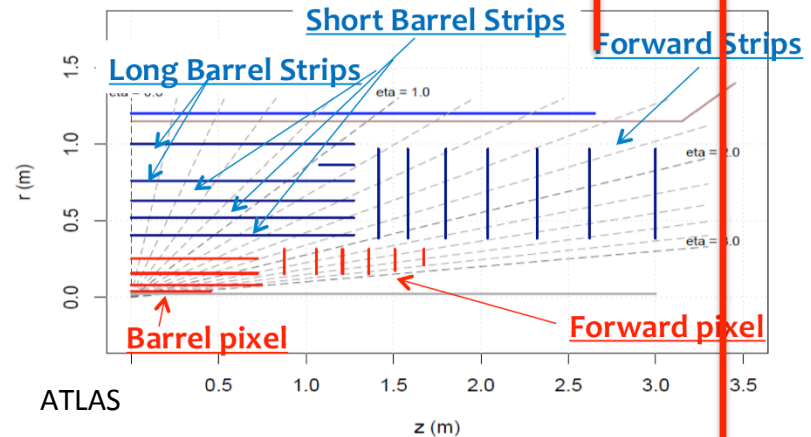
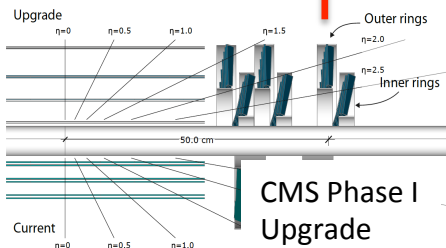
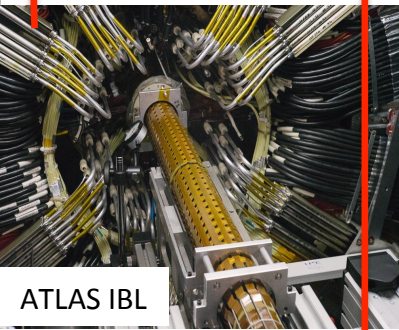
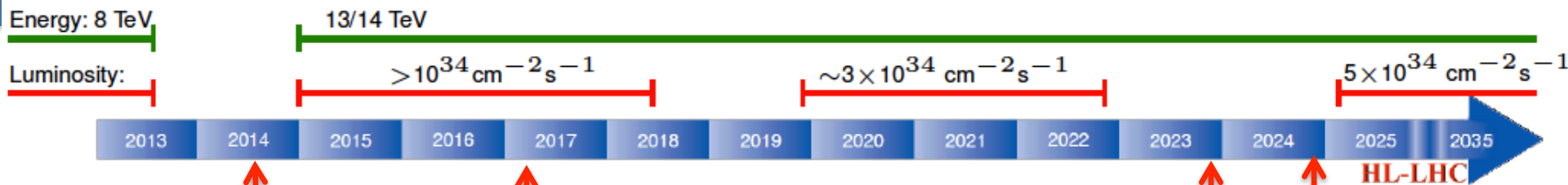


Universität Hamburg

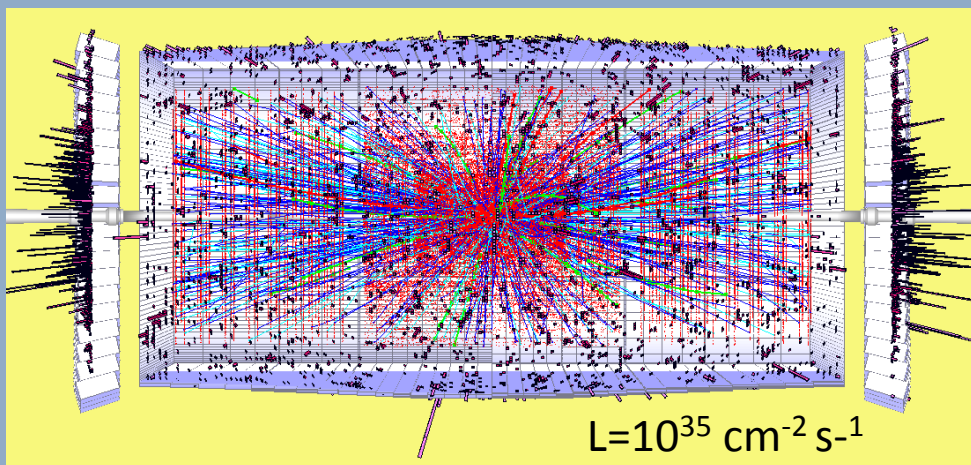
DER FORSCHUNG | DER LEHRE | DER BILDUNG



LHC timeline



High Luminosity LHC Challenges



Challenging environment for

- Precision tracking
- Primary and secondary vertex reconstruction

Requirements:

- Operate in 140 collisions per bunch crossing at $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$ and 40 MHz
 - Maintain occupancy at $\approx \%$ level
- More granularity and smaller pixel
- More radiation hard sensors

Reducing material in the tracking volume

- Improves performance at low p_T
- Reduce rates of nuclear interaction, γ conversions, bremsstrahlung...

Reducing the pixel size

- Improves performance at high p_T and two track separation

2022

2023

2024



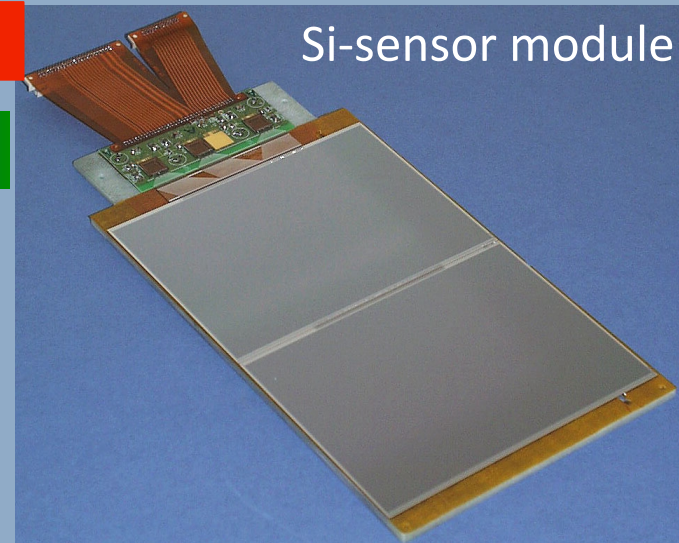
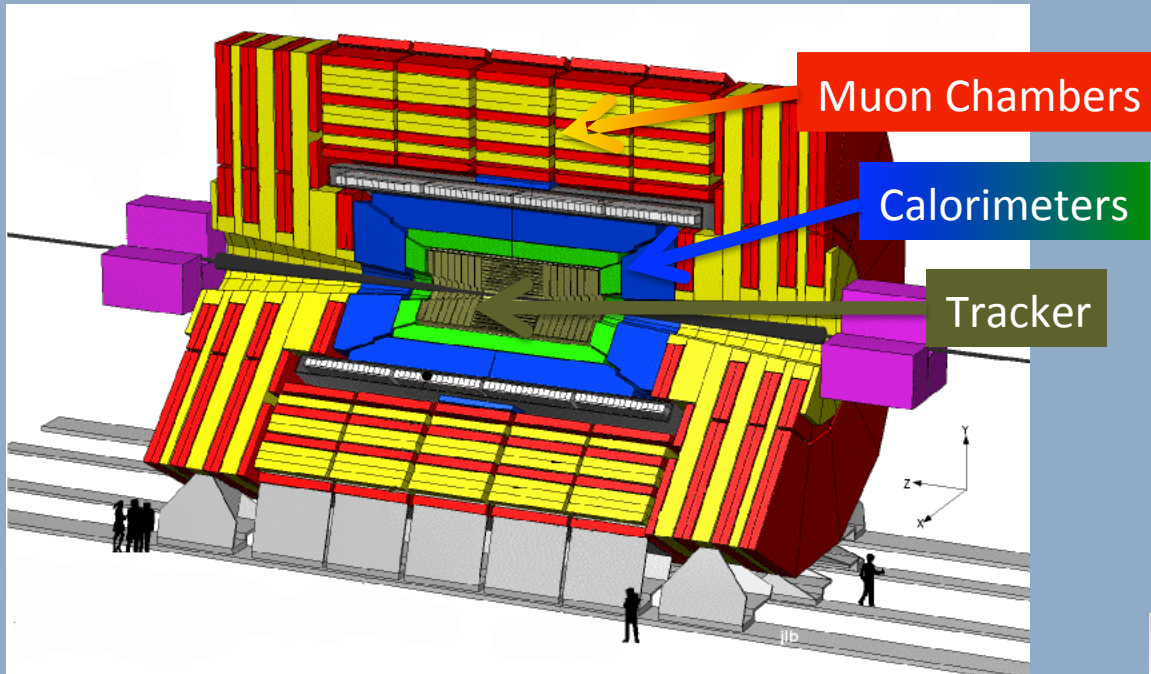
LS3

Data
taking
“phase II”

Installation of a
new CMS tracker

- Phase-2 pixel detector (Pixel)
- Phase-2 outer tracker (OT)
- Level 1 Track trigger

The CMS experiment



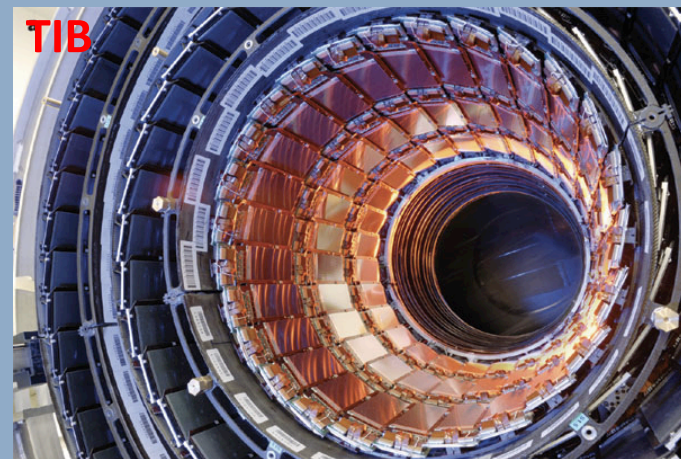
Tracking very important for physics programme

Micro Strip

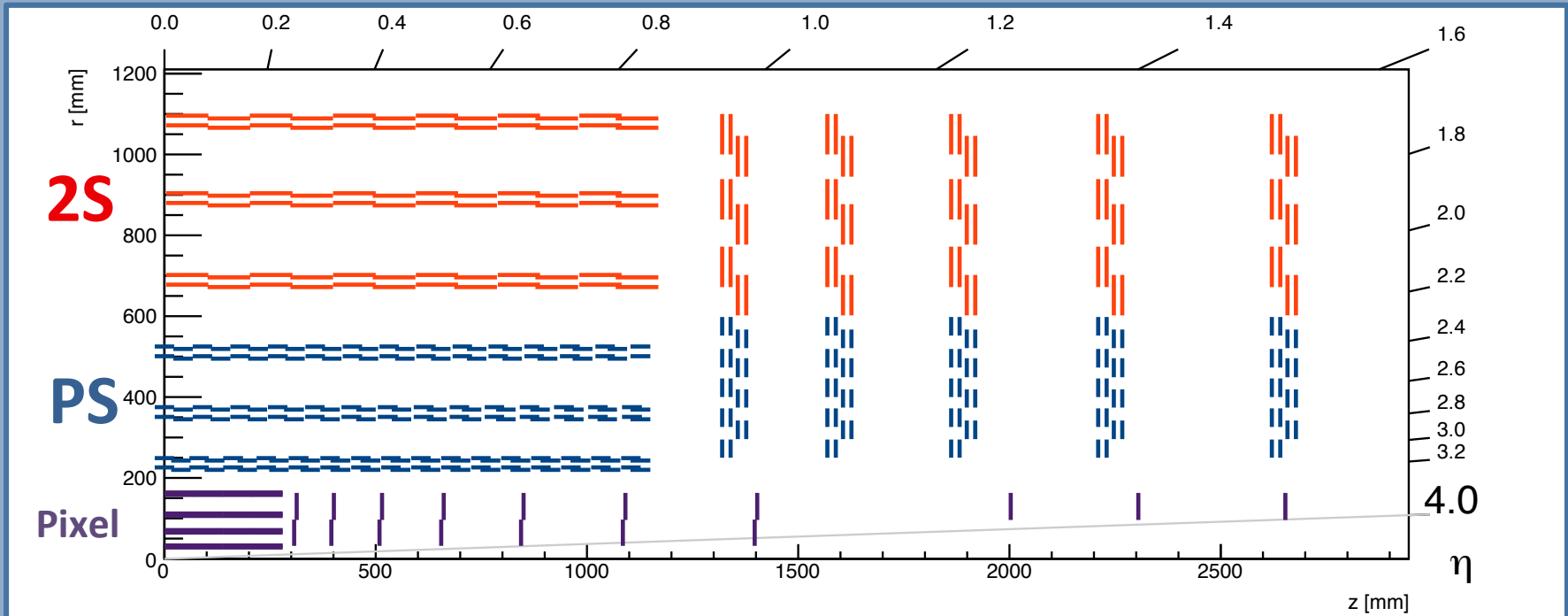
- $\sim 214 \text{ m}^2$ of silicon strip sensors, 11.4 million strips

Pixel

- Inner 3 layers: silicon pixels ($\sim 1 \text{ m}^2$)
- 66 million pixels ($100 \times 150 \mu\text{m}$)



Layout for the CMS Phase II Tracker



Baseline layout:

$R > 20$ cm: Outer Tracker with 6 barrel layers and 5 endcap disks (with 2S and PS modules)

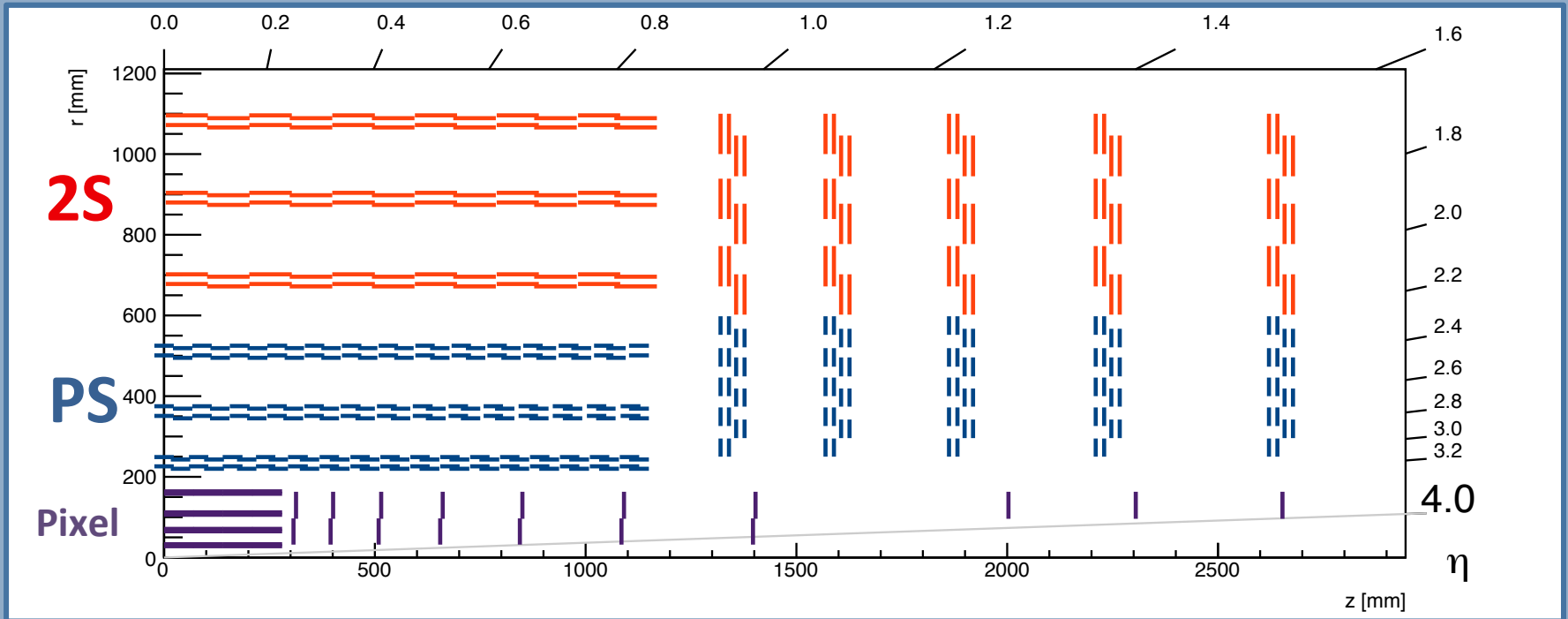
$20 \text{ cm} > R > 4$ cm: Inner Tracker with 4 barrel layers and 10 disks (with pixel modules)

Pixel detector layout:

- “Similar” to Phase I Pixel
- Extends to $\eta=4$ in the forward region

Requires most R&D work

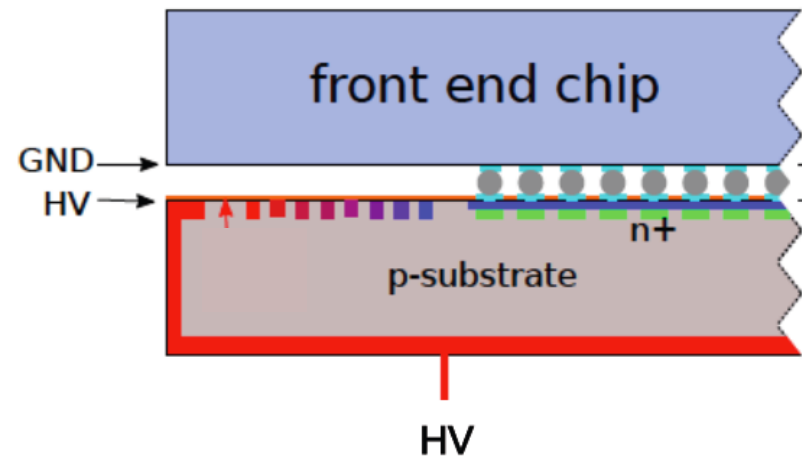
Layout for the CMS Phase II Tracker



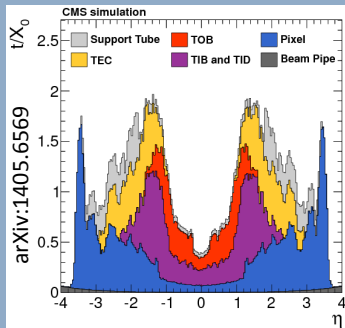
Pixel Issues:

- How to manufacture and bump bond very fine pitch pixel ($25\ \mu\text{m} \times 100\ \mu\text{m}$).
- Radiation damage up to $\Phi = 2 \times 10^{16}\ \text{cm}^{-2}$.

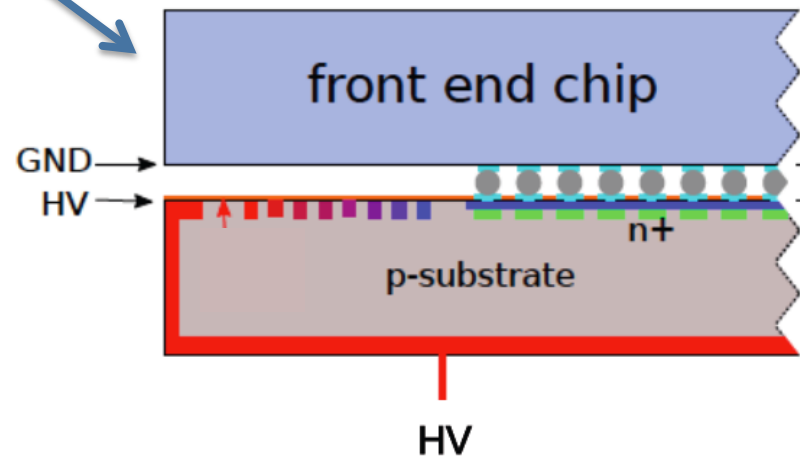
Pixel Design Challenges



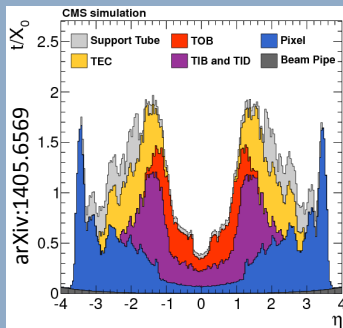
Pixel Design Challenges



Reduce material budget

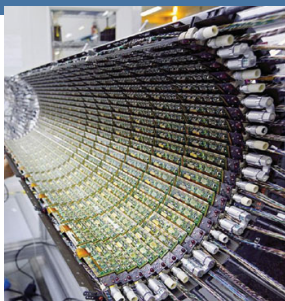
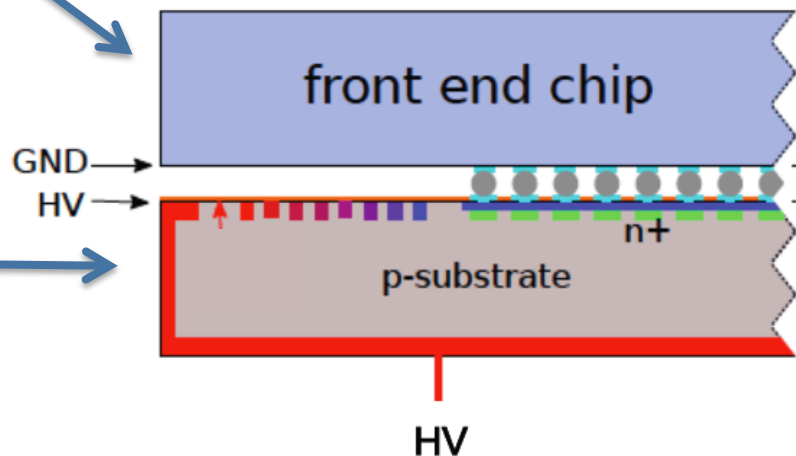


Pixel Design Challenges

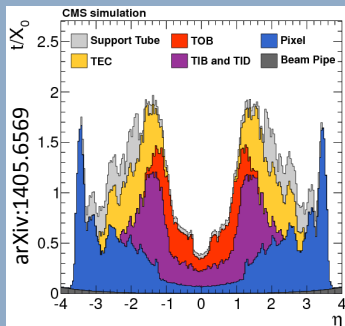


Reduce material budget

Each experiment has to cover $8 + ? \text{ m}^2$ with silicon
→ Be cheap and reliable

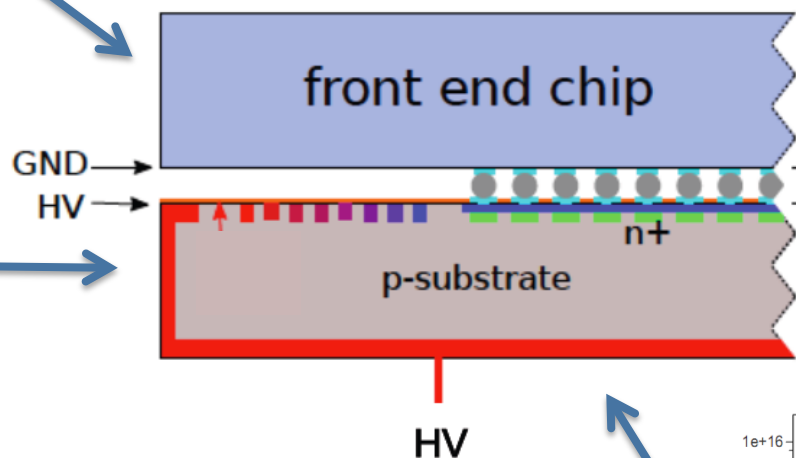
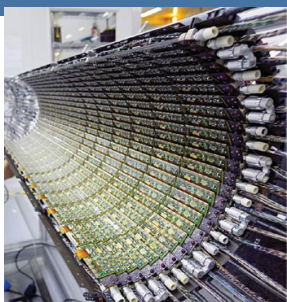


Pixel Design Challenges

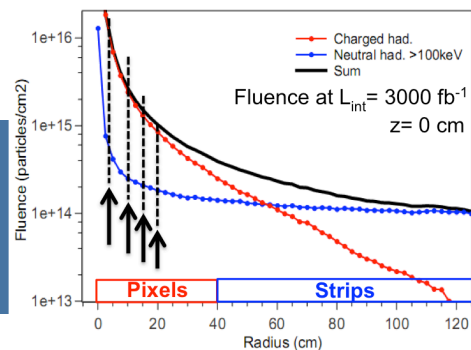


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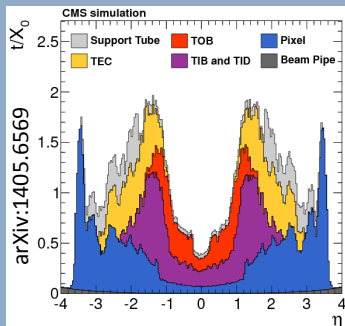


Improve radiation tolerance
 → Maximize efficiency and minimize noise hits



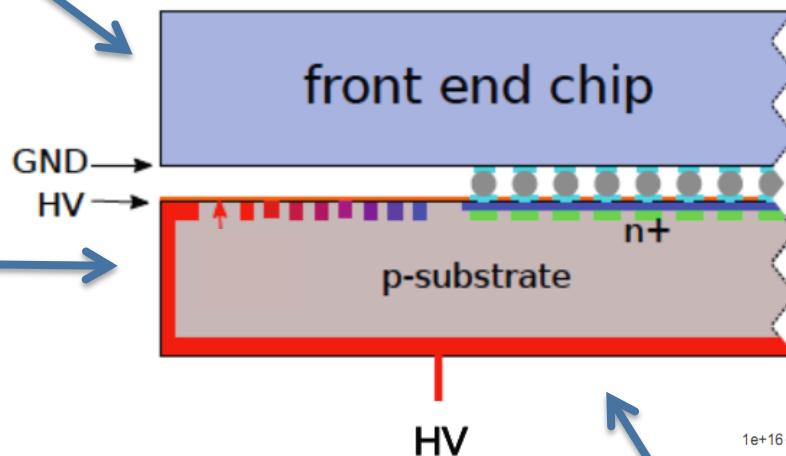
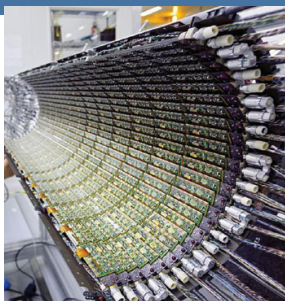
10/13/14

Pixel Design Challenges



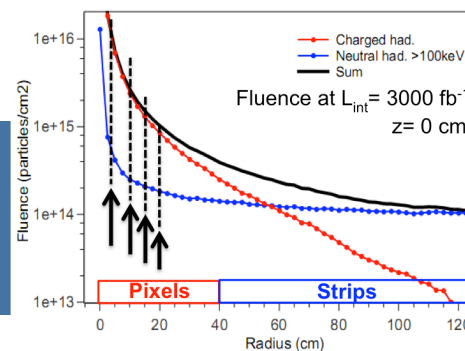
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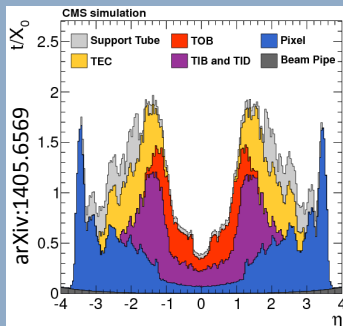


Improve inter-connection techniques

Improve radiation tolerance
 → Maximize efficiency and minimize noise hits

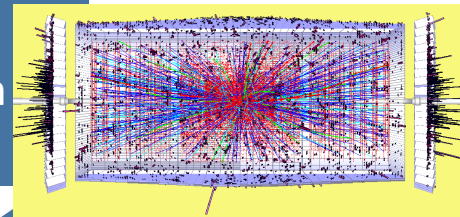


Pixel Design Challenges

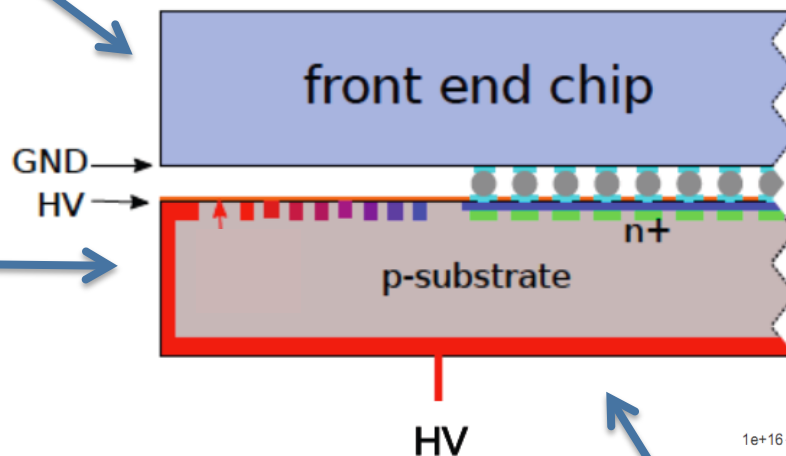
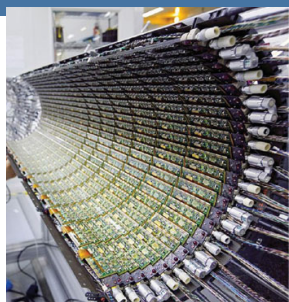


Reduce material budget

Luminosity: $5 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
 \rightarrow Improve spatial resolution and maintain occupancy at $\approx \%$ level

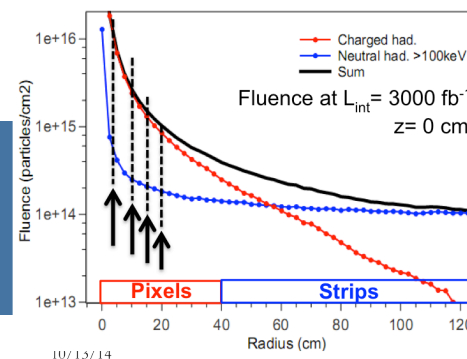


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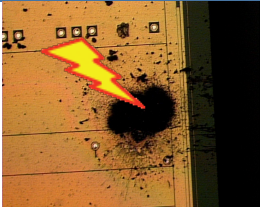
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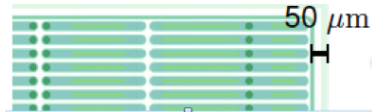


Pixel Design Goals

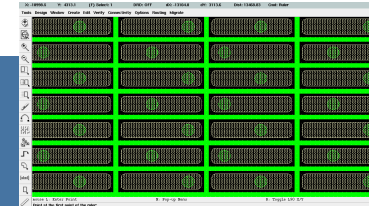
Sparking at sensor edge



Decrease inactive edges



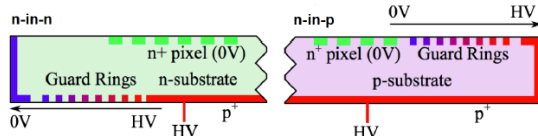
Optimize pixel geometries (small pitches)



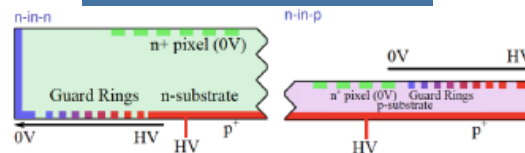
Bump bonding (small pitches, thin sensor / ROC)

Choose sensor bulk material

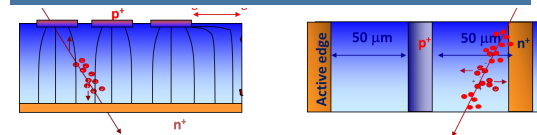
- n-in-p 6" wafers



Sensor (& ASIC) Thickness



Move to 3D technology



Pixel Design Goals

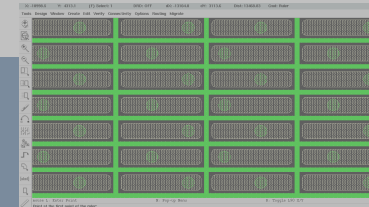
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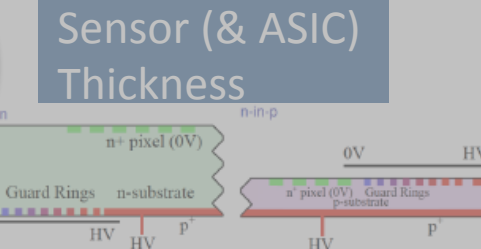
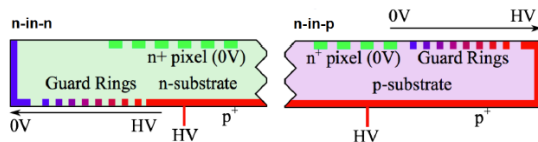
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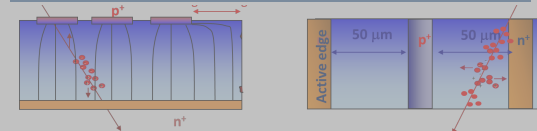
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Sensor (& ASIC) Thickness

Move to 3D technology



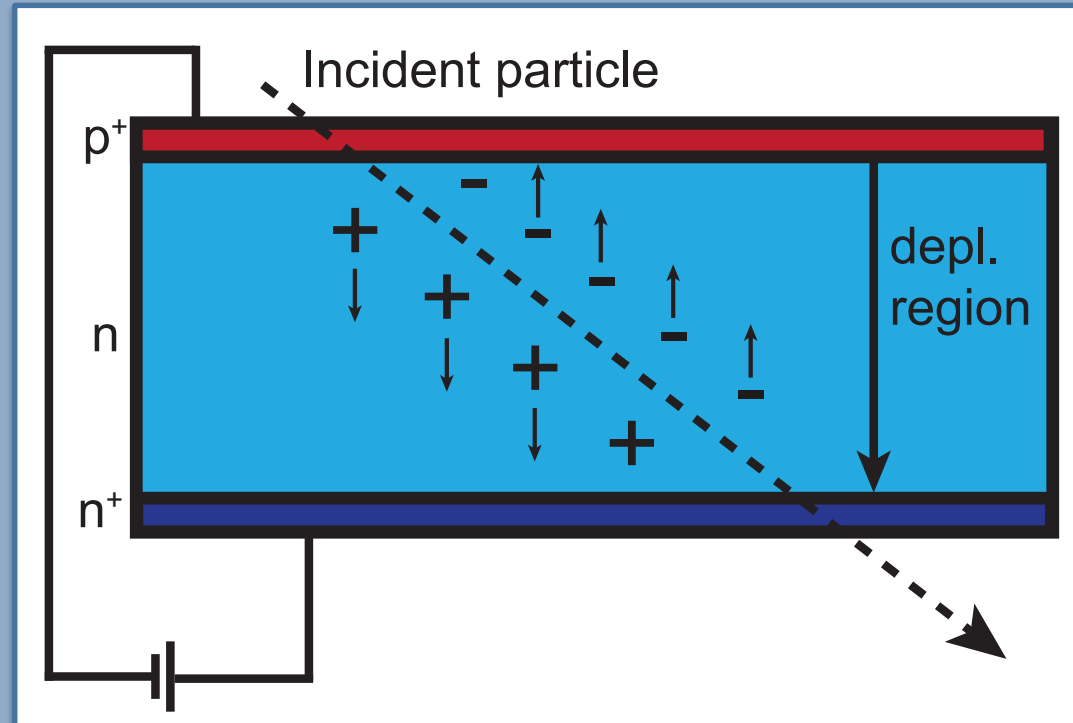
Silicon sensor principle

Operation:

- pn diode in reverse-bias
- Depletion layer starts from junction
- Particle ionises Si, producing e/h-pairs
- e/h-pairs drift in E-field to electrodes

Properties:

- Thickness currently 300 μm
- Signal ~ 25000 e/h-pairs
- Segmented in strips or pixels



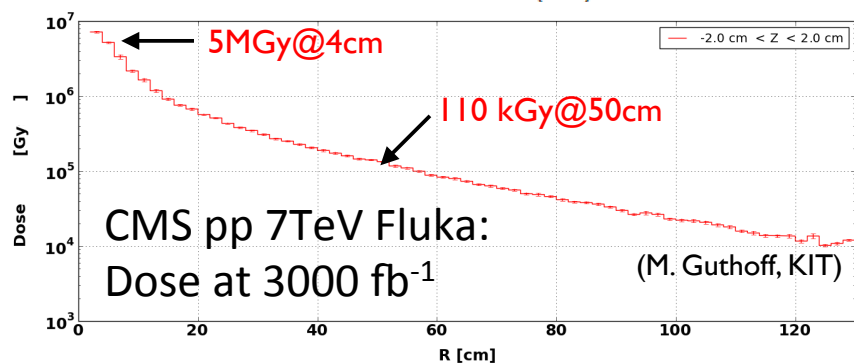
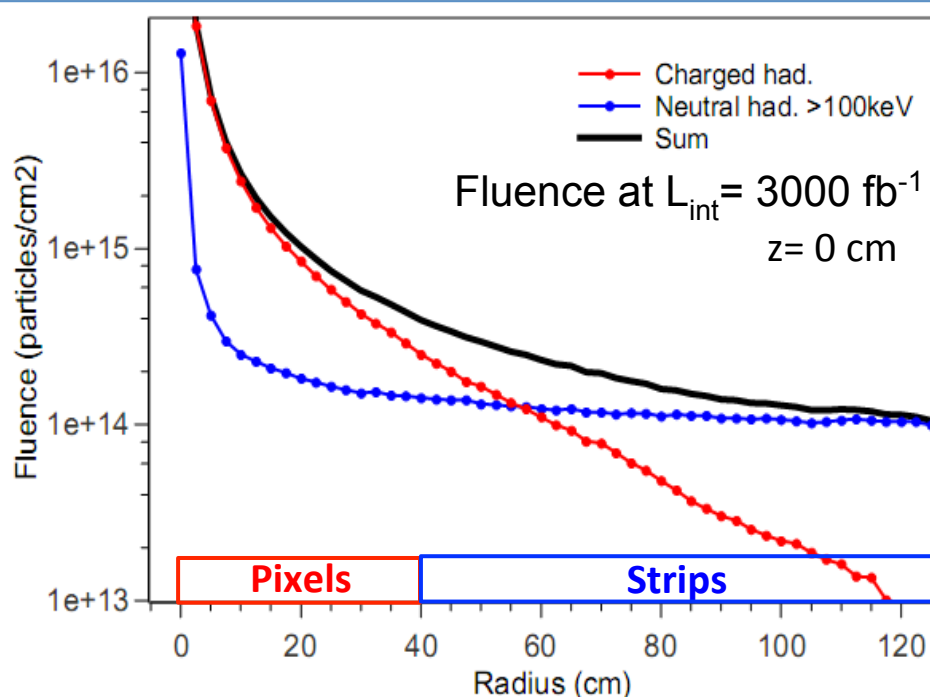
Advantage of silicon:

- Low ionisation energy
- Fast signal collection

Relevant parameters for performance

- Leakage current (I_{dep})
- Depletion voltage (V_{dep}) → operational voltage
- Power consumption ($P = U \cdot I$) & heat load
- Collected charge

Radiation damage in the tracker



Fluence up to $\Phi \approx 2 \times 10^{16} \text{ cm}^{-2}$ for innermost pixel layer

- Phase 2 will yield $3,000 \text{ fb}^{-1}$ and about $300 \text{ fb}^{-1}/\text{year}$.
- Radiation damage of the previous 10 years in only one year!

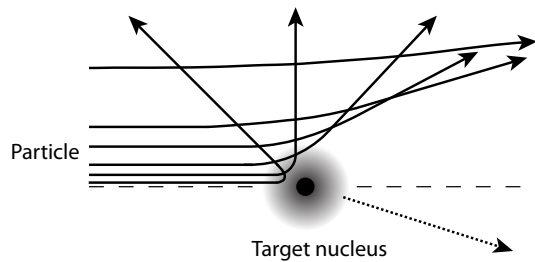
Surface damage not negligible for pixel region:

- Dose at 4 cm: 5 MGy
- Dose at 50 cm: 110 kGy

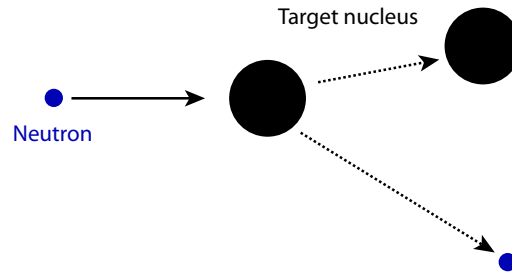


Generation of bulk damage

Coulomb scattering



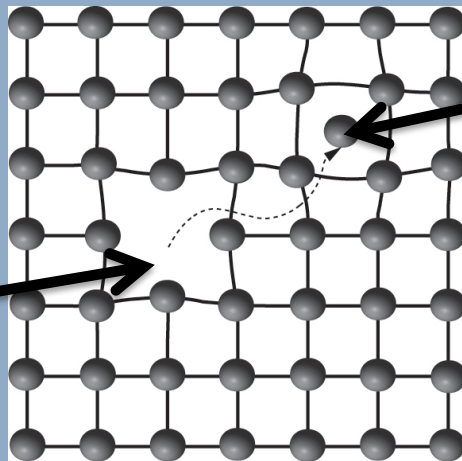
Elastic nuclear scattering



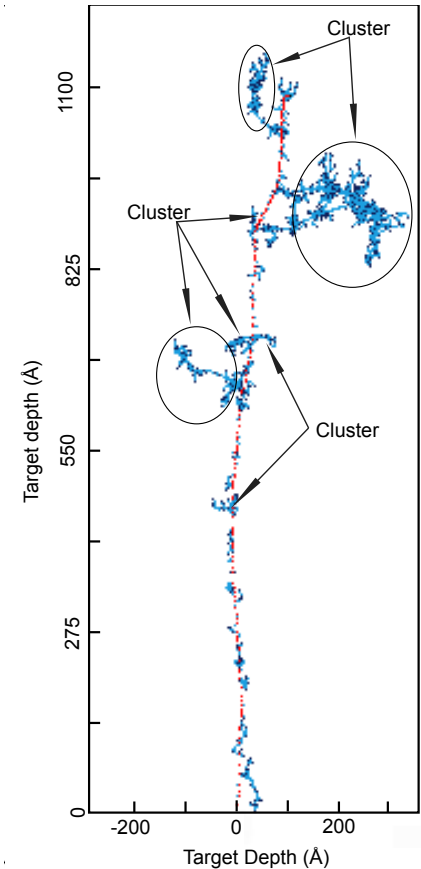
PKA

$$E_{\text{PKA}} > 25 \text{ eV}$$

Vacancy
missing Si atom



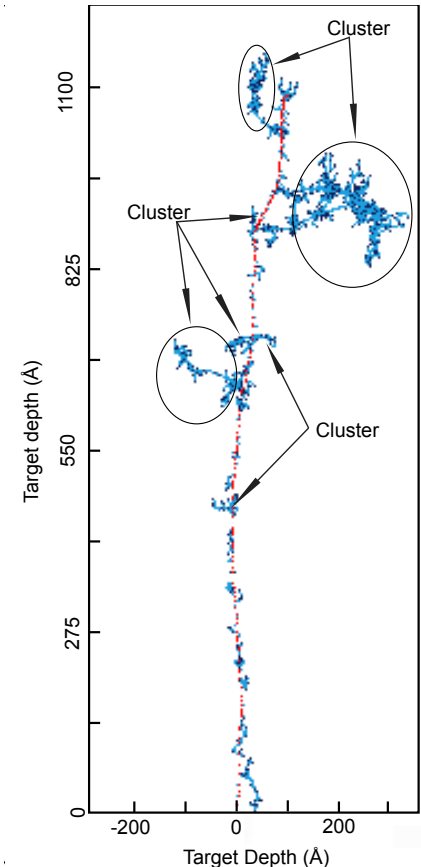
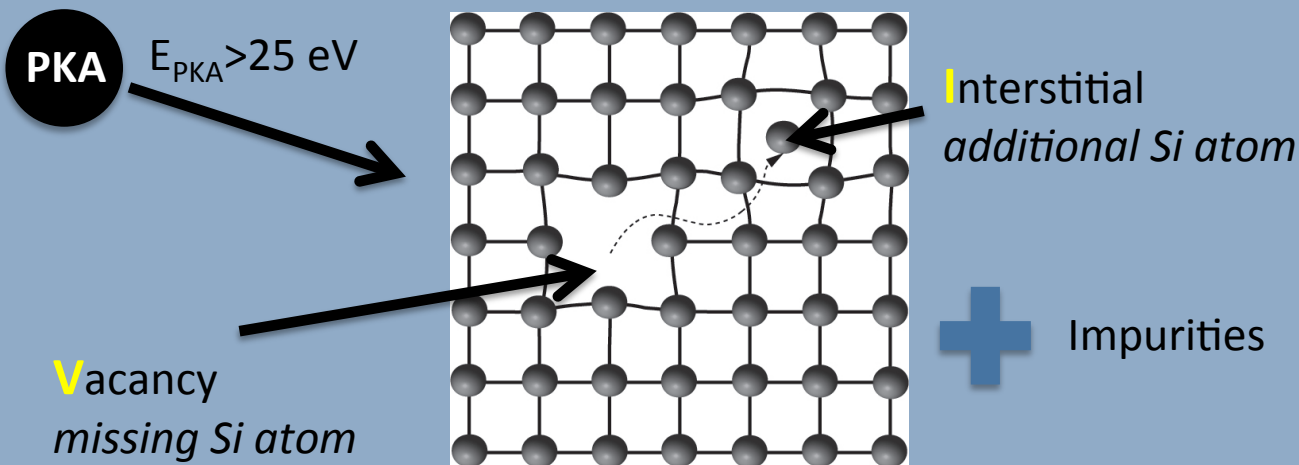
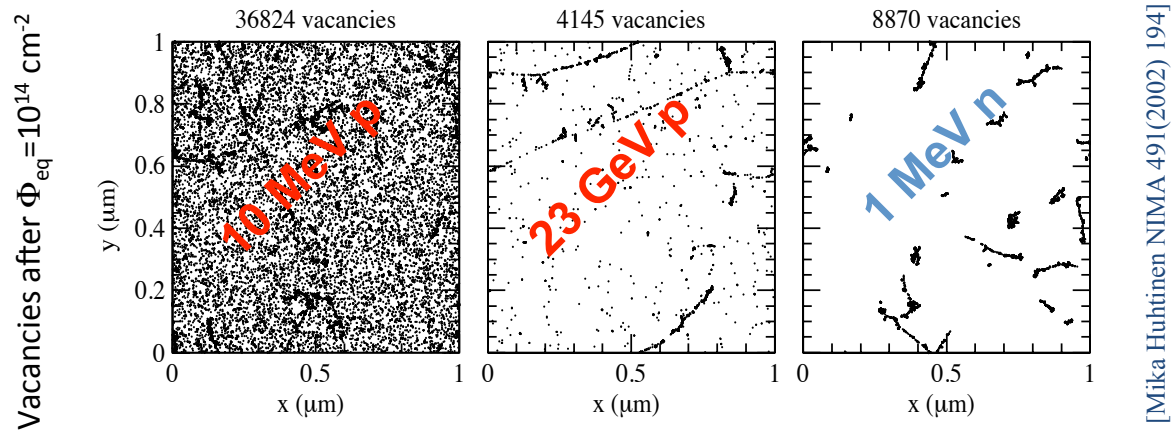
Interstitial
additional Si atom



Simulation of 50 keV PKA
damage cascade (1 MeV n)

Generation of bulk damage

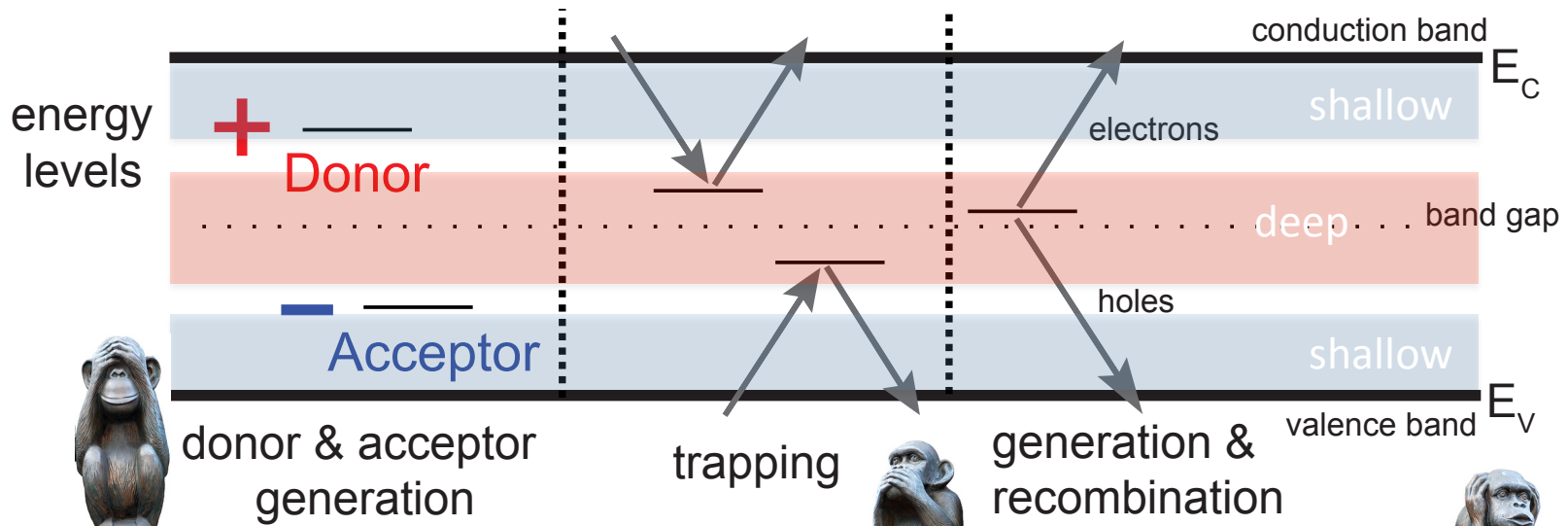
Depending on particle charge and mass



Simulation of 50 keV PKA damage cascade (1 MeV n)

Impact of defects on detector properties

Determined by Shockley-Read-Hall statistics

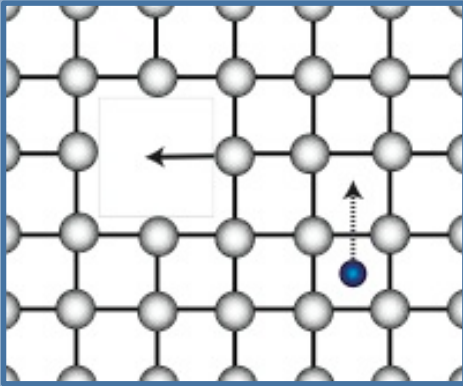


Charged defects (at RT)
→ **Change of space charge**
(Acceptors in the lower half and donors in the upper half of the band gap)

Deep defects
→ **CCE**
(Shallow defects do not contribute due to de-trapping)

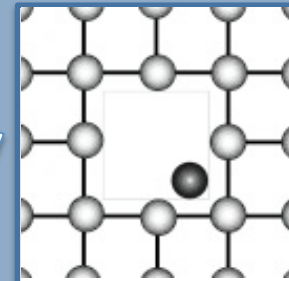
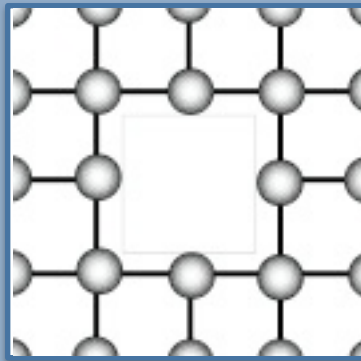
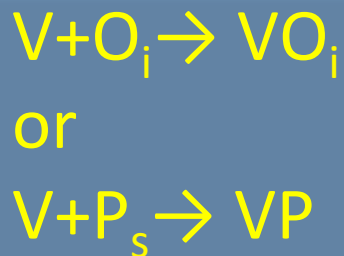
Levels close to midgap
→ **I_{leak} (Noise)**
→ **Polarisation effects**
→ **Power consumption / heat dissipation**

Approach: Defect engineering

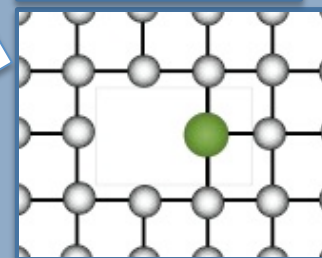


- Frenkel pairs are created due to irradiation
- Defect complexes form due to migration
 - Migration depends on thermal energy
 - Kinetics like in chemical reactions

Example: Benefit of oxygen rich silicon: VO_i generation high – VP (donor removal) suppressed



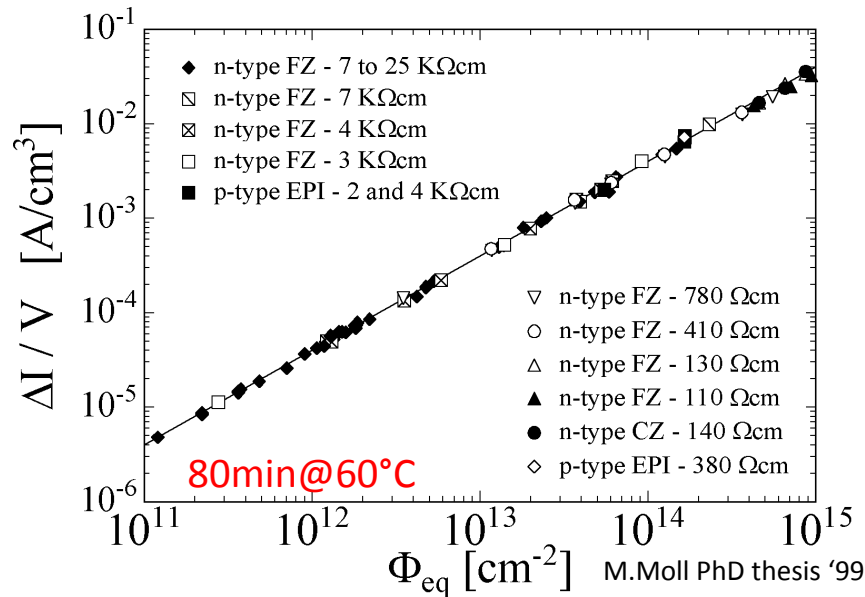
No influence!



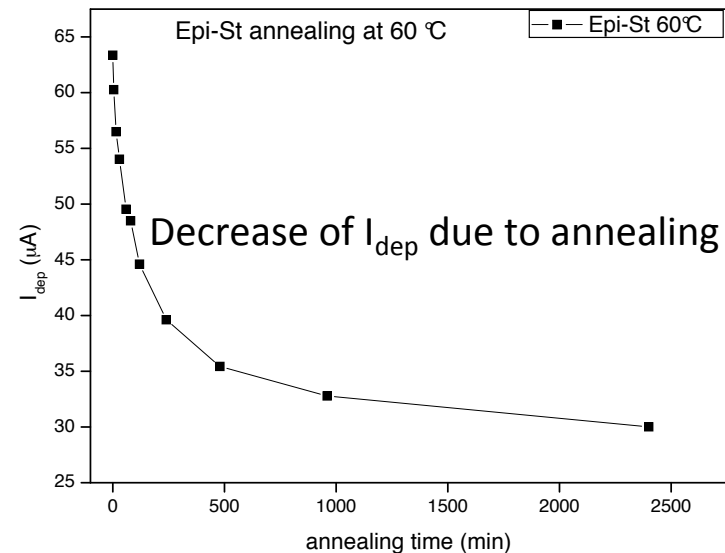
Donor removal

Change of leakage current...

... depending on the fluence...



... and on annealing

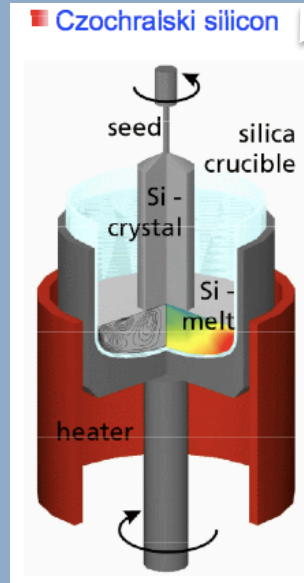
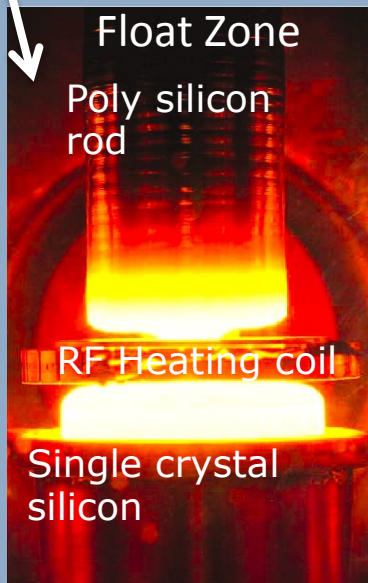


$$\Delta I = \alpha \cdot V \cdot \Phi_{eq}$$

- Damage parameter α not depending on material or particle type
→ Oxygen does not influence behaviour
- Constant over orders of magnitude
→ Noise increase (cooling helps due to T-dep of I_{leak})

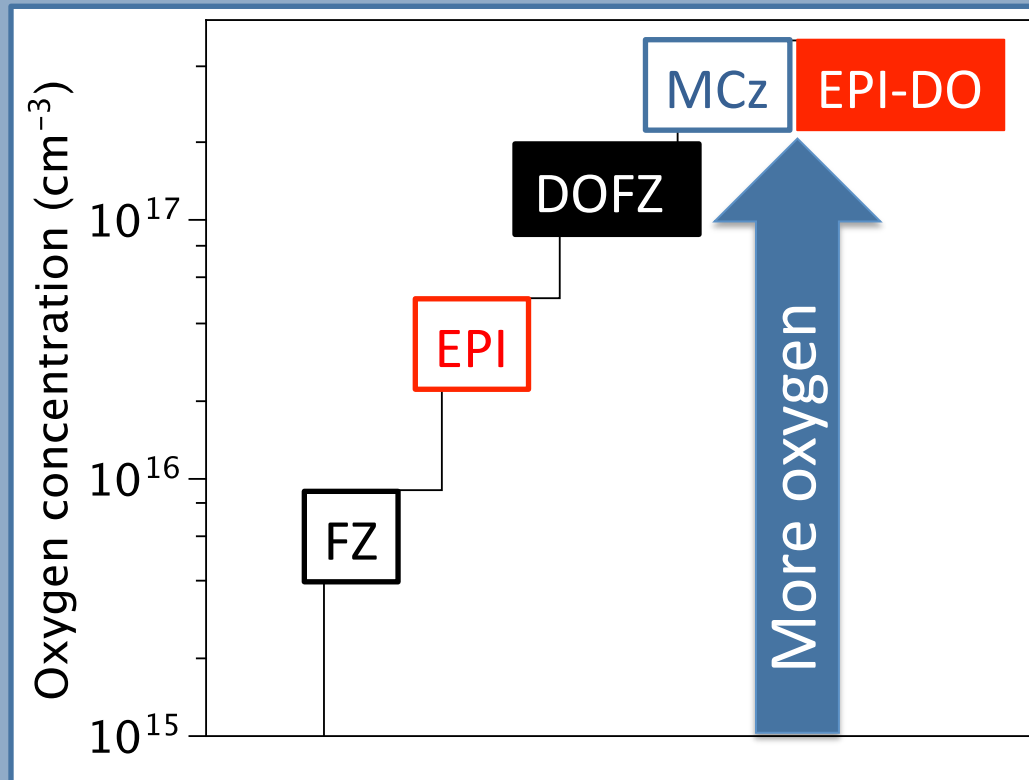
Silicon “Materials”

Float zone (FZ)
Magnetic Czochralski (MCz)
Epitaxial silicon (EPI)
Oxygen enriched FZ (DOFZ)
Oxygen enriched EPI (EPI-DO)



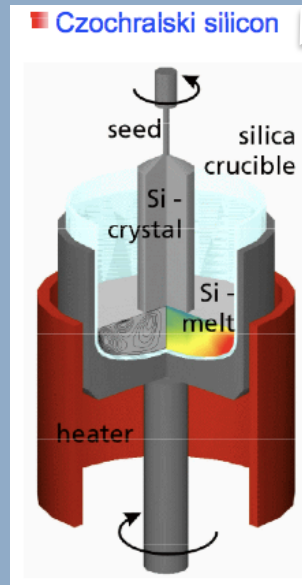
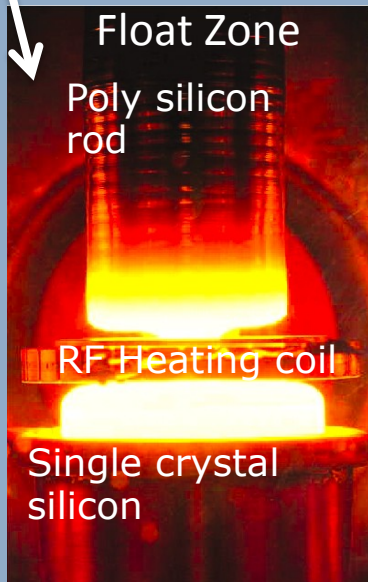
Si-growth process determines

Impurity concentration, mainly oxygen



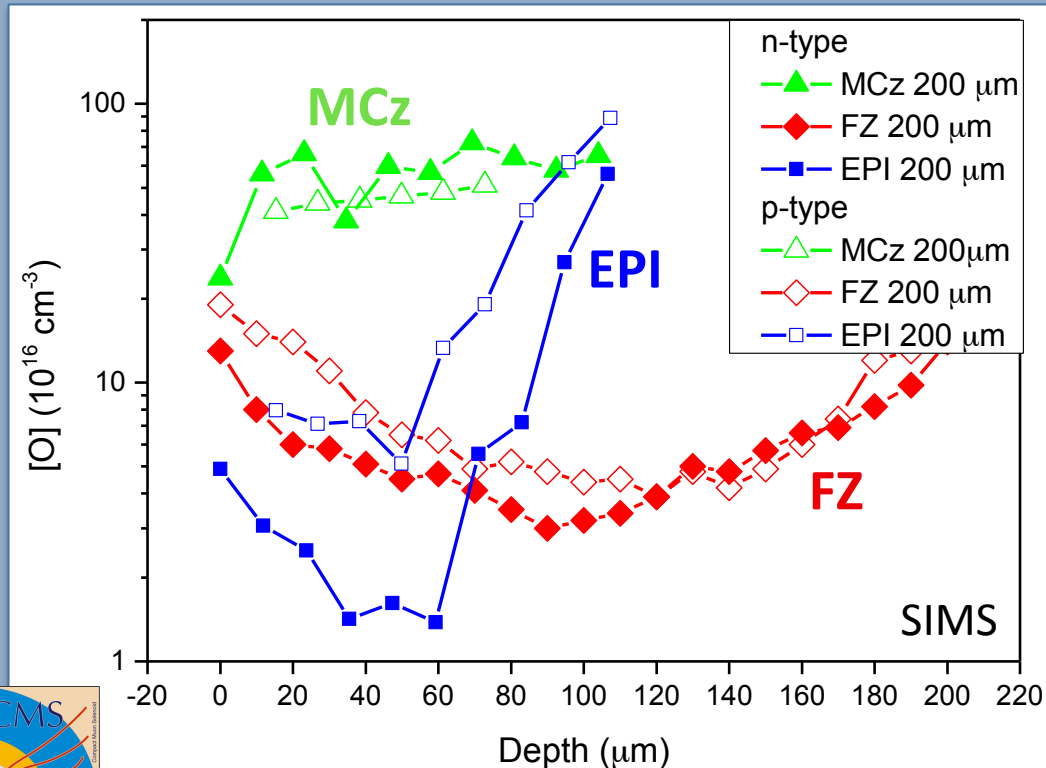
Silicon “Materials”

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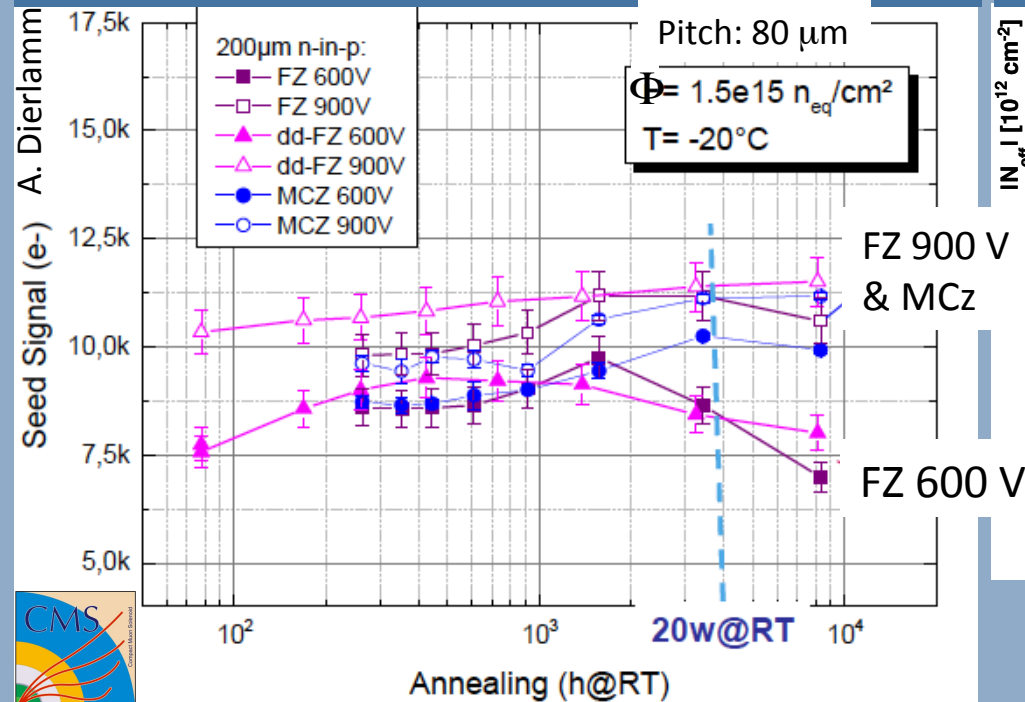
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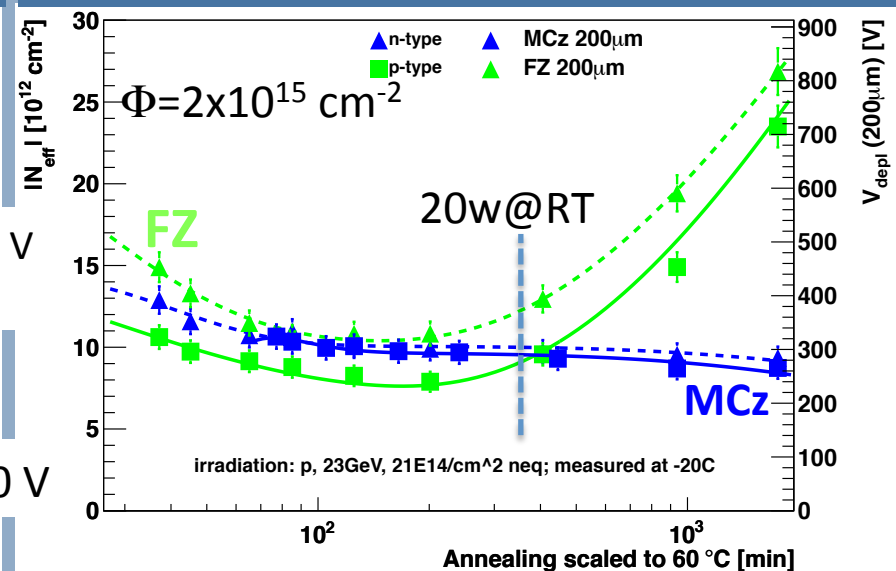


Advantageous Annealing Behavior of p-MCz

Proton & neutron irradiated strip sensors



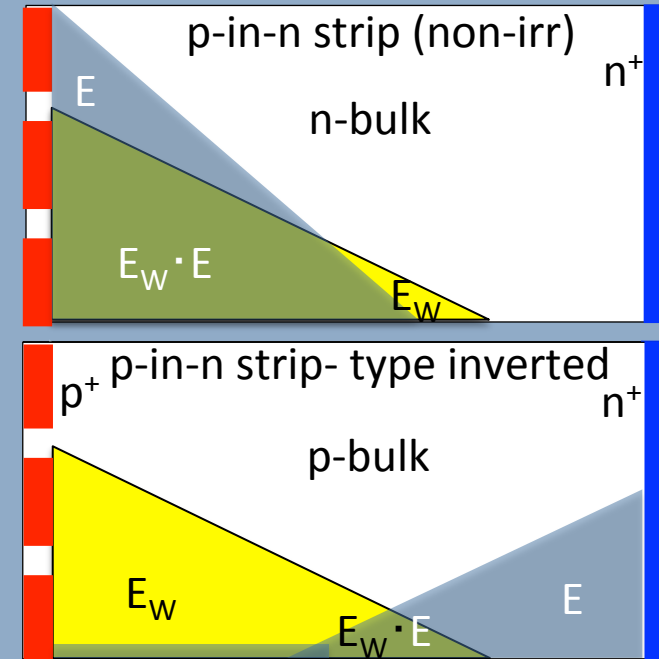
Proton & neutron irradiated pad diodes



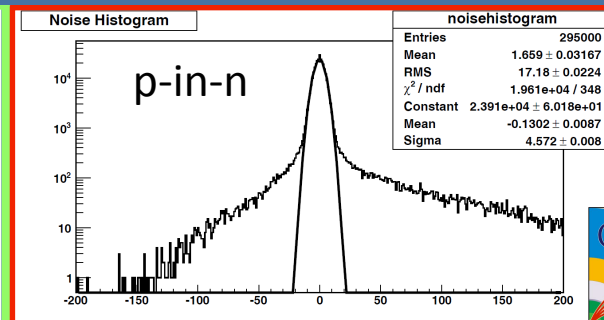
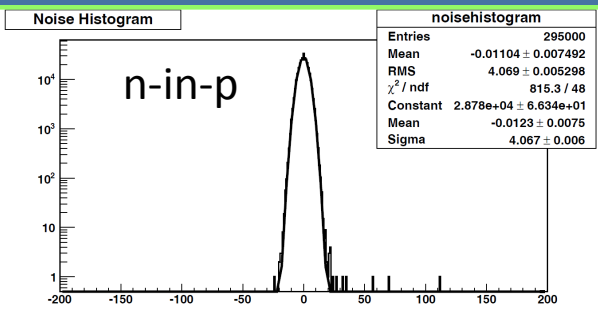
- P-type MCz demonstrates advantageous “long term annealing”
 - Operation voltage does not increase in MCz at long annealing times
- Longer warm up or controlled annealing periods possible
- Potentially good for power dissipation

From n-in-n to n-in-p

- Be cost effective \rightarrow N-in-p is a single sided process
- Thin \rightarrow very costly with a double-sided process
- N-side read out is preferred:
 - Favourable combination of weighting and electric field in heavily irradiated detector
 - CMS results show potential noise effects at doses $> 1 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
 - T-CAD simulations confirm the tendency of p-in-n strip sensors to exhibit higher electric fields at the strips for increasing oxide charge



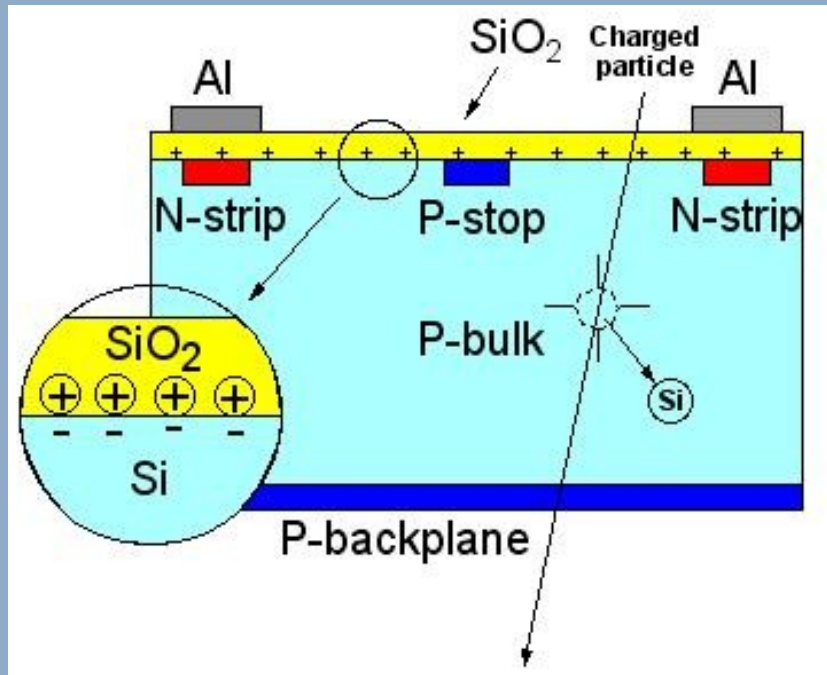
Noise histograms in 80 μm pitch strip sensor



A. Nürnberg



N-in-p sensors require isolation layer



Oxide charge in SiO₂

- Positive oxide charges
- Attract negative charges (electron accumulation at Si-SiO₂ interface)
- Bad/no strip or pixels isolation

- Additional p implant layer (p-spray)
- Additional p implant trench or ring (p-stop)

Problems of p-spray and p-stop:

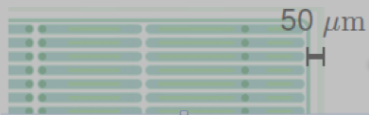
- Noise due to high fields or bad breakdown behavior
- Instability due to radiation damage
- Critical design point for fine pitches
 - Sets limits on inter pixel distances and so on

Pixel Design Goals

Sparking at sensor edge



Decrease inactive edges



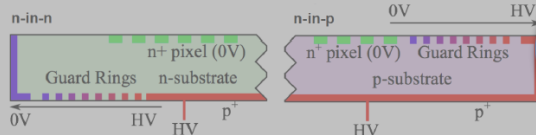
Optimize pixel geometries (small pitches)



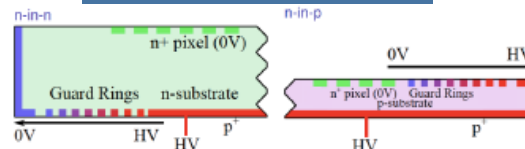
Bump bonding (small pitches, thin sensor / ROC)

Choose sensor bulk material

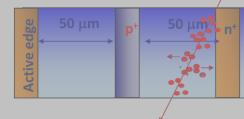
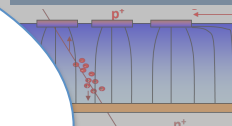
- n-in-p 6" wafers



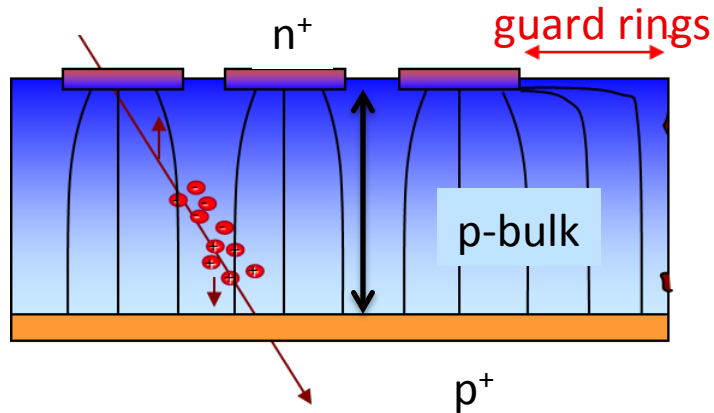
Sensor (& ASIC) Thickness



Move to 3D technology



Going thin



Thinning technologies:

- Deep diffusion
- Handling wafer
- Epitaxial growth
- Etching
- Grinding

Advantage:

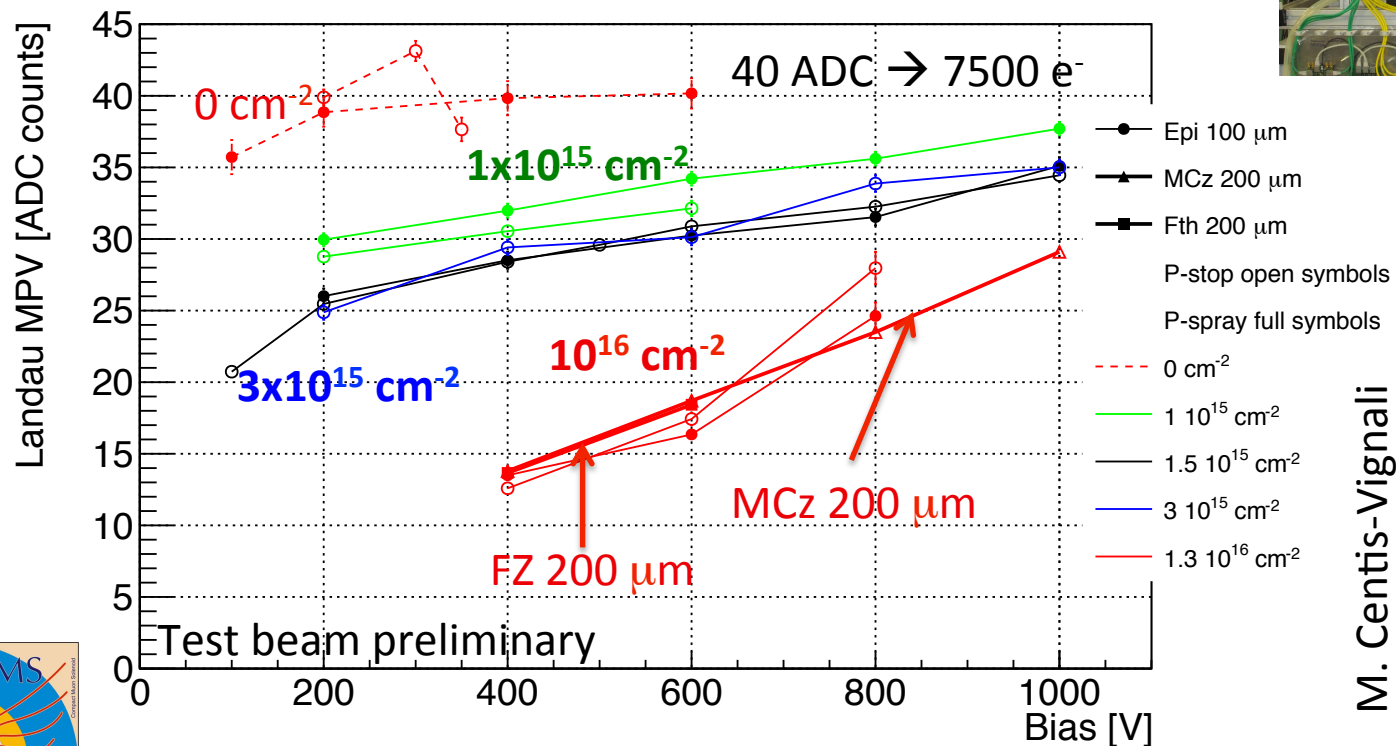
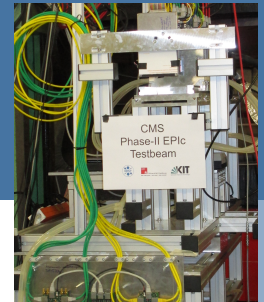
- Lower total leakage current after irradiation
- Lower operational voltage
→ less power consumption
- Short drift path → less trapping
- Higher electric fields at low V_{bias} (faster collection time)
- Less material (multiple scattering)
- Lower occupancy at high eta

Drawback:

- Smaller initial signal ($76 \text{ e}^-/\mu\text{m}$)
- Thinning technologies increase price
- Thin sensors (and ROCs) “bow”

Comparison between 100 μm & 200 μm sensor thickness

- Strip sensors with 80 μm pitch, mainly EPI with 100 μm active + 200 μm substrate
- @ 10^{16} cm^{-2} : MCz and FZ with 200 μm physical thickness
 - 100 μm \rightarrow faster signal recovery
 - 200 μm \rightarrow higher breakdown voltage
 - Similar signal height for both thicknesses at highest bias

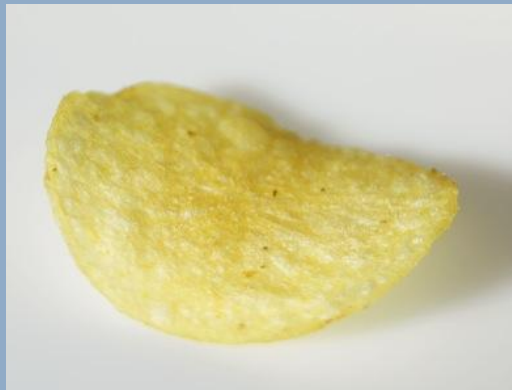
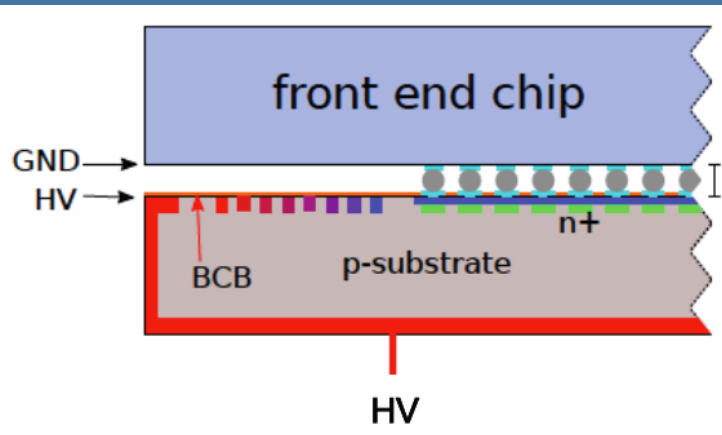


M. Centis-Vignali



Flatness of sensor and read out chip

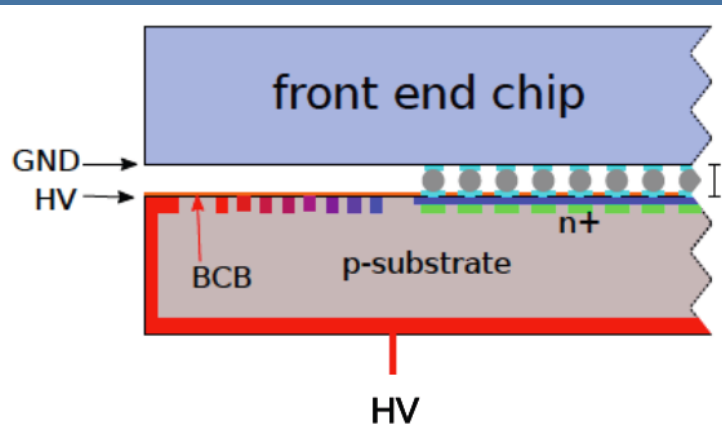
Normally bump bonding is done with flat chip and flat sensor



If sensor and roc are shaped like potato chips, bump bonding will not work well

Flatness of sensor and read out chip

Normally bump bonding is done with flat chip and flat sensor

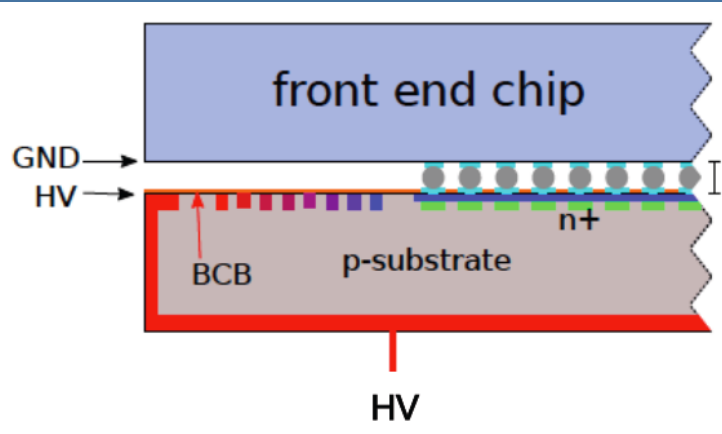


If sensor and roc are shaped like potato chips, bump bonding will not work well



Flatness of sensor and read out chip

Normally bump bonding is done with flat chip and flat sensor



ASICs: Multiple metal stacks and large ROC sizes can lead to internal stresses

Sensors: thinning, UBM, sensor size

- Bow during processing leads to alignment inaccuracies
- Bow during reflow can lead to disconnected bumps

Community and vendors are working on:

- Compensation layers
- Stress release
- Staves
- Temporary support

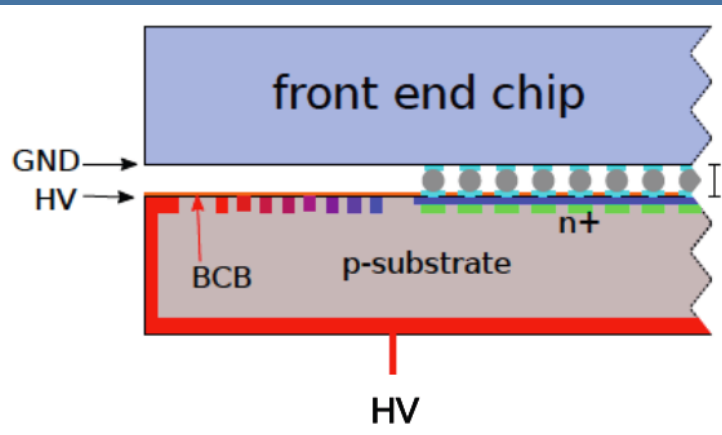


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Flatness of sensor and read out chip

Normally bump bonding is done with flat chip and flat sensor



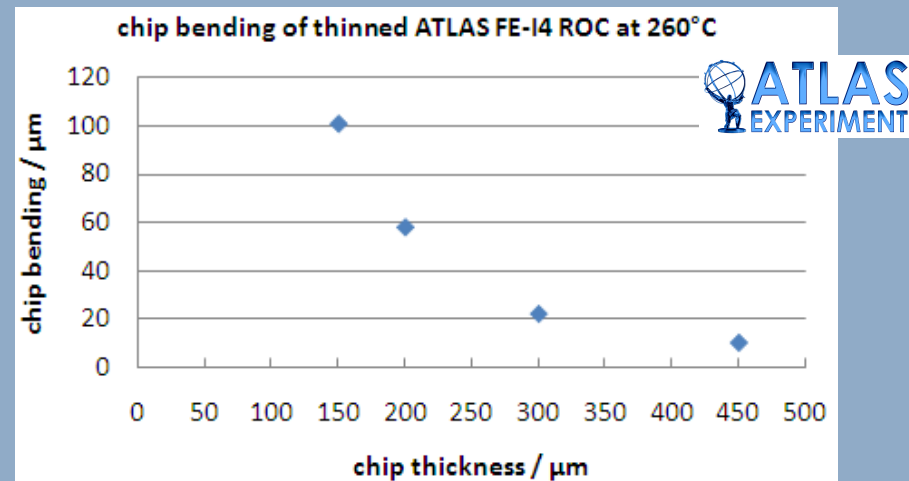
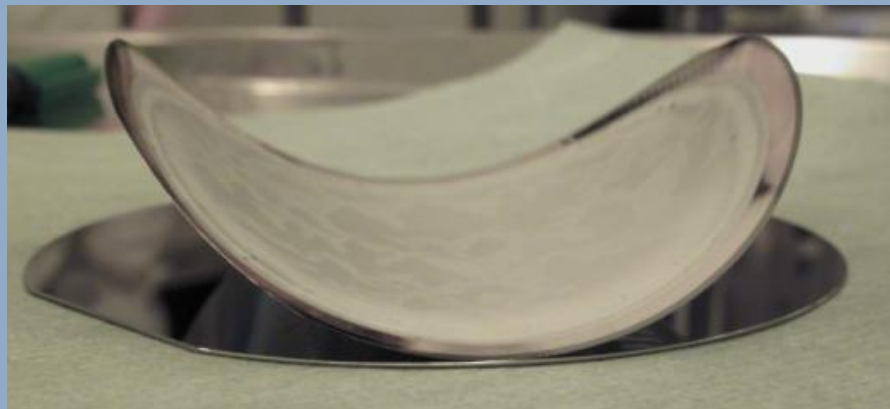
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T. Fritsch, TALENT Summer School, CERN 2013

Pixel Design Goals

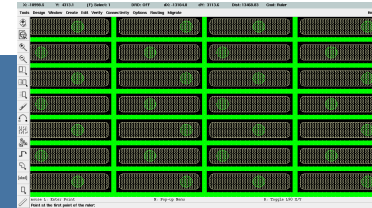
Sparking at sensor edge



Decrease inactive edges



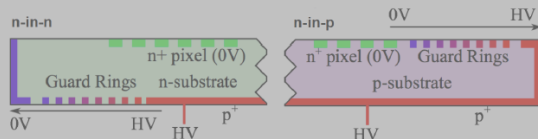
Optimize pixel geometries (small pitches)



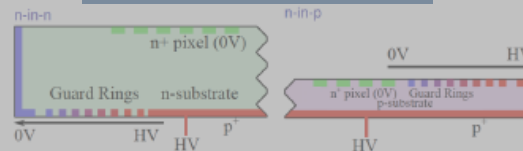
Thick bonding (small pitches, thin sensor / ROC)

Choose sensor bulk material

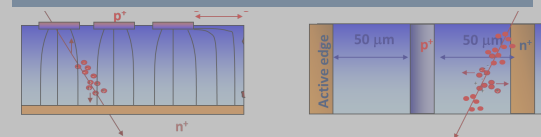
- n-in-p 6" wafers



Sensor (& ASIC) Thickness



Move to 3D technology



Investigate Fine-Pitch Pixel Sensors

Motivation

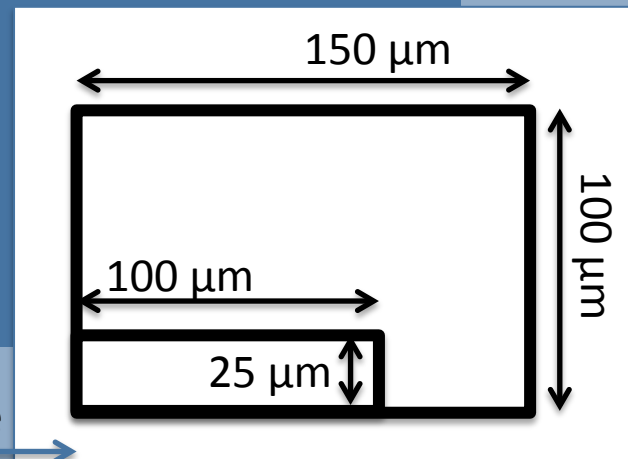
- Improve spatial resolution (depending on $r\phi$, rz)
 - Keep occupancy below %-level
- Investigate $25\ \mu\text{m} \times 100\ \mu\text{m}$ (and $50\ \mu\text{m} \times 50\ \mu\text{m}$)

Problems for fine pitches

- Not enough space for p-stop for each pixel cell
 - Not enough space for conventional bias scheme (for sensor tests)
 - Not much experience with bias scheme at very high Φ
- Investigate alternatives

- Common p-stop
- Common punch through
- Poly-Si resistors
- No biasing scheme

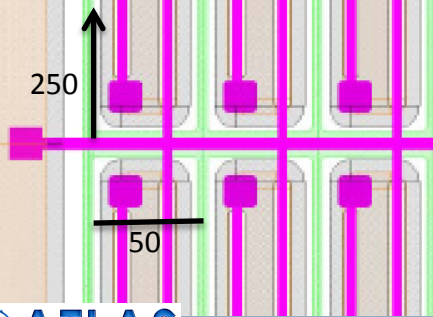
Comparison of current CMS pixel cell size to foreseen size



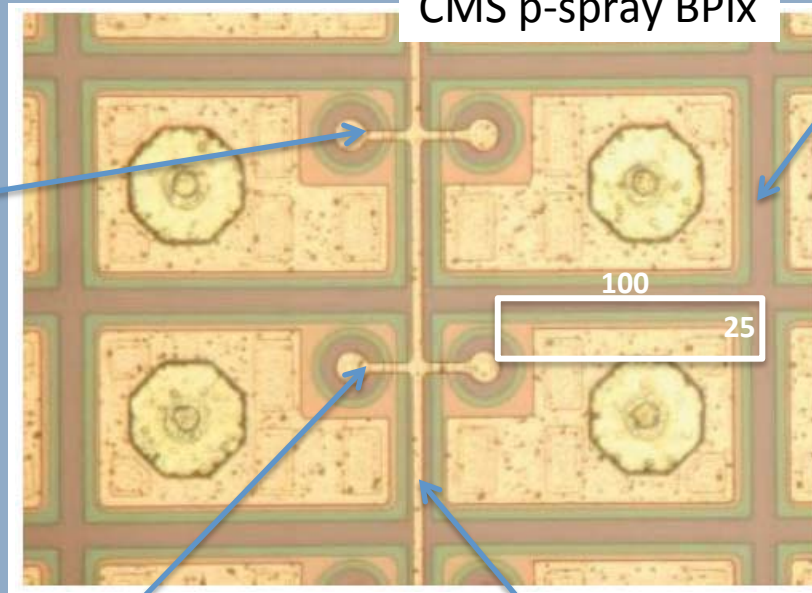
Investigate Alternatives

Poly-Si resistor

Type13 (Wide p-stop)

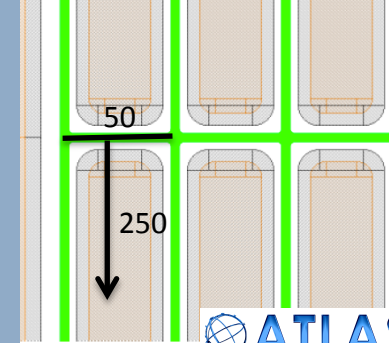


CMS p-spray BPix

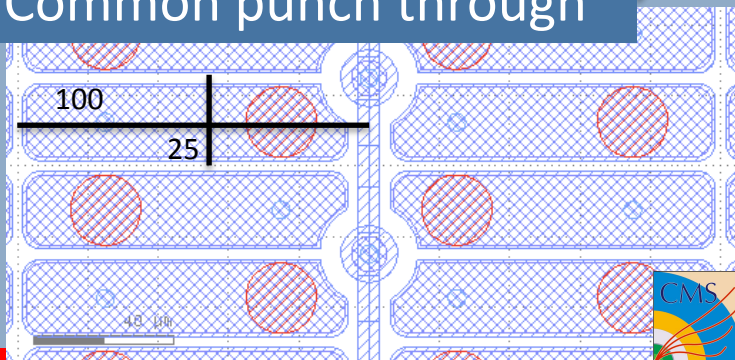


Common p-stop

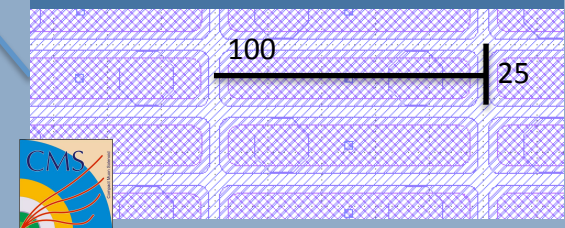
Type 19 (No Bias)



Common punch through

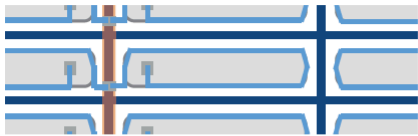


No biasing scheme P-spray



Effect of the Bias Rail at $1 \times 10^{16} \text{ cm}^{-2}$

(a) Poly Silicon, Common P-stop



(b) Poly Silicon, P-spray



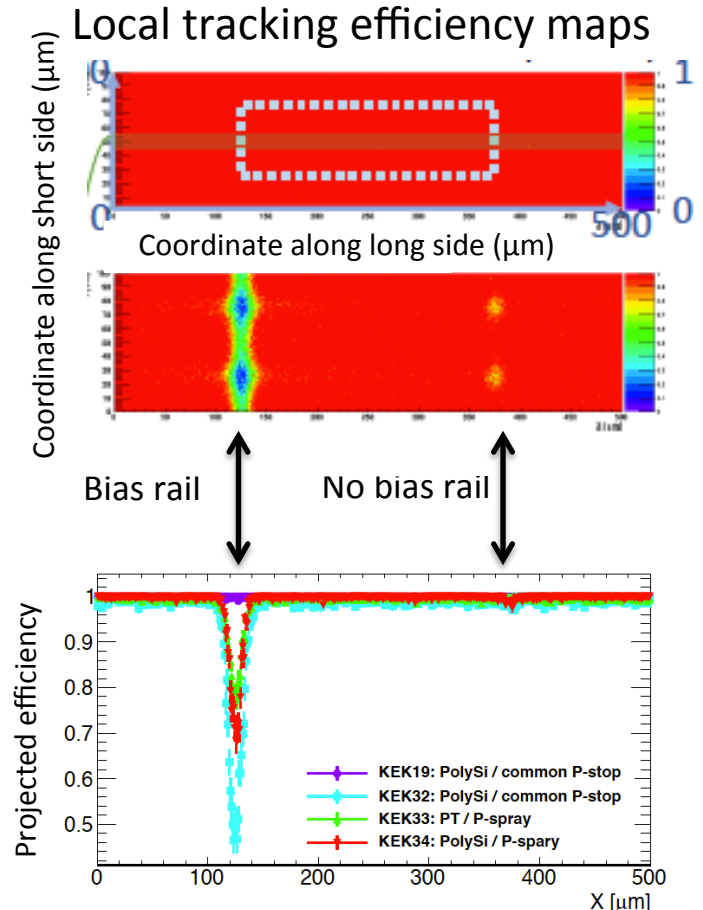
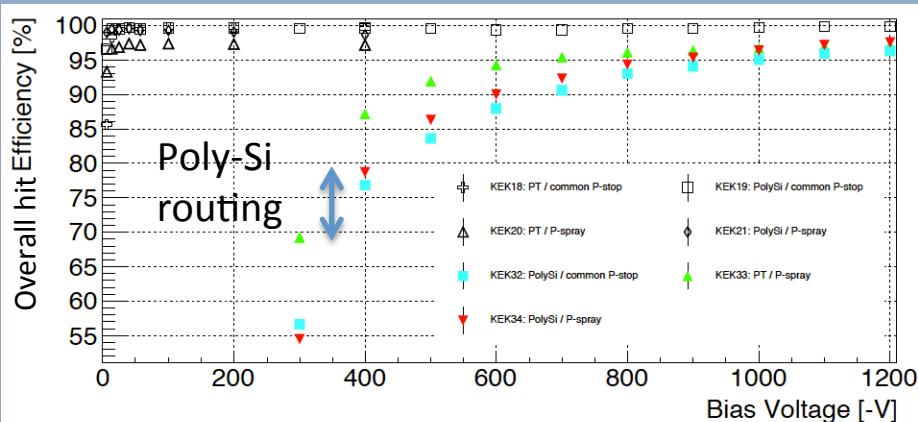
(c) Punch Through, Common P-stop



(d) Punch Through, P-spray



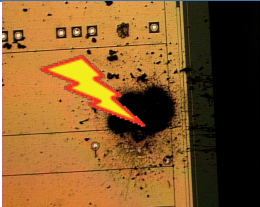
Pixel Electrode Common P-stop P-spray
Bias Rail Poly Silicon Resistor Punch Through Dot



- Severe efficiency loss at the boundary of pixels, under bias rail
- Sight efficiency loss due to the routing of bias resistor

Pixel Design Goals

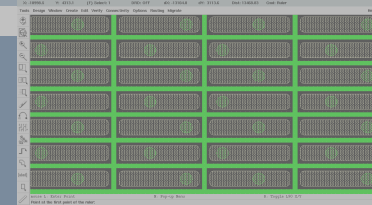
Sparking at sensor edge



Decrease inactive edges



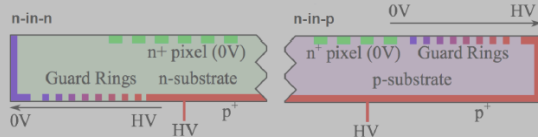
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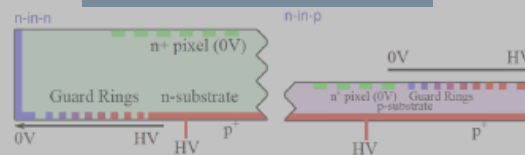
Bump bonding (small pitches, thin sensor / ROC)

Choose sensor bulk material

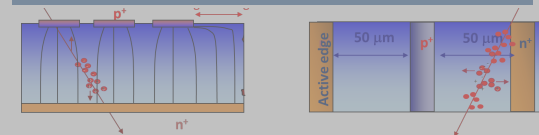
- n-in-p 6" wafers



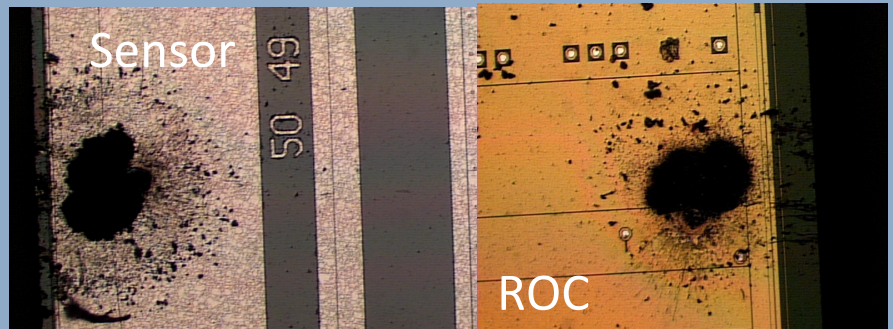
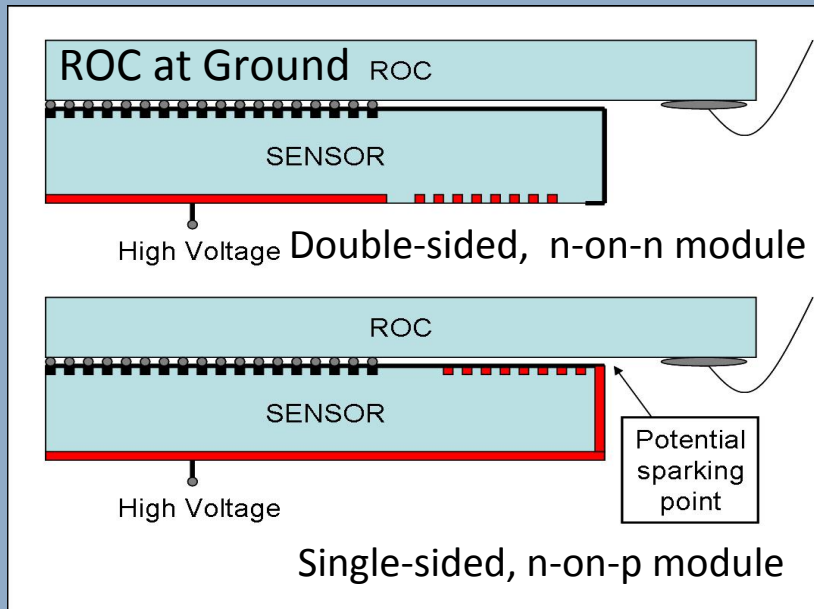
Sensor (& ASIC) Thickness



Move to 3D technology



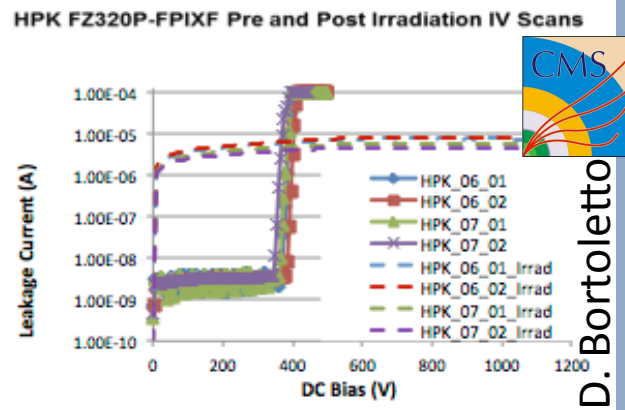
Spark protection



- Consequence of p-type choice: HV is close to ASIC and sparking can occur
- As voltages up to 1000 V may be required, protection is necessary

Post process solutions

- Encapsulation - becomes brittle after irradiation
- Paralyne-N coating (ATLAS & CMS) - Tests show very good radiation hardness



In process solutions

- BCB coating (ATLAS) with lithography on sensor surface
- N+ implantation + passivation barrier (under test)

Pixel Design Goals

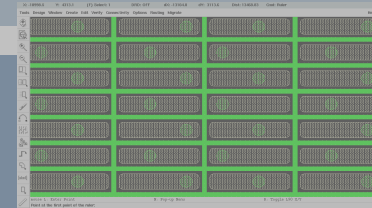
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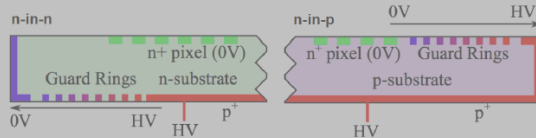
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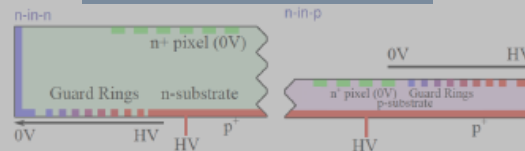
Bump bonding (small pitches, thin sensor / ROC)

Choose sensor bulk material

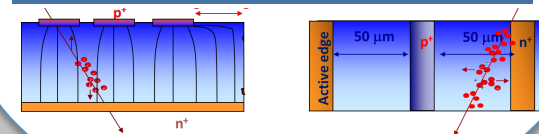
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Sensor (& ASIC) Thickness

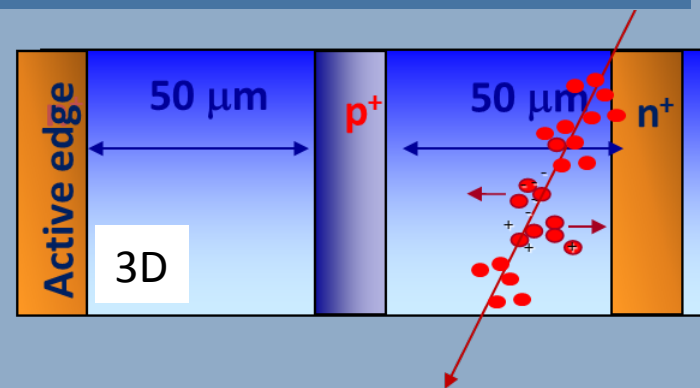
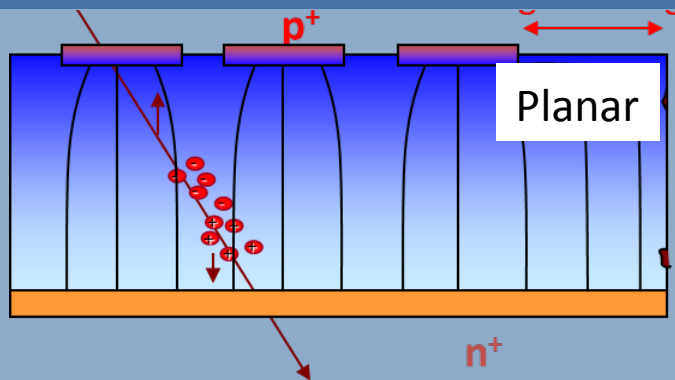


Move to 3D technology



Thin Planar Sensors and 3D

The most promising technologies that are options for the phase II pixel upgrade:
3D and planar pixel sensors



Common advantages:
Short drift path
Higher fields at same V_{bias}
Common problems:
ROC availability
Bump bonding

Thin planar sensors:

- Low total leakage after irradiation

Drawback:

- Smaller initial signal ($76e^-/\mu\text{m}$)
- Design limits for small pixels
- Thinning of handling wafer

3D sensors:

- Thick sensor possible

Drawback:

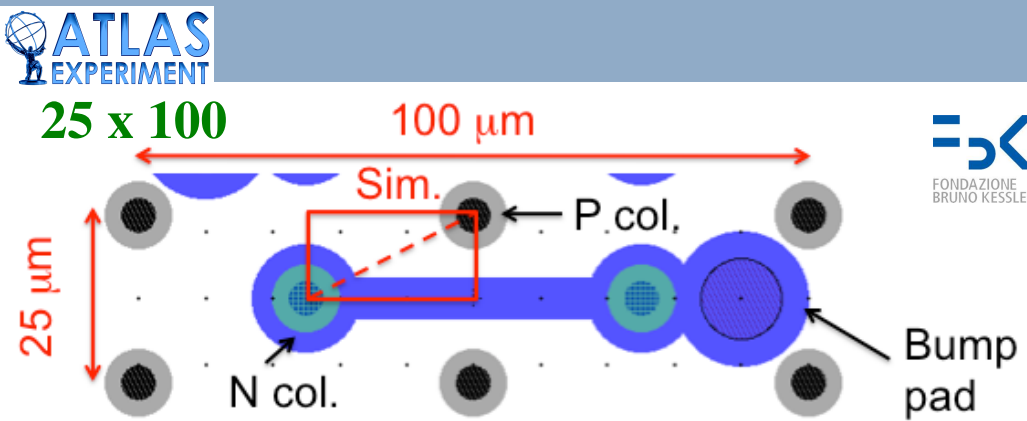
- Higher Capacity
- Low yield
- Are very small pitches possible?

ATLAS and CMS are jointly submitting 2 new productions!

3D Sensors with Small Pitch

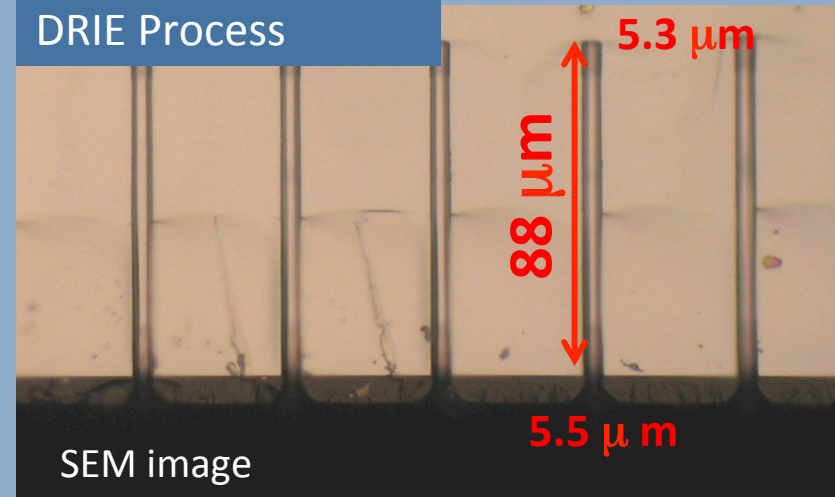
- Smaller pitches require very narrow columns
 - And smaller inter-electrode spacing required for high Φ
 - Defined aspect ratio between hole heights and width
 - To keep aspect ratio, sensors need to be thinner
- Use handling wafer, requires thinning

Issue could arise from placing bump pads over columns



R. Mendicino Trento Workshop 2015

DRIE Process



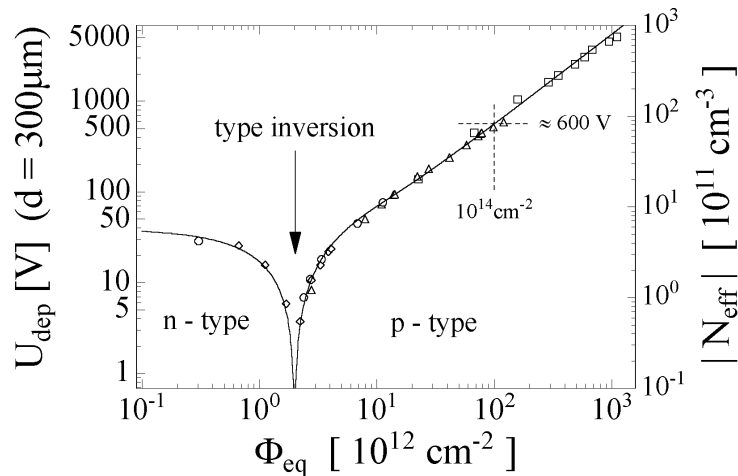
SEM image

Summary

- The vast majority of the pixels is defined to be n-in-p
- Technical challenges are now to fine tune solutions
 - Technology choice for innermost layers
 - Choice of optimal thickness and material
 - Handling and processing of thinned sensors and ASICs
 - Industrial solution to prevent sparking
 - Layout and design of small pitch pixels
 - Cost effective large area production
- Sensor performance requirements at the HL-LHC result in huge synergies between the experiments
- No show stoppers!

Depletion voltage

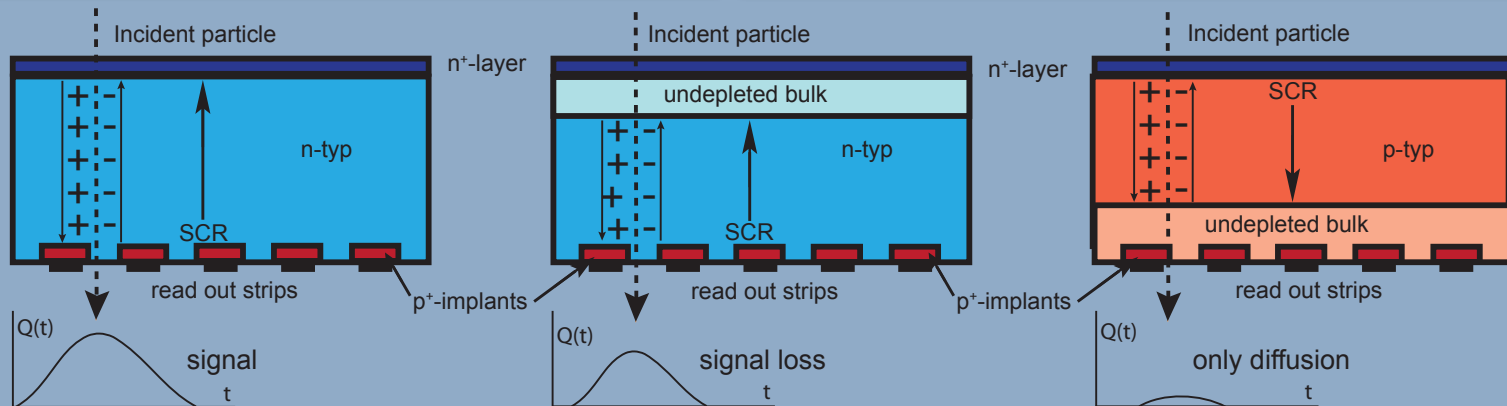
With particle fluence:



R. Wunsdorf, PhD thesis 1992, Uni Hamburg

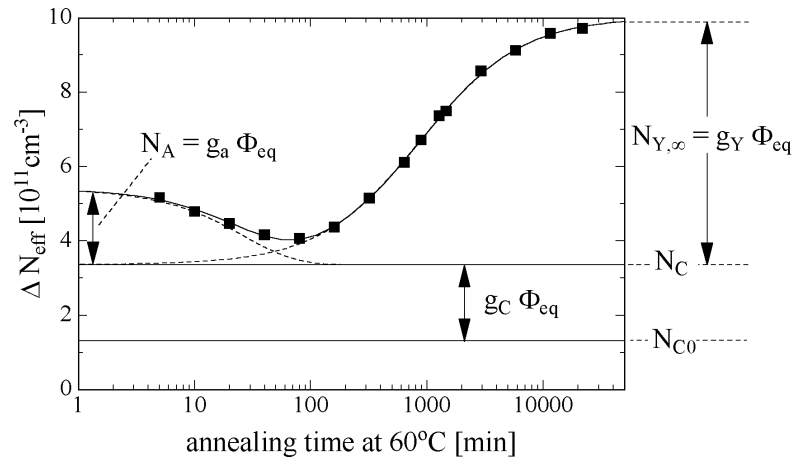
$$V_{dep} = \frac{q_0}{\epsilon \epsilon_0} \cdot |N_{eff}| \cdot d^2$$

- Acceptors compensate original doping
- Type inversion from n- to p-type
- Increase of depletion voltage after SCSi
→ Signal loss
- Annealing studies show impact of high T maintenance times



Depletion voltage

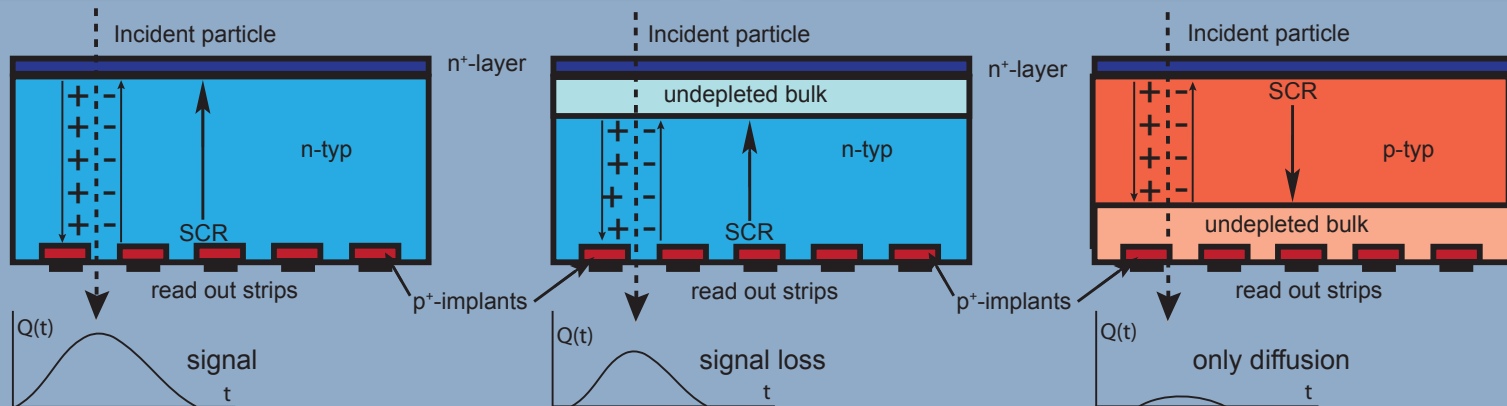
With annealing:



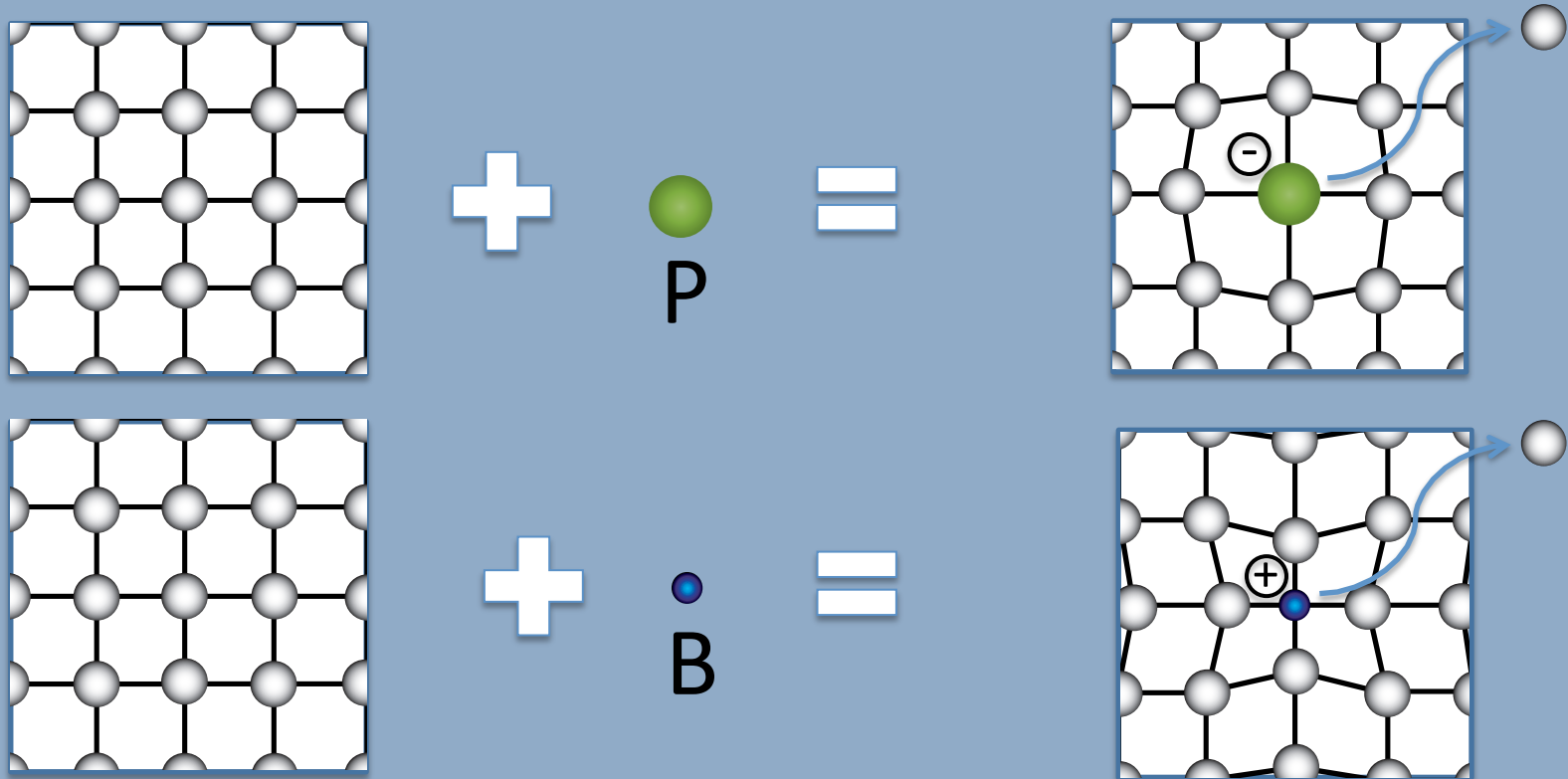
M. Moll, PhD thesis 1999, Uni Hamburg

$$V_{dep} = \frac{q_0}{\epsilon \epsilon_0} \cdot |N_{eff}| \cdot d^2$$

- Acceptors compensate original doping
- Type inversion from n- to p-type
- Increase of depletion voltage after SCS
- Signal loss
- Annealing studies show impact of high T maintenance times



Doping atoms are “defects” ...



...with desired impact on the detector properties.

Surface and Bulk damage

Today's knowledge:

Surface defects in p-on-n sensors:

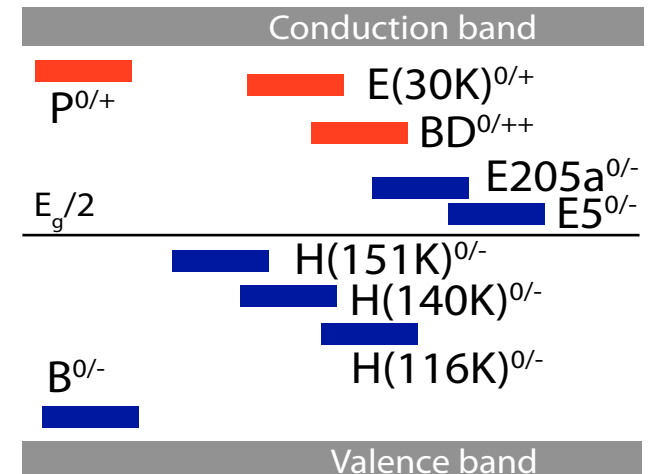
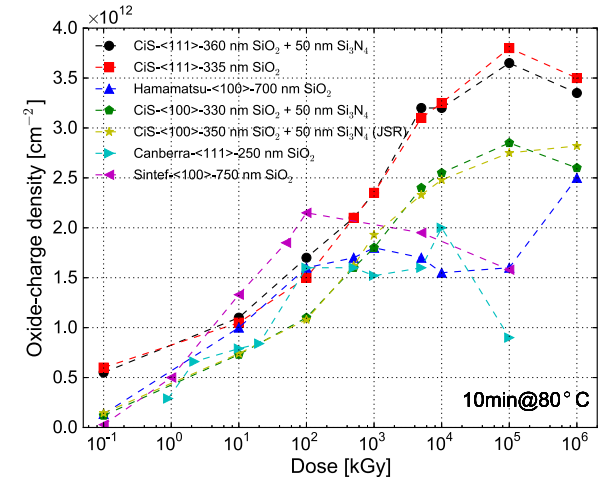
- Oxide-charges build-up from photons
- Some understanding of the generation of interface-states

→ Effective model for simulations

Bulk defects meanwhile also in n-on-p sensors:

- Leakage current scales with fluence, originates from cluster defects, mechanism not fully understood
 - Several bulk defects with impact on depletion voltage found, impact on space charge not fully understood
 - Some defects suspected to do trapping
- Several models with 2-, 3-, 5- levels ("free parameters") available for up to $\Phi=10^{15} \text{ cm}^{-2}$

Dose dependence of oxide-charge density



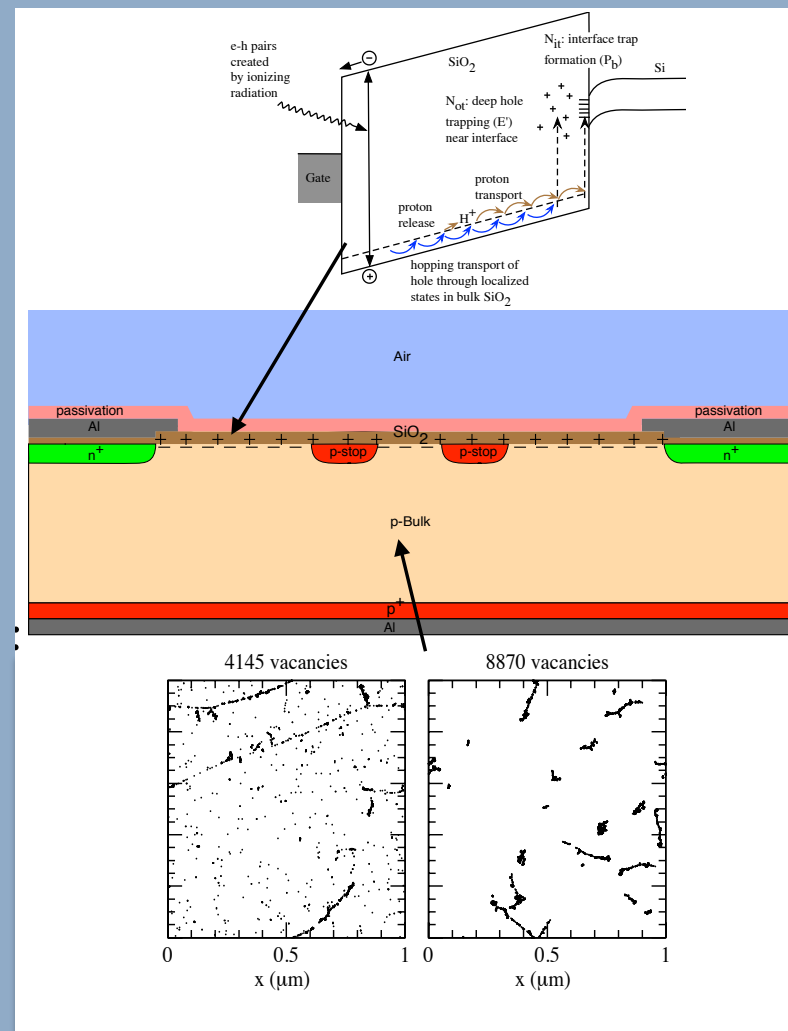
Impact of Radiation damage

Surface damage (Ionising Energy Loss):

- Increase of oxide charge
- Increase of interface traps
- ➔ Increase of leakage current
- ➔ Change of break-down voltage
- ➔ Change of charge collection

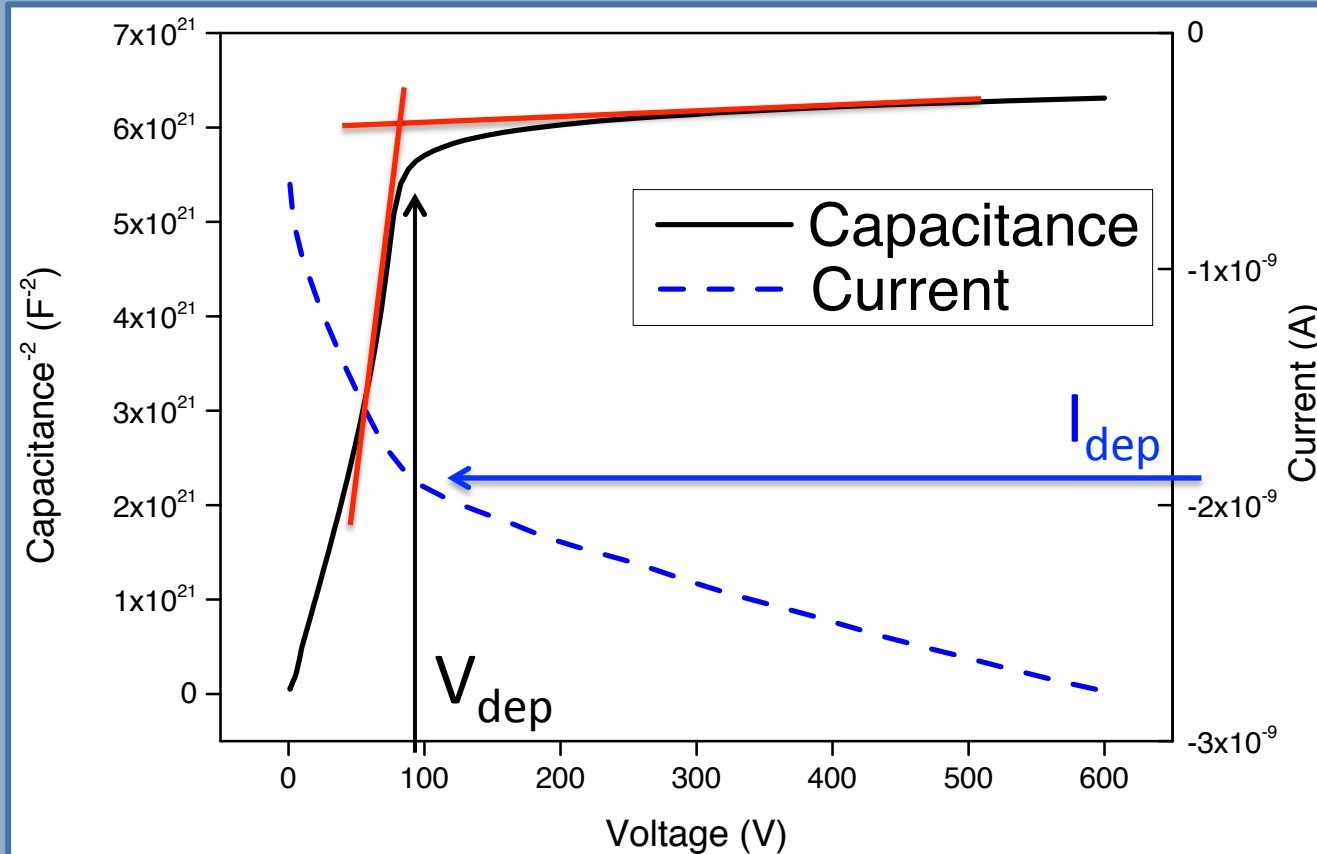
Bulk damage (Non-Ionising Energy Loss):

- Cluster and point defects
- ➔ Change of the space charge
- ➔ Change of depletion voltage
- ➔ Change of trapping



Extraction of sensor parameters

Capacitance-Voltage and Current-Voltage measurement



Capacitance measurement:

- 20 °C (10 kHz)
- 0 °C (at 1 kHz)
- -20 °C (at 1 kHz & 455 Hz)

→ Extract depletion voltage V_{dep}

→ Calculate:

$$N_{eff} = 2\epsilon\epsilon_0 V_{dep} / q_0 d^2$$

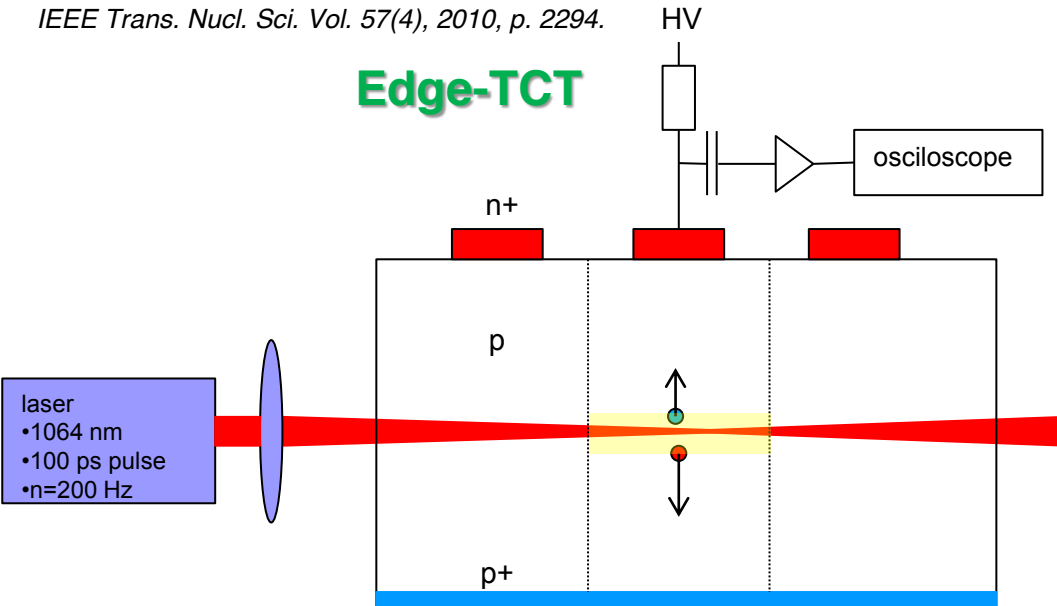
TCT techniques

TCT techniques

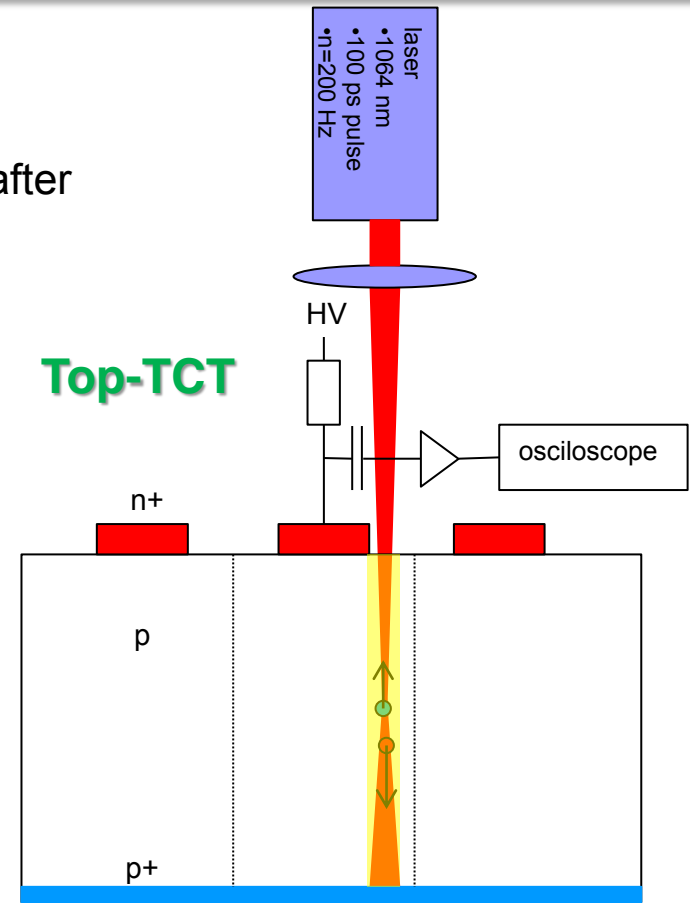
Measuring induced currents with fast current amplifiers after e-h generation with the laser pulse!

IEEE Trans. Nucl. Sci. Vol. 57(4), 2010, p. 2294.

Edge-TCT



Top-TCT



■ Probing the field in depth (average)

- Charge collection profile: $Q(y) = \int_0^{20ns} I(y, t) dt$
- Velocity profile: $I(y, t \sim 0) \propto (v_e + v_h)(y)$

■ Probing the lateral field (average)

- Properties of the mid-strip region
- Multiplication profiles
- Trapping induced charge sharing

G. Kramberger, Vertex 2012