Picosecond Photodetectors: What can we learn from modern III-V semiconductor technologies?

Serge Oktyabrsky

SUNY College of Nanoscale Science and Engineering, Albany NY
• CNSE brief overview
• Applications of ps UV photodetectors
• Vertical vs. Lateral field PDs
• Fast APDs
• How to make ps single-photoelectron counting detector?
• III-V technologies – challenges and breakthroughs
• Summary
CNSE OVERVIEW

Mr. Ross Goodman, Esq.
Assistant Vice President, Business Development and Economic Outreach
SUNY College of Nanoscale Science and Engineering
> 1,000,000 sq.ft. of cutting-edge facilities, with 135,000 sq. ft. of 300mm and 450 mm cleanrooms with a current expansion to 1,300,000 sq. ft.

- More than 300 industry partners including electronics, energy, defense & biohealth
- Over $17B investments and over 3,100 R&D jobs currently on site
CNSE’s STATEWIDE NANO IMPACT

- Canandaigua
  CNSE Smart System Technology & Commercialization Center (STC)

- Buffalo
  CNSE-AMRI-BNMC Medical Innovation and Commercialization Hub

- Rochester
  CNSE Photovoltaic Manufacturing and Technology Development Facility (CNSE MDF)

- Utica
  CNSE-SUNYIT Computer Chip Commercialization Center (QUAD-C)

- Halfmoon
  CNSE Solar Energy Development Center

- CNSE’s Albany NanoTech Complex

- Albany
  CNSE Smart Cities Technology Innovation (SCiTI) Center at Kiernan Plaza
CNSE is dedicated to nanotechnology with constellations in:

- Nanoscience
- Nanoengineering
- Nanobioscience
- Nanoeconomics

**Vision** Leverage combined resources to establish effective partnerships that will enable realization of *industry* technology roadmaps and pioneering nanoscale research.

**Mission** Create a financially and technically competitive environment to empower the nanoelectronics *industry* with manufacturing advantages through vertically integrated partnerships.
NYS Governor Cuomo Announces Global 450 Consortia

- $4.8 billion investment
  - $4.4 billion pledged by IBM, Intel, TSMC, GlobalFoundries, Samsung
  - $400 million pledged by NYS
- Intel to establish its East Coast headquarters in Albany to manage 450mm development.
- R&D in Albany, Canandaigua, Utica, East Fishkill and Yorktown Heights.
- 2,700 new high-tech jobs, including:
  - 800 at the CNSE
  - 400 in Utica
  - 1,500 construction jobs in Albany
CNSE Site Expansion
Applications for ultra-fast UV photodetectors:

- **High energy physics**
  - LAr and LXe detectors
  - Fast crystal calorimetry: many inorganic scintillators, i.e. BaF$_2$, emit in UV
  - Cherenkov detectors
- **Space research**
- **Medical TOF imaging and tomography**
  - TOF positron emission tomography
  - Fast gamma imaging/TOF tomography

**Scintillator emission**

$\Delta t \sim \text{average time between photons} = \text{jitter}$

$\Delta t = k \frac{\tau_{sc}}{N_{sc} K_{eff}}$

- $K_{eff}$ – system collection efficiency
- $\tau_{sc}$ – scintillator decay time
- $N_{sc}$ – scintillator photon yield
- $k \sim 1$ coefficient close to unity (statistics dependent)

**Example: Projected time resolution for TOF PET**

<table>
<thead>
<tr>
<th>Scintillator</th>
<th>Decay time (ns)</th>
<th>Light output (ph./MeV)</th>
<th>$\Delta t$ at $K_{eff}=0.2$ &amp; 0.5 MeV (ps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>LYSO</td>
<td>40</td>
<td>40,000</td>
<td>10</td>
</tr>
<tr>
<td>BaF$_2$ (fast component)</td>
<td>0.9</td>
<td>1400</td>
<td>6</td>
</tr>
<tr>
<td>LaBr$_3$ (Ce)</td>
<td>16</td>
<td>70,000</td>
<td>3</td>
</tr>
<tr>
<td>CsBr</td>
<td>0.07</td>
<td>20</td>
<td>35</td>
</tr>
</tbody>
</table>

Need: Semiconductor UV/Vis single photoelectron detector with ps resolution
Materials: Bulk Properties

Group III-V materials

Attractive material parameters are similar for MOSFETs and ultrafast PDs

300 K Electron Transport Properties

<table>
<thead>
<tr>
<th>Material</th>
<th>$E_g$, eV</th>
<th>$m_e(-)$</th>
<th>$m_e(-)$</th>
<th>$\mu_e$, cm²/Vs</th>
<th>$V_{e,sat}$, 10⁷ cm/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.12</td>
<td>0.19</td>
<td>0.98</td>
<td>1350</td>
<td>0.7</td>
</tr>
<tr>
<td>Ge</td>
<td>0.66</td>
<td>0.082</td>
<td>1.64</td>
<td>3900</td>
<td>0.7</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.42</td>
<td>0.067</td>
<td>-</td>
<td>8500</td>
<td>2</td>
</tr>
<tr>
<td>InP</td>
<td>1.35</td>
<td>0.079</td>
<td>-</td>
<td>5900</td>
<td>2.4</td>
</tr>
<tr>
<td>In₀.₅₃GaAs</td>
<td>0.8</td>
<td>0.04</td>
<td>-</td>
<td>14000</td>
<td>2.9</td>
</tr>
<tr>
<td>InAs</td>
<td>0.36</td>
<td>0.027</td>
<td>-</td>
<td>33000</td>
<td>3.5</td>
</tr>
<tr>
<td>GaSb</td>
<td>0.73</td>
<td>0.041</td>
<td>-</td>
<td>3750</td>
<td>0.8</td>
</tr>
<tr>
<td>InSb</td>
<td>0.17</td>
<td>0.013</td>
<td>-</td>
<td>77000</td>
<td>0.42</td>
</tr>
</tbody>
</table>

300 K Hole Transport Properties

<table>
<thead>
<tr>
<th>Material</th>
<th>$m_{hh}$</th>
<th>$m_h$</th>
<th>$m_{hh-in_pl}$</th>
<th>$\mu_h$, cm²/Vs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>0.54</td>
<td>0.15</td>
<td>0.22</td>
<td>460</td>
</tr>
<tr>
<td>Ge</td>
<td>0.34</td>
<td>0.043</td>
<td>0.057</td>
<td>1900</td>
</tr>
<tr>
<td>GaAs</td>
<td>0.53</td>
<td>0.08</td>
<td>0.11</td>
<td>400</td>
</tr>
<tr>
<td>InP</td>
<td>0.56</td>
<td>0.12</td>
<td>0.16</td>
<td>150</td>
</tr>
<tr>
<td>In₀.₅₃GaAs</td>
<td>0.36</td>
<td>0.041</td>
<td>0.052</td>
<td>400</td>
</tr>
<tr>
<td>InAs</td>
<td>0.4</td>
<td>0.026</td>
<td>0.035</td>
<td>450</td>
</tr>
<tr>
<td>GaSb</td>
<td>0.8</td>
<td>0.05</td>
<td>0.055</td>
<td>680</td>
</tr>
<tr>
<td>InSb</td>
<td>0.42</td>
<td>0.016</td>
<td>0.020</td>
<td>850</td>
</tr>
</tbody>
</table>
Materials: Saturation Velocity

**Saturation velocity and necessary operating voltage for 10ps risetime**

<table>
<thead>
<tr>
<th>Material</th>
<th>Saturation field, kV/cm</th>
<th>Spacing for 10ps, μm</th>
<th>Operating Voltage, V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>20</td>
<td>0.7</td>
<td>1.4</td>
</tr>
<tr>
<td>GaN</td>
<td>150</td>
<td>1.4</td>
<td>21*</td>
</tr>
<tr>
<td>GaAs</td>
<td>3.5</td>
<td>2</td>
<td>0.7</td>
</tr>
<tr>
<td>InP</td>
<td>12</td>
<td>2.3</td>
<td>2.6</td>
</tr>
<tr>
<td>InGaAs</td>
<td>5</td>
<td>3</td>
<td>1.5</td>
</tr>
</tbody>
</table>

* For GaN operating voltage should be further increased due to longer absorption lengths and lower mobility

**Saturation velocity – limited electron drift time (TOF)**

Experimental data from:
Absorption

Absorption coefficients in semiconductors
[Carruthers, Electro-Optics Handbook ]

- In the region $\lambda<360$nm the absorption takes place within $<100$ A
- Highly-doped layer in p-i-n or APD structures kills efficiency
- Evolution of carriers is strongly affected by the surface/interface recombination, relaxation in the Brillouin zone close to the surface
- Si has the highest $\alpha$ in UV and the lowest in visible $\rightarrow$ the worst material for fast PDs
- Detectors with lateral field are of great interest for (near)-UV
UV QE Enhancement in Si

Quantum efficiency of UV-enhanced (delta-doped) CCDs 4x4 µm² pixel [JPL]


- Making a thin inversion layer increases UV efficiency but also increases sheet resistance
- Sheet resistance is high ~10 kΩ/sq.
- Fine in slow devices, but series resistance kills leading front
**Geometry: Lateral vs. Vertical**

<table>
<thead>
<tr>
<th>Vertical (p-i-n)</th>
<th>Lateral (MSM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Large area contact, usually thin depletion layer, higher C</td>
<td>Small area contact, large gaps between electrodes, lower C</td>
</tr>
<tr>
<td>Surface dead layer due to top contact, bad for UV</td>
<td>No dead layer, large exposed surface, surface recombination</td>
</tr>
<tr>
<td>3D device, requires special packaging</td>
<td>Planar device, compatible with FET process, simple integration</td>
</tr>
<tr>
<td>Most common semiconductor detector type</td>
<td>Some designs commercially available, e.g. MSM’s or Si drift detectors</td>
</tr>
</tbody>
</table>

**Lateral:**
Both contacts on one surface
Field parallel to the surface

**Vertical:**
Top and bottom contacts
Field normal to the surface

**Silicon Drift Detector with integrated transistor**
[from PulseTor.com]
The simplest lateral field detector is MSM structure which is back-to-back connected Schottky diodes

Advantages
- Low capacitance per unit area
- Lack of dead contact layer (important to absorption coefficients $a > 10^6 \text{ cm}^{-1} \rightarrow 10\text{nm absorption length}$)
- Reduced volume for generation-related dark current (in particular QW structures)
- Planarity, compatibility with FET process flow

Disadvantages
- Reflection from surface metal contacts
- Surface states enhance generation/recombination, reduce efficiency and increase dark current
- Metal-semiconductor interface is the origin of traps and leakage
Metal-Semiconductor-Metal (MSM) PDs

Zeghbroeck et al., EDL 1988
GaAs MSM: 105 GHz, 5 ps (drift limited)

Chou et al., APL 1992
LT-GaAs MSM: 0.87 ps

Hamamatsu GaAs MSM
30 ps FWHM

Advanced Laser Diode Systems
InGaAs MSM: 20ps FWHMz
Capacitance of MSM device:

\[
C = \frac{K(k) \varepsilon_0 (\varepsilon + 1) A}{K(\sqrt{1-k^2}) 4(L+W)}
\]

\[
K(k) = \int_0^{\pi/2} \frac{d\phi}{\sqrt{1-k^2 \sin^2 \phi}}
\]

\[
k = \tan^2 \frac{\pi W}{4(L+W)}
\]

- MSM shows \(~5\times\) reduction of device capacitance (vs. pin) for the same drift length
- Capacitance reduction for the same TOF*: \(15\times\) as compared to Si p-i-n.

*TOF- Electron time-of-flight or drift time
• Shot noise is the major intrinsic noise source
\[
\langle i_{PD\_noise}^2 \rangle = \left( 2q I_{tot} + \frac{4kT}{R_{eq}} \right) \Delta f \xrightarrow{\text{small signal}} 2q I_{dark} \Delta f
\]

• Dark current in MSM is mostly due to thermionic emission over the Schottky barrier

\[ J_{thermionic} \sim T^2 \exp\left(-\frac{q \phi_B}{kT}\right) \]

• Use of a contact on higher bandgap semiconductor (AlGaAs or AlInAs) lowers the dark current

• The lowest dark current in InAlAs/InGaAs heterostructure

\[ 4.5 \times 10^{-6} \text{ A/cm}^2 \quad \text{[Kim et al. TED 51 351 (2004)]} \]

• Compare to \( 5 \times 10^{-11} \text{ A/cm}^2 \) for Si p-i-n PDs

**Dark current in GaAs MSM**

[Ito et al. JQE 22 1073 (1986)]

\[ 4.5 \times 10^{-6} \text{ A/cm}^2 \quad 4 \times 10^{-5} \text{ A/cm}^2 \]
Dark current in 1μm GaAs MSM and p-i-n diodes: effect of thermionic emission and generation

- A simple built-in heterojunction barrier close to Schottky contact can reduce current by 3-4 orders of magnitude to ~100 el/s-μm²
- It can be further reduced by introducing p-n junctions instead of Schottky junctions
- Feasible to have one heterojunction and another Schottky junction
- Then dark current is limited by generation current:

\[ I_{SHR} = qV_{depletion} \frac{n_i}{2\tau_o} \]
Dark currents in p-i-n PDs

**Dark current in Si p-i-n PD**

- S1227 series
- [hamamatsu.com](http://hamamatsu.com)
- Dark current = 0.1nA/cm²

**Dark current in GaAs p-i-n PD**

- [kyosemi.co.jp](http://kyosemi.co.jp)
- Dark current = 30nA/cm²

**Generation dark current in W=0.5 µm pin diodes**

<table>
<thead>
<tr>
<th>Material</th>
<th>$n_i$, cm⁻³</th>
<th>$\tau_{SHR}$, s</th>
<th>$J_{GR}$, A/cm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1.5x10¹⁰</td>
<td>10⁻³</td>
<td>6x10⁻¹¹</td>
</tr>
<tr>
<td>GaAs</td>
<td>1.8x10⁶</td>
<td>10⁻⁸</td>
<td>7x10⁻¹⁰</td>
</tr>
<tr>
<td>Al₀.₃GaAs</td>
<td>1.7x10³</td>
<td>10⁻¹⁰</td>
<td>7x10⁻¹¹</td>
</tr>
</tbody>
</table>

- Reverse current is ~2 orders of magnitude higher in GaAs than in Si p-i-n’s
- There are number of reports of lower reverse currents, i.e. ~50 pA/cm² in $p^+\text{-}p\text{-}n^+$ [Chen et al. J. Phys.D, 44 215303 (2011) ]
- Generation current is scaling as volume of the depletion region. Effective volume can be reduced in lateral structure

\[
J_{GR} \approx qW \frac{n_i}{2\tau_{SHR}}
\]
Si APDs: State-of-the-Art

From D. Hitlin, CalTech/RMD/JPL, 2013

Reaching Through Avalanche Photodiode (RTAPD)

Reverse biased photodiode with $p^+\pi p n^+$ structure

- Avalanche gain in $pn^+$ junction
- Electric field drives electrons toward junction
- Deep implant
  - UV QE Low, unstable

No background rejection

Signal 220 nm

Background 330 nm

Dead layer formed by $p^+$ implant

Avalanche gain

Drift: velocity 10 ps/μm

Absorption

Multiplication

Recombination

Total light output: $1.2 \times 10^4$ photons/MeV

85% 650 ns

15% 900 ps

RMD 9x9mm
RMD SSPM: 130 fF/pixel (pixel size ~50μm)

SSPM: APD array in parallel

[From: “Scintillation Detectors”, U. of Heidelberg]

• Geiger-mode: Gain ~10^6
• ns-range device: best jitter ~100ps

KETEC SSPM

AdvanSiD SSPM

Hamamatsu SSPM: S12571

[From hamamatsu.com]
State of the art: Digital SiPM

Philips Digital SSPM

[From: www.research.philips.com and PDPC presentation, 2012]

- Digital SiPM: each pixel contains its own electronics
- Low parasitic capacitance → reduced gain → improved stability
• Multiple transits in APDs reduce speed (multiplication buildup time)
• Geiger mode does not provide benefits
• Multiplication length can be reduced to >100nm to increase speed
• Demonstrated gain-bandwidth product ~300-400 GHz
Fast APDs: S/N for single photoelectron detection

Dependent parameters:

- Fixed rise time $\tau$ limits multiplication $M$ (fixed GBP)
- Multiplication $M$ determines total charge at amplifier input
- Signal voltage determined by charging the capacitor
- Noise of an amplifier input determines maximum capacitance

Limited room for variations!
- Capacitances of $\sim 10$ fF are needed to obtain reasonable S/N ratio at low $M$’s
- Need for low-C integration of the PD with amplifier $\rightarrow$ monolithic integration

For single photoelectron detection for GBP= 300 GHz

$$V_{ph} = \frac{I_{ph} \tau}{C} \quad \text{single p.e.} \quad \frac{Me}{C}$$

$$R_{eq} C << \tau$$

$$v_{noise}^2 = 4\pi kT R_{eq} \Delta f$$

For $S/N = 1$:
- $M=20$
- $C=20$ fF
Improvement of APD noise: \( \text{Al}_{0.8}\text{Ga}_{0.2}\text{As/GaAs} \)

Excess noise in III-V APDs
[Xi, PhD thesis U. Sheffield, 2012]

Comparison of \( \text{Al}_{0.8}\text{Ga}_{0.2}\text{As} \) and commercial InP APDs
[from J. David, U. Sheffield, 2003]

- Commercial InP-based APD give excess noise of \( k_i \approx 0.7 \)
- Much lower excess noise can be obtained with wider bandgap III-V’s, e.g. \( \text{Al}_{0.8}\text{Ga}_{0.2}\text{As} \) as avalanche medium

\[ \text{Excess noise factor, } F \]
\[ \text{Avalanche region width, } w \ (\mu \text{m}) \]

\[ \text{ENF} = \kappa M + \left( 2 - \frac{1}{M} \right) (1 - \kappa) \]

Commerical InP-based APD
Fujitsu VN206
Concept for ps APD

Variable bandgap AlGaSb to collect photocarriers

Al$_2$O$_3$ passivation and AR layer

Schottky or $p^+$ junction

Small volume to reduce generation noise current

$n^+$-GaAs/AlGaAs superlattice to reduce excess noise

Small cross-section to reduce capacitance and dark current

$p^+$- field buffer

Trench or implant isolation

Semi-insulating substrate and buffer to reduce parasitic capacitance and leakage
Integration with a transistor amplifier:

- FET uses same basic technology
- Possibly uses same QW as a photodetector
- Area separated by insulating trench or implant within the same pixel
- Integration of planar detector with FET previously demonstrated

Integration of GaAs MSM with MESFET
[Ito et al. APL 47 1129 (1985) ]

Integration of InGaAs MSM with HEMT
[Kato, TMTT 47 1265 (1999) ]
Finally: Partitioning and Integration with electronics (Si)

**Face-up mounting** of thinned GaAs wafer to Si
- Larger openings to run conductors to Si
- Still front side illumination
- Lost system area for electrical connections

**Face down (flip-chip)**
- Established technology using solder bumps, e.g. for FPAs
- Backfill with polymer for mechanical stability
- Minimizes interconnect problem
- Requires precise substrate removal: oxidation lift-off
III-V MOSFETs (and FinFETs) is extremely hot and fast developing topic pursued by many IC manufactures: INTEL, GlobalFoundries, IBM, TSMC, Samsung…

Tool manufactures (AMAT, TEL,… and pilot IC R&D’s (Sematech, IMEC) are adapting existing Si technologies / toolsets for III-V’s

INTEL InGaAs FinFET (2010)

IMEC’s InGaAs FinFET (2013)
Aixtron 300mm MOCVD tool for III-V on silicon processes

300 mm Si wafer and shower-head

Integration on Si: from R. Hill, Sematech 2013

Aixtron G5 HT MOCVD* system operated by SEMATECH and CNSE:

- III-As and III-N growths
- MO and hydride precursors
- In-situ cleaning

* MOCVD – metal-organic chemical vapor deposition
Molecular Beam Epitaxy (MBE) Laboratory

- MBE Veeco Gen II system:
  - Duo-chamber MBE system for As- and Sb-based III-V’s
  - Triple-magnetron sputtering chamber (HfO₂, TaN, TiW)
  - Reactive e-beam evaporator (HfO₂ and Al₂O₃)
Compound Semiconductor Materials and Devices: Examples

Shape-engineered QD

2ML AIAs

Materials/Technologies
- MBE III-As and III-Sb
- Entire in-house processing
- Heterostructures
- In-situ (UHV):
  - High-k oxides
  - Contacts and Metallization

Quantum dots – related application
- Tunnel-coupled QD-QW VCSEL
- QD SLED for OCT
- Media with controlled photo-electron kinetics

Electronic devices
III-V high-k MOSFETs
- In-situ high-k oxide for n-MOSFET
- High-mobility p-MOSFET
- Regrown source/drain

HfO$_2$/InGaAs with $\Delta$ In$_0.5$GaAs

Photonic devices
- Cavity optical decoupling approach: duo-cavity VCSEL-modulator
- Q-switching with intracavity modulator
- Bragg MQW lattice
- QWIPs/QDIPs
- QD solar cells

VCSEL-Modulator

InGaAs 3 nm

10Gb/s eye diagram

45ps FWHM Q-switch pulse generation

Shape-engineered QD

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- Q-switching with intracavity modulator
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- QD solar cells

VCSEL-Modulator

InGaAs 3 nm

10Gb/s eye diagram

45ps FWHM Q-switch pulse generation
High-k oxide:
- High quality interface with dielectric (as SiO$_2$/Si):
  - Low surface recombination rate
  - Low density of interface states
  - High thermal and chemical stability of the interface

Improvement of channel transport:
- Low mass: Scattering – Coulomb, roughness, remote soft phonons
- Buried channel

S-D resistance:
- Regrown InAs for n-type or InSb on p-type
- Epi-SD and gate-last flow

From Weber et al. SSE 2006
GaAs/high-k Interfaces: Surface recombination

RT Photoluminescence and Internal Efficiency of GaAs with Different Surfaces
[Passlack, in “Materials Fundamentals of Gate Dielectrics…” 2005]

- Air exposed surface has high recombination velocity → kills photocarriers
- Great (~4-5 orders) reduction of the surface recombination demonstrated with various passivation techniques
a-Si Interface Passivation of High-k/GaAs interface

1.5 nm a-Si on GaAs + PVD HfO₂
Angle-resolved As 2p XPS spectra and CV's

Fermi level is pinned

Fermi level is not pinned

Wallace and Vogel groups, UTD
Removal of As-O with a-Si deposition

As-oxide not detectable after 20 sec of Si exposure

Eff. mobility vs. different passivation

Koveshnikov, APL 88, 022106 (2006)

Hinkle, APL 92, 071901 (2008)
Milojevic, APL 93, 202902, 252905 (2008)
Sonnet. Microel. Eng. 88,1083 (2011)
ALD Al₂O₃: “TMA Self-Cleaning”

UHV STM and STS of TMA-exposed InGaAs surface (Kummel group, UCSD)

In-situ XPS and C-V (Wallace and Vogel groups, UTD)

- Saturation dose of TMA results in a near monolayer coverage with no substrate atom displacement
- TMA dosing restores the Fermi level to the CB edge

Kummel ISAGST (2011)

- TMA is efficient to remove Ga- and As-oxides
- As-As dimers is the major component left

Wang Microel. Eng. 88, 1061 (2011)
HfO$_2$/a-Si/GaAs High-k Gate Stack

**TEM of the Gate Stack**

- **2.5 nm a-Si IPL**

- **GaAs**
- **SiO$_2$**
- **HfO$_2$**
- **TaN**

- **As/Si~0.3 alloying**
- **Part of Si layer is oxidized**

**a-Si scaling (10nm HfO$_2$)**

- Capacitance vs. Gate Voltage

**HfO$_2$ scaling (1.5 nm a-Si)**

- Capacitance vs. HfO$_2$ Thickness

- EOT vs. HfO$_2$ Thickness

- K = 21.7

**Notes:**
- The k-value of the HfO$_2$ gate oxide ~21-22
**III-V Processing**

**E-beam lithography process for FinFET fabrication**

- **E-beam exposure using Vistec VB 300**
  - NEB and HSQ negative resists: Fin Width down to 50 nm
- **Plasma etching of hard mask pattern into InGaAs**
  - CH₄/H₂/Ar recipe optimized for smooth, vertical sidewalls
  - Damage removal with diluted piranha wet etch
Ion Damage Removal

RIE damage removal after CH₄/H₂/Ar etch

• 1μm n-In₀.₅₃GaAs on n-GaAs MOS Capacitor
• Diluted Piranha = similar CV to as-grown surface
• CV characteristics restored

![Capacitance-Voltage plots for different etching processes]
• Gate-last flow MOSFET with epi $p^+$-GaSb SD and InAs etch stop layer
• After TMAH recess etch, InAs (1.5nm) is present on the surface
Oxidation Lift-off Technology

**Oxidation lift-off**

- Bonding by Au-Ge eutectic or polymer
- Bonding, device separation and formation of the oxide isolation in the same process

FIB cross-sections of the device fabricated by oxidation lift-off technique.
Conclusions

• Group III-V technologies are rapidly progressing towards mainstream logic ICs

• III-V materials have credible benefits for photodetectors:
  • High carrier velocity,
  • Low saturation field

• Planar lateral field architecture is beneficial for fast UV PD
  • Low capacitance
  • Transport close to the surface
  • Reduced volume for current

• Materials benefits + Available technologies => ps PDs?
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