

# **Development and fabrication of full 3D-sensors at SINTEF MiNaLab**

**FNAL October 21, 2009**

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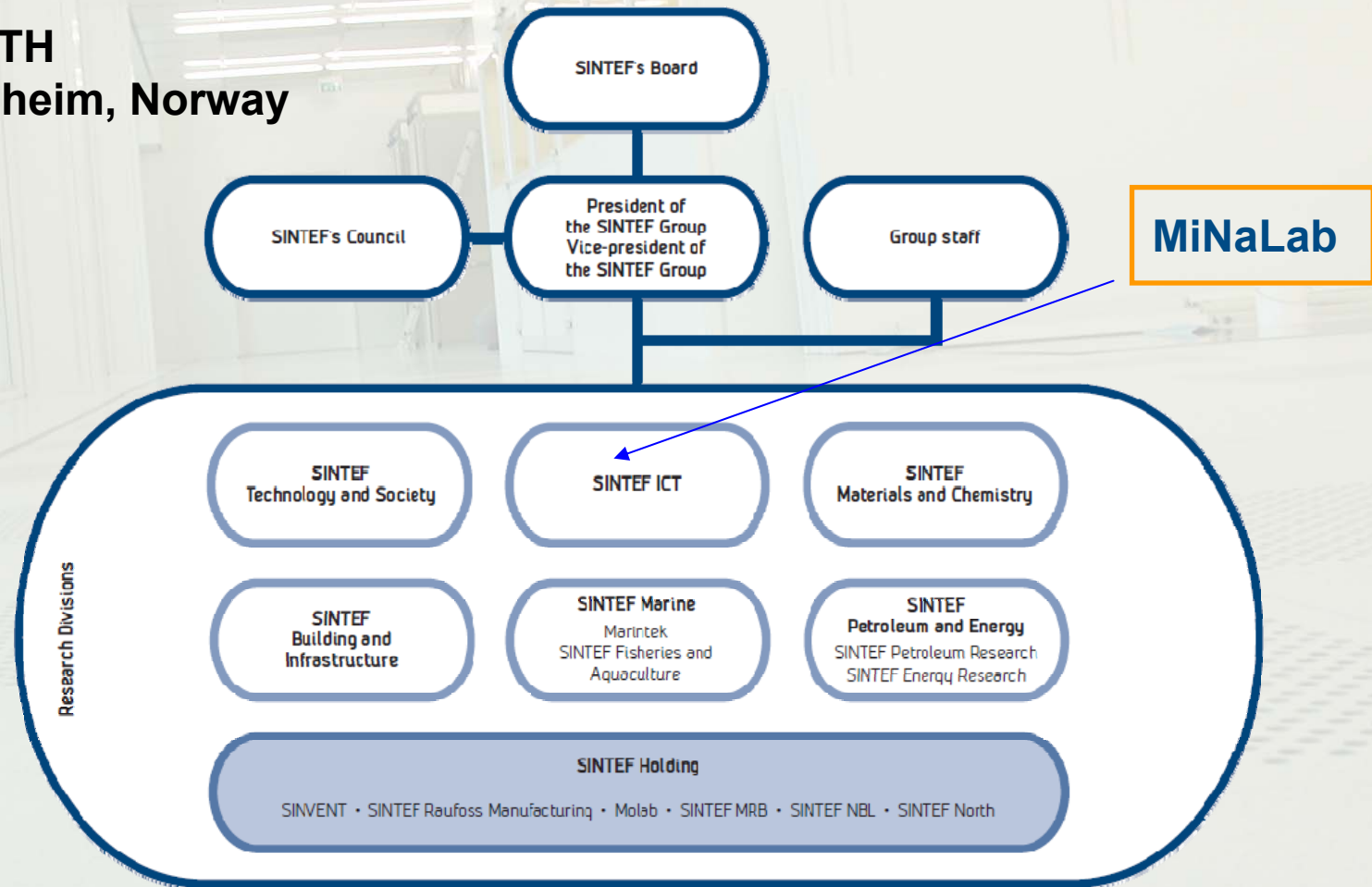
# Outline

- Short (2 minutes?) presentation of SINTEF and MiNaLab
- 3D structures
- Principle of operation, advantages and disadvantages
- Motivation for 3D-detector activity and SINTEF involvement
- Fabrication tools and technology issues
- Wafer layout and results from SINTEF first 3D-run
- Technology improvements, wafer layout, and results from second run
- Conclusions and further work



## Independent applied research foundation

Founded 1950 at NTH  
Headquarter Trondheim, Norway  
2100 employees  
Turnover 2008:  
NOK 2.6 billion  
(USD 470 millions)



# MiNaLab (Micro- and Nanotechnology Laboratory in Oslo)



- Moved into new lab in 2005
- Shared facility with the University of Oslo  
Two separate clean room floors:  
SINTEF: 800 m<sup>2</sup>  
University of Oslo: 600 m<sup>2</sup>
- SINTEF:
  - Silicon line with annual capacity of 10.000 6-inch wafers on one shift, 4 layer process
  - 4-inch and 6-inch wafers
- Situated on the University of Oslo campus.

## MiNaLab

- Net turnover 2007: NOK 53.4 millions (~ USD 9.6 millions)
- Net turnover 2008: NOK 58.3 millions (~ USD 10.5 millions)
- Employees: 39
  - Scientists: 28 (16 with PhD)
  - Engineers: 11
- QA system approved to ISO 9001:2008
- R&D areas:
  - Radiation sensors (includes wafer production and foundry service)
  - MEMS sensors and actuators
  - Micro - fluidics
  - Micro - optics (diffractive optics)
  - Active materials (MEMS with piezo-electric PZT)

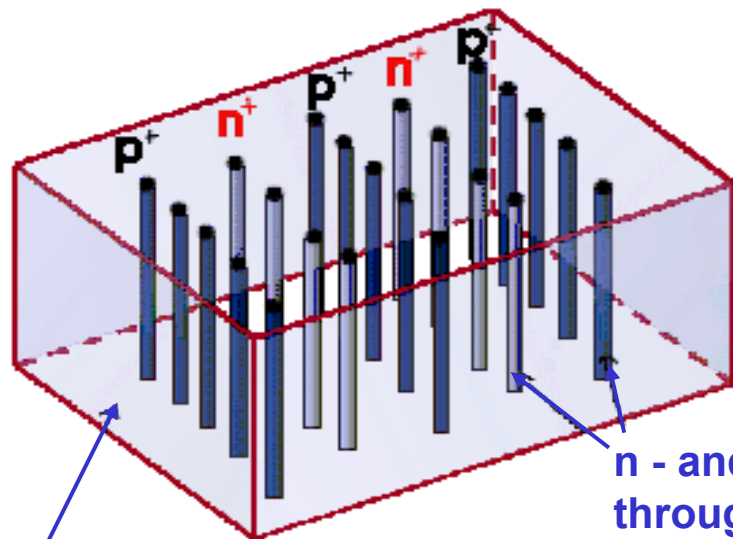
# SINTEF Device configuration

## Full 3-D Structure with active edges

Previously only made at Stanford

3-D silicon detectors proposed by S. Parker in 1995

Active edge proposed by C. Kenney in 1997



Silicon chip (200 to 300  $\mu\text{m}$  thick)

n - and p - electrode holes penetrating through chip. Completely filled with doped poly-silicon

p - active edge trench filled with doped poly-silicon

### Advantages:

1. Active edge which makes chip sensitive right up to physical edge
2. Poly-silicon filling makes electrodes sensitive (50 to 60 % efficiency)

### Disadvantages:

1. Short inter-electrode distance implies high capacitance
2. Cost

# Main fabrication steps

## Modification of Stanford Process (S. Parker, C. Kenney)

IEEE Trans Nucl Sci 464 (1999) 1224

IEEE Trans Nucl Sci 482 (2001) 189

**P-spray implant**

**Oxidation**

**Wafer bonding**

**2 DRIE steps**

**2 Poly-silicon deposition steps**

- Readout Electrodes
- Bias Electrodes and Trench

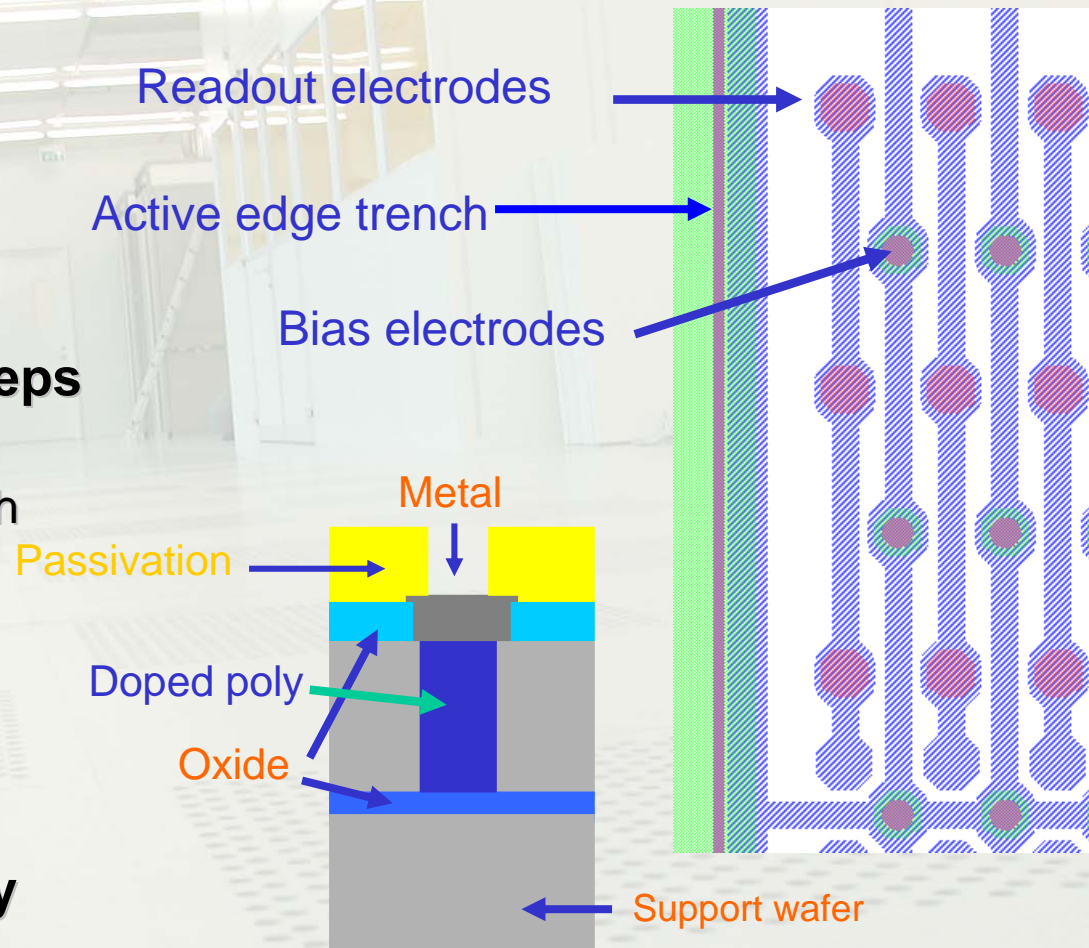
**RIE poly-silicon back etch**

**Contact holes**

**Metal**

**Passivation**

**7 layers of photolithography**



# Alternative 3D –configurations

Double sided processing

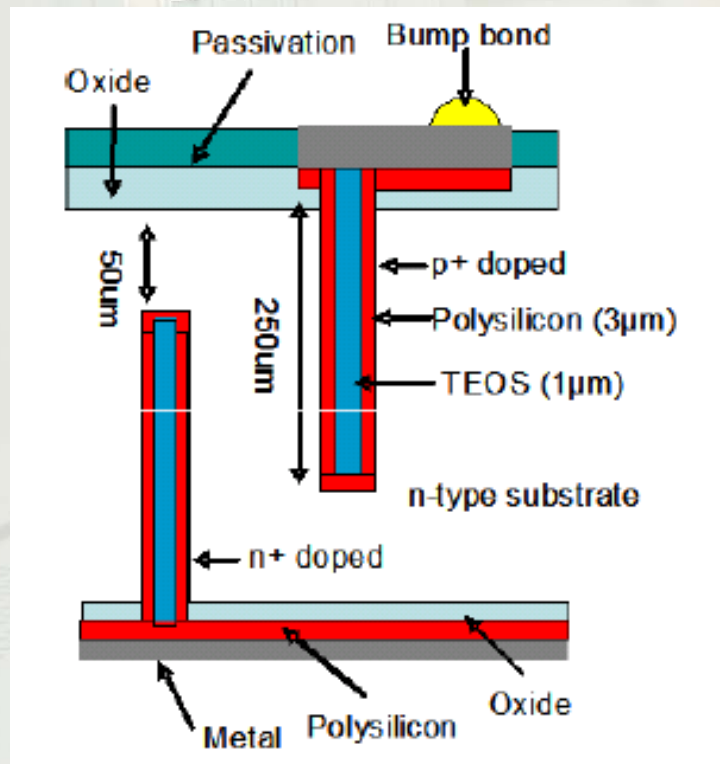
No active edge, less sensitive area

Open (insensitive) electrodes

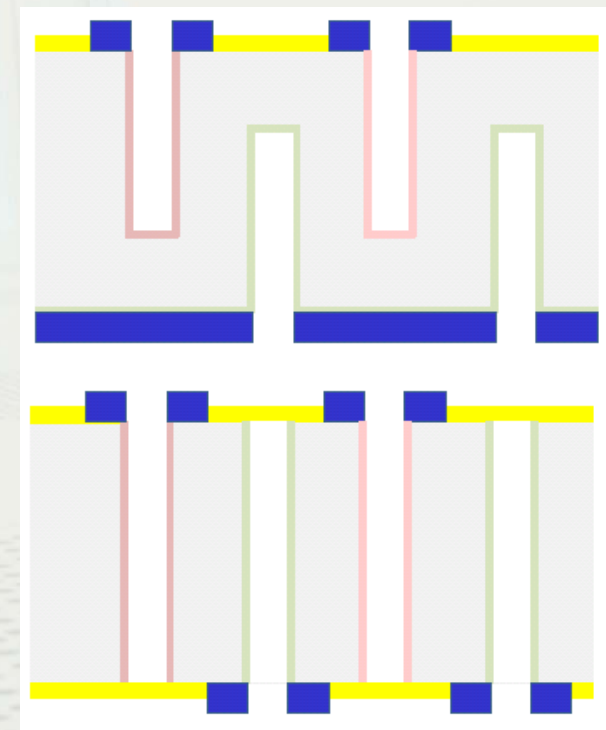
Distorted electric field distribution

Simpler processing?

No support wafer



CNM Barcelona

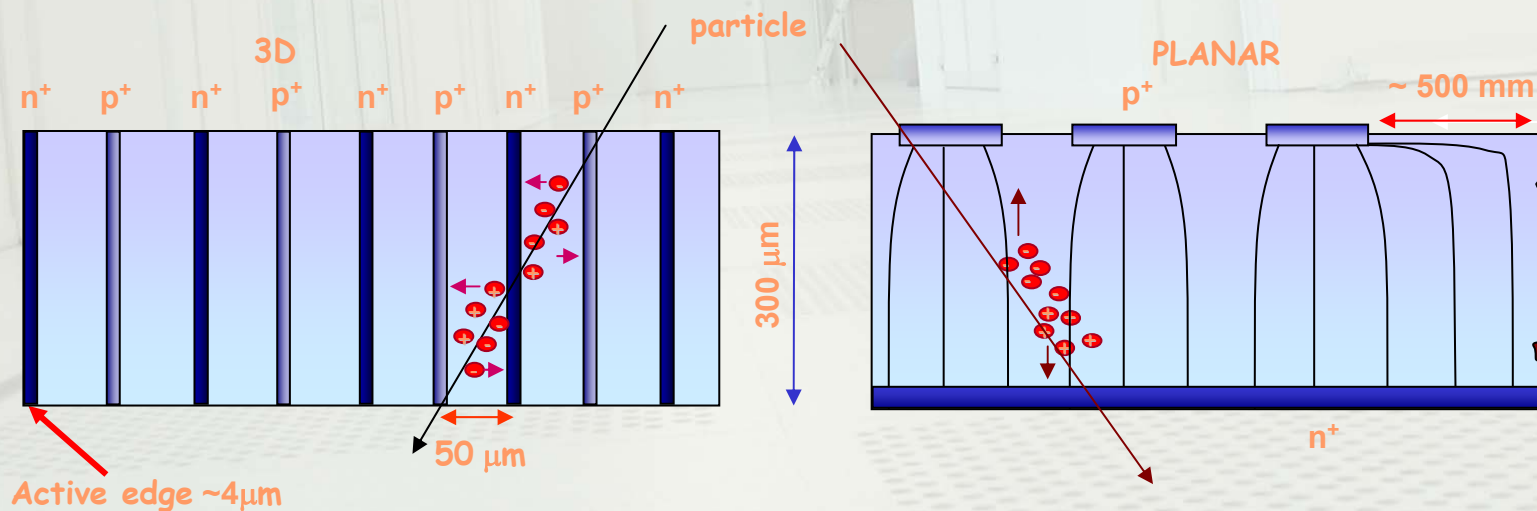


FBK Trento



# PROPERTIES OF 3D SENSORS

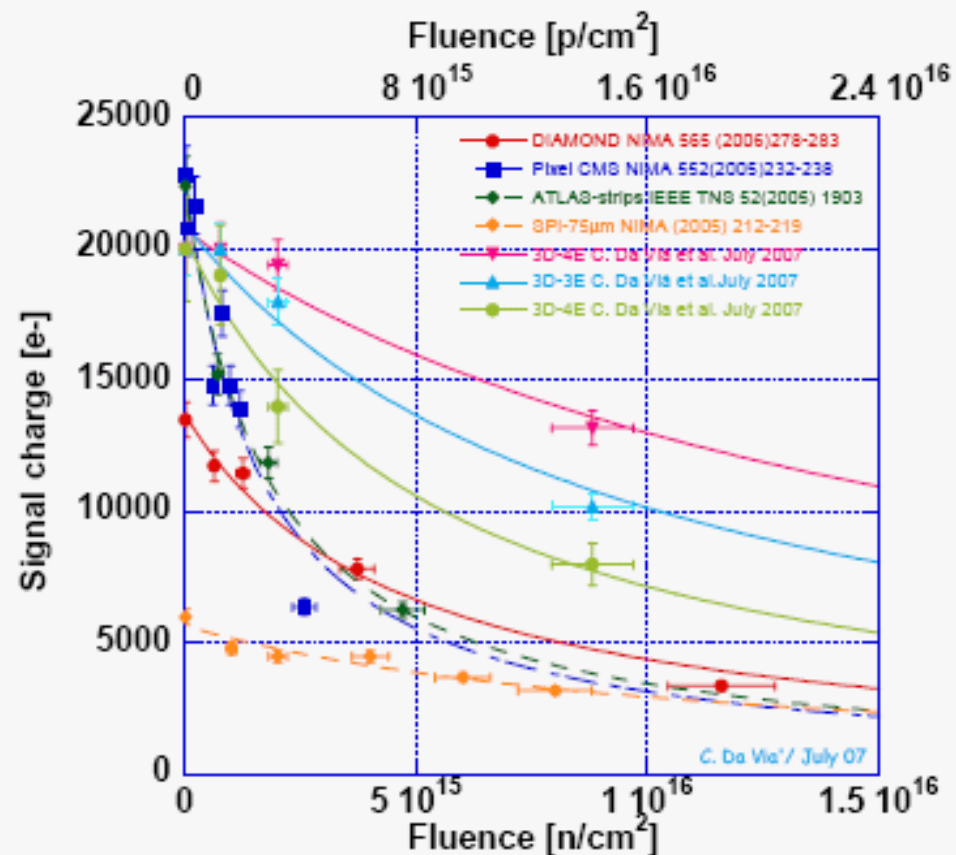
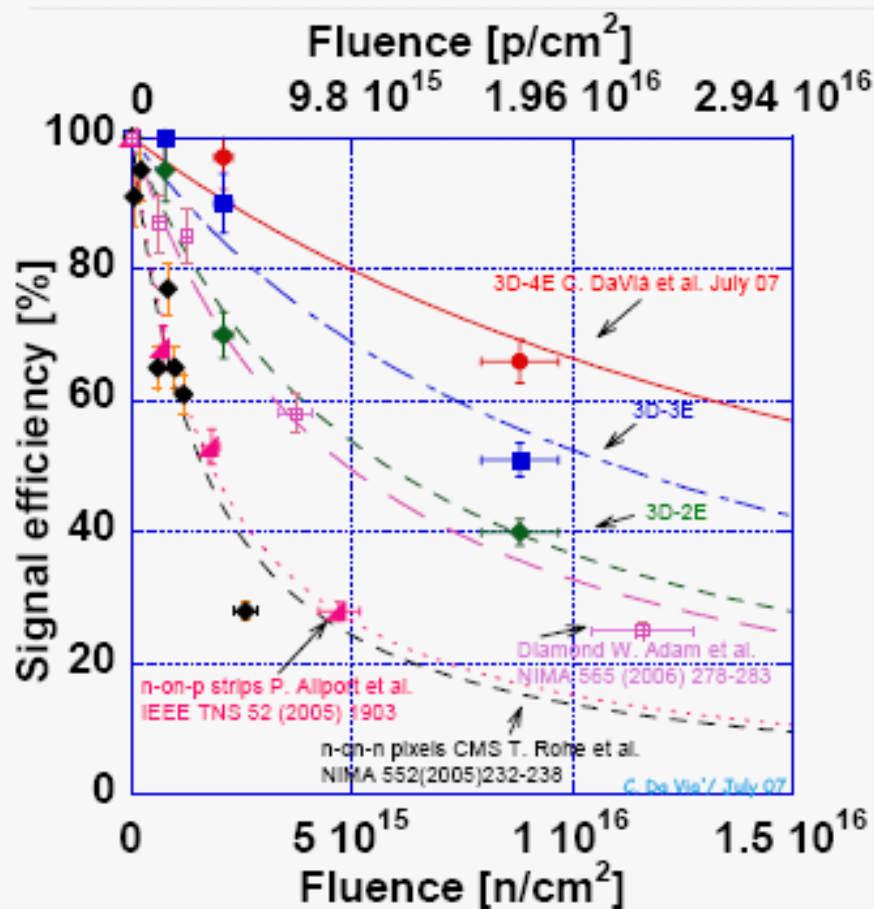
- ❑ Almost same charge generation as planar sensor with same thickness
- ❑ Carrier drift length independent of chip thickness ( $\geq 45 \mu\text{m}$ ).
- ❑ Short drift length implies high radiation hardness and fast response.
- ❑ Active edge secures sensitivity up to chip edge.



S. Parker, C. Kenney, J. Segal,  
NIM A395 (1997) 328-343.

# Signal versus fluence compilation

Silicon biased at  $\sim 2.2V/\mu m$   
 Diamond biased at  $1V/\mu m$



**S/N is the relevant parameter at the end. It depends not only on the signal, but also on the front end electronics and sensor capacitance.**

## Motivation for SINTEF to join 3D-collaboration

- The 3D-collaboration now includes Univ. of Manchester, Univ. of Hawaii, SLAC, Purdue Univ., Oslo Univ., CNM-Barcelona, FBK-Trento, SINTEF. Prague Technical Univ. is associated member
- SINTEF joined 3D-collaboration in 2006. Part of effort to transfer 3D technology to affordable(?) small and medium scale production
  - Processing line adapted to sensor fabrication. Experience in sensor technology since early 1980ties. Automatic and semiautomatic tools
  - Number of in-house state-of-art Deep Reactive Ion Etchers (DRIE)
  - Long experience in 3D silicon micromachining (MEMS applications)

# Fundamental Tool for 3D - Detectors: Deep Reactive Ion Etcher (DRIE)

Tools at SINTEF:

AMS200#1  
“DIRTY HARRY”

AMS200# 2  
“ OLDBOY”

AMS200 ISPEEDER  
“IPROD”

State-of-art  
Alcatel ICP tools

Bosch process with  
subsequent etching  
and deposition of  
polymer

“Old boy” and  
“IPROD” with robot



**“IPROD” (Alcatel AMS 200 ISPEEDER) commissioned beginning of 2008.**

Used in SINTEF 2<sup>nd</sup> 3D run.

About 4x throughput compared to “Old Boy” used in first run.

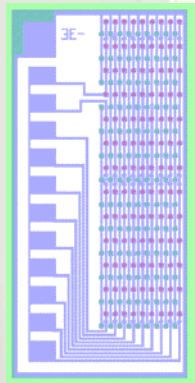
Can be operated with both low and high frequency chuck bias.

Low frequency bias reduces and/or removes notching problems

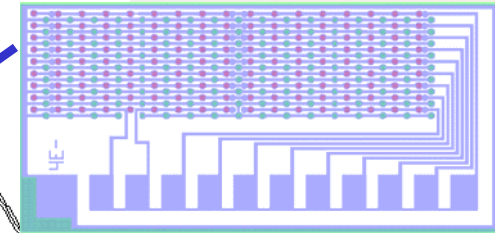
## First 3D development run at SINTEF

- Started mid December 2006, completed February 2008. Included several very time consuming process developments
- Original photo mask design by Chris Kenney with ATLAS pixel layout, slightly modified by SINTEF
- N-type wafers, 4-inch, 250  $\mu\text{m}$  thick, specific resistivity 1500 to 2000  $\Omega\text{cm}$ . Not optimal configuration for n-readout as active edge is part of total chip pn-junction
- Limitation at SINTEF:  
Polysilicon filling have to be performed at Stanford. SINTEF LPCVD is restricted to deposition of  $\leq 1\mu\text{m}$

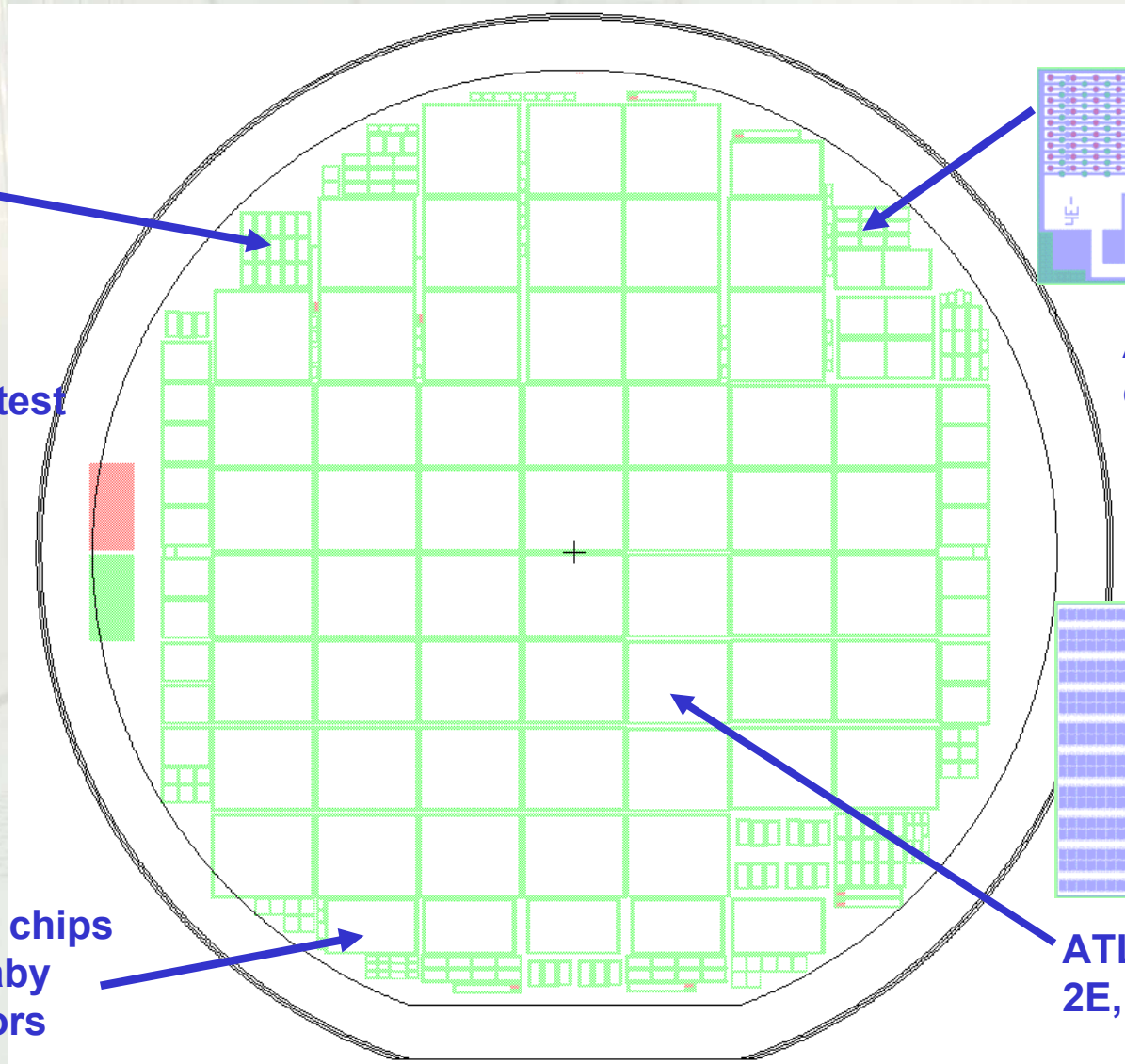
# ATLAS 3-D Pixel – Wafer Layout: Designed by C Kenney, modified by SINTEF



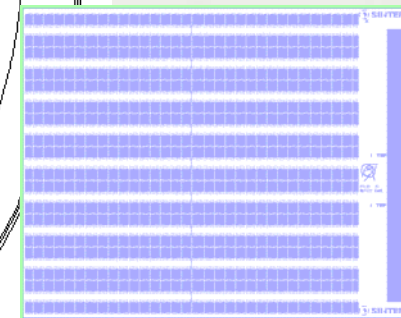
ATLAS pixel test chips



ATLAS pixel test chips



Various test chips including baby strip detectors



ATLAS FE-I3 chips, 2E, 3E, 4E – config.

# ATLAS pixels: 4E -, 3E -, 2E – configurations

2.nd run also included 1E and 5E configurations

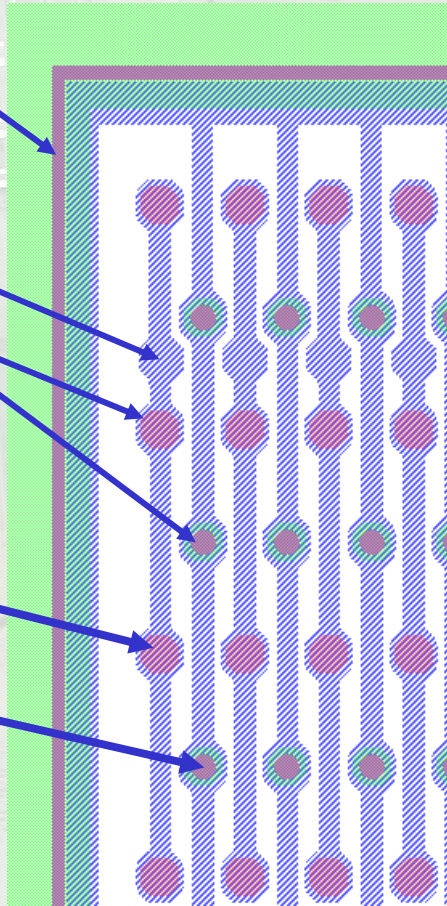
4 or 7  $\mu\text{m}$  trench  
(active edge)

pad for  
bump-bonding

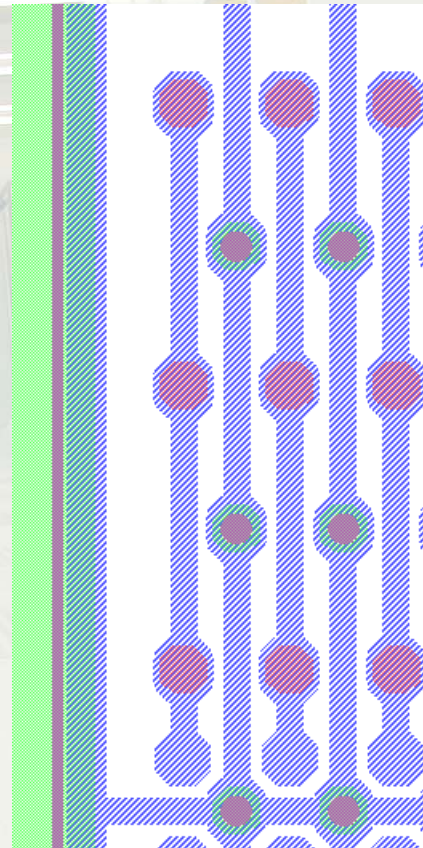
14 $\mu\text{m}$  holes

n-readout  
electrodes

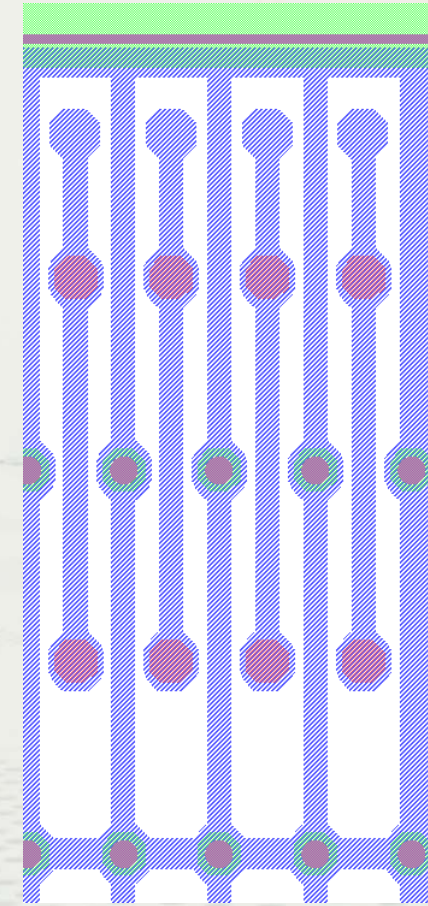
p-bias  
electrodes



4 electrodes per  
pixel – 4E

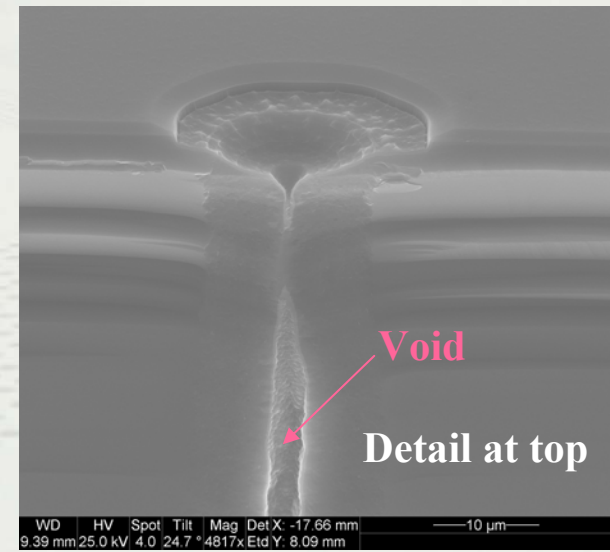
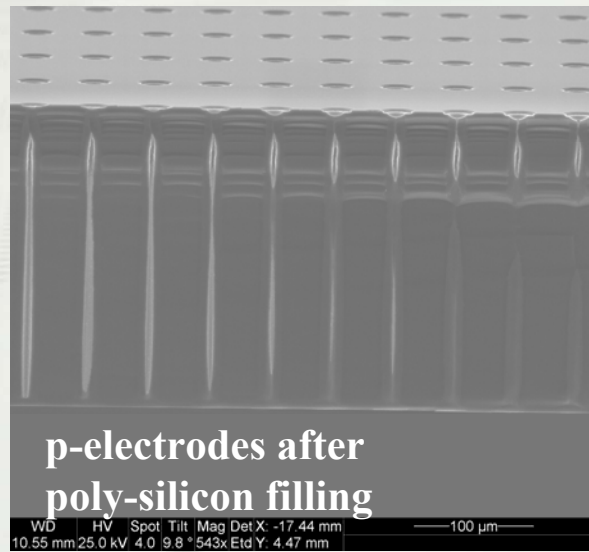
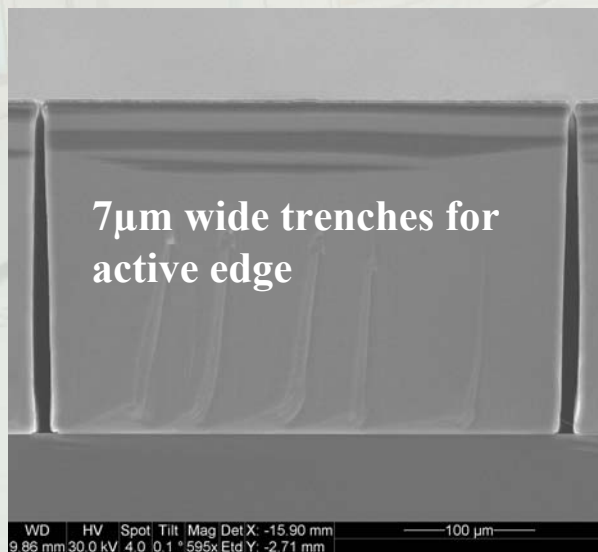
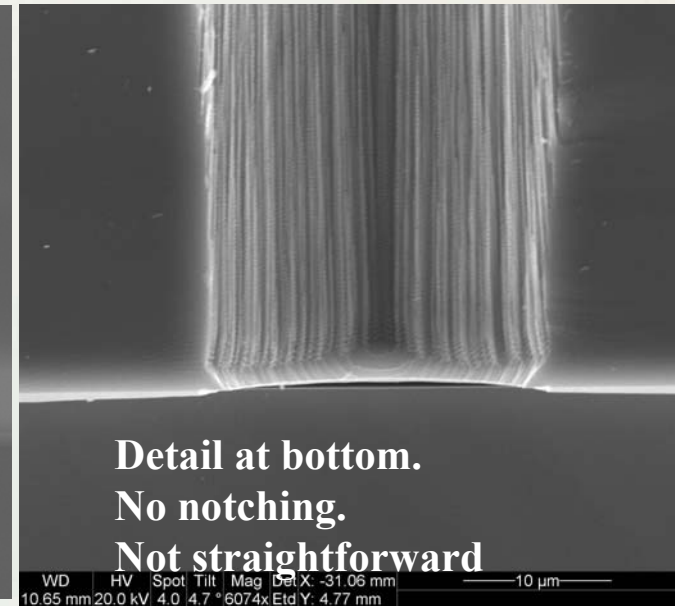
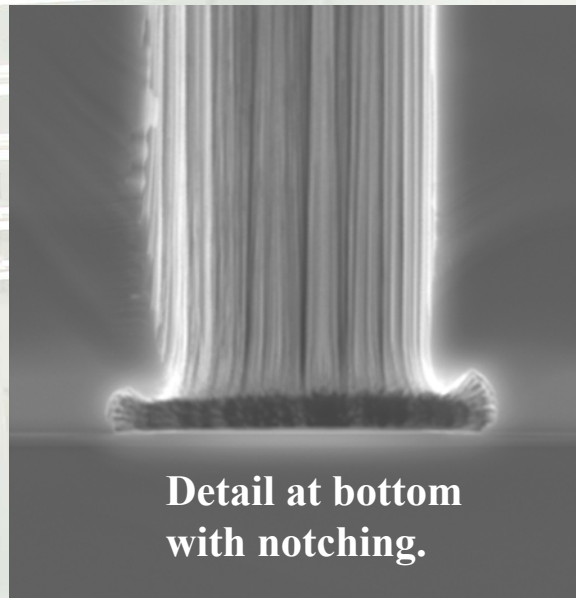
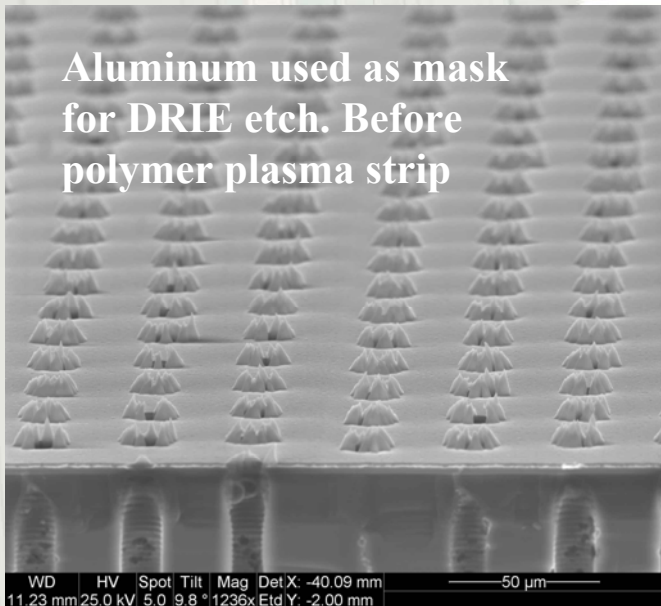


3 electrodes per  
pixel – 3E



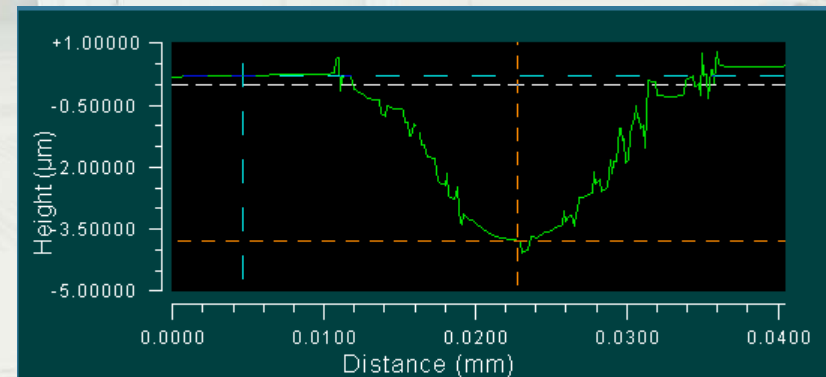
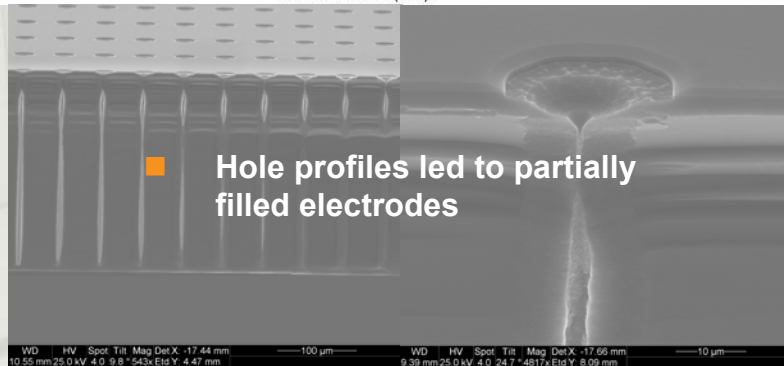
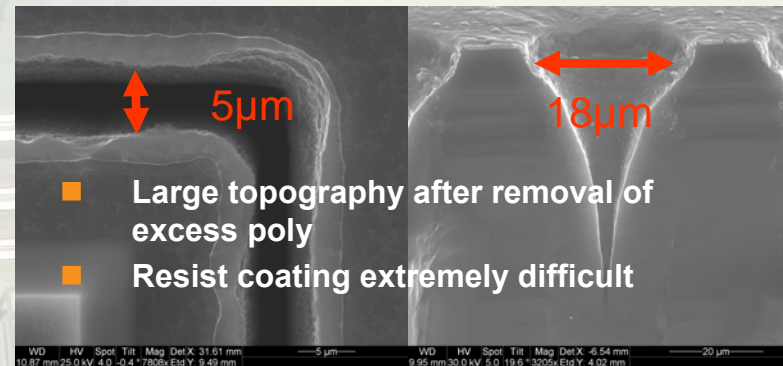
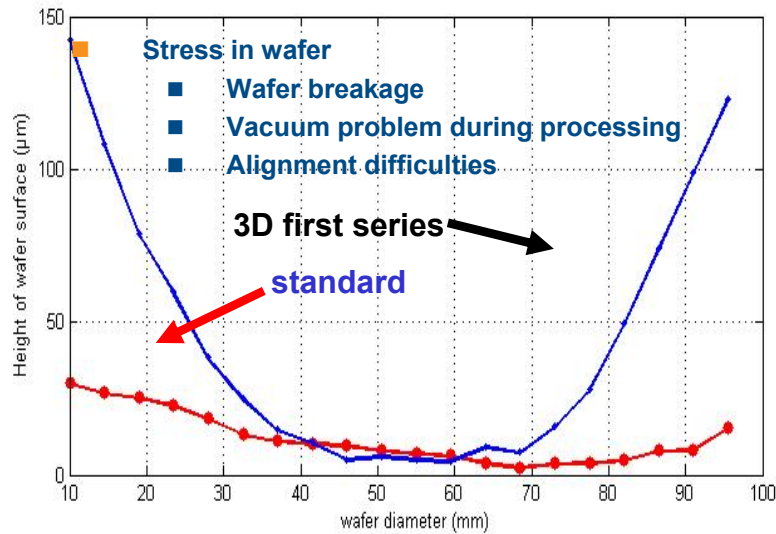
2 electrodes per  
pixel – 2E

# Fabrication steps and issues – First 3D-run





# Fabrication issues in first run

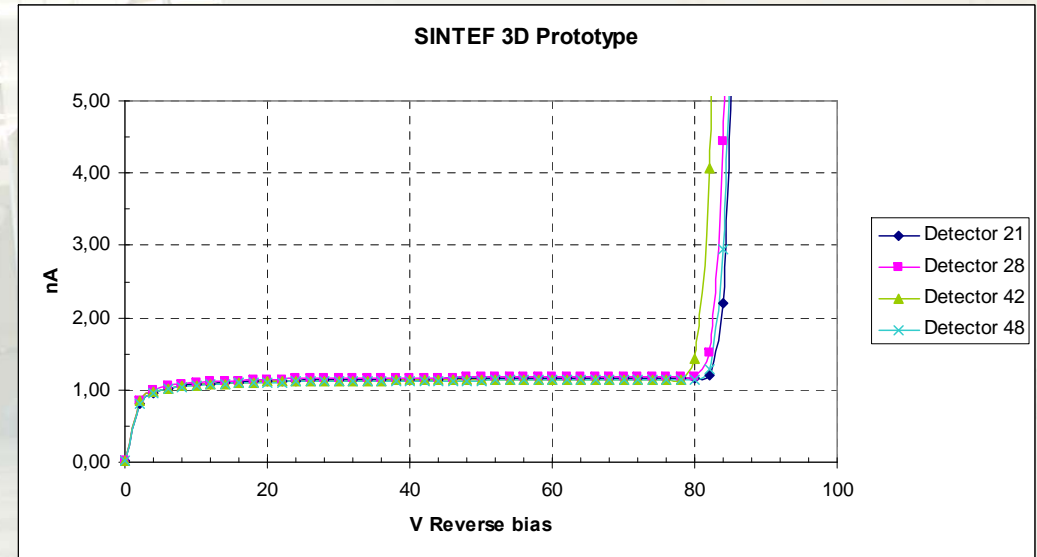
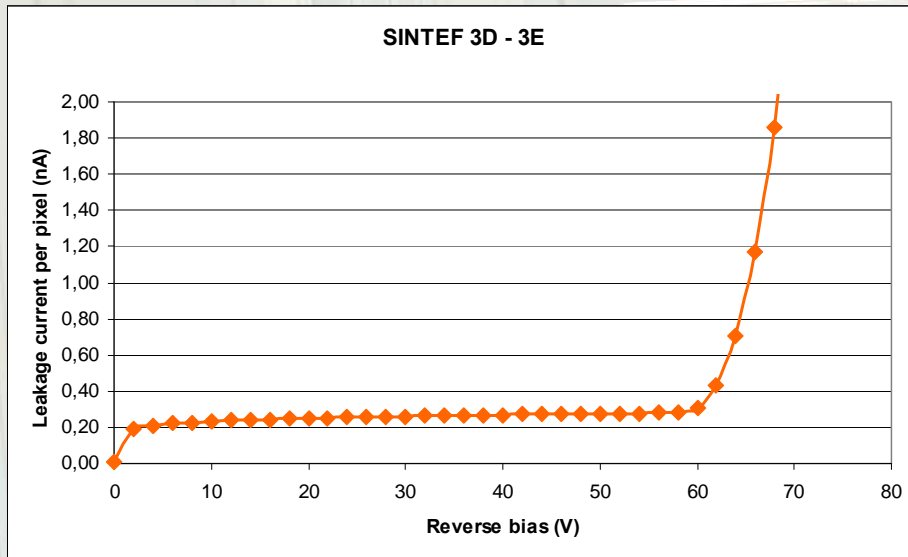


- Wafer stress after second electrode filling (p-electrodes). Induced wafer stress, bow and large breakage
- Bow and large topography made photolithography and alignment extremely difficult
- In spite of problems two wafers showed good diode characteristic

# Electrical measurements at the wafer stage first 3D-run

The p-bias electrodes represent the pn-junction and are all connected.

Thus measurement on one n-pixel gives total chip leakage current.



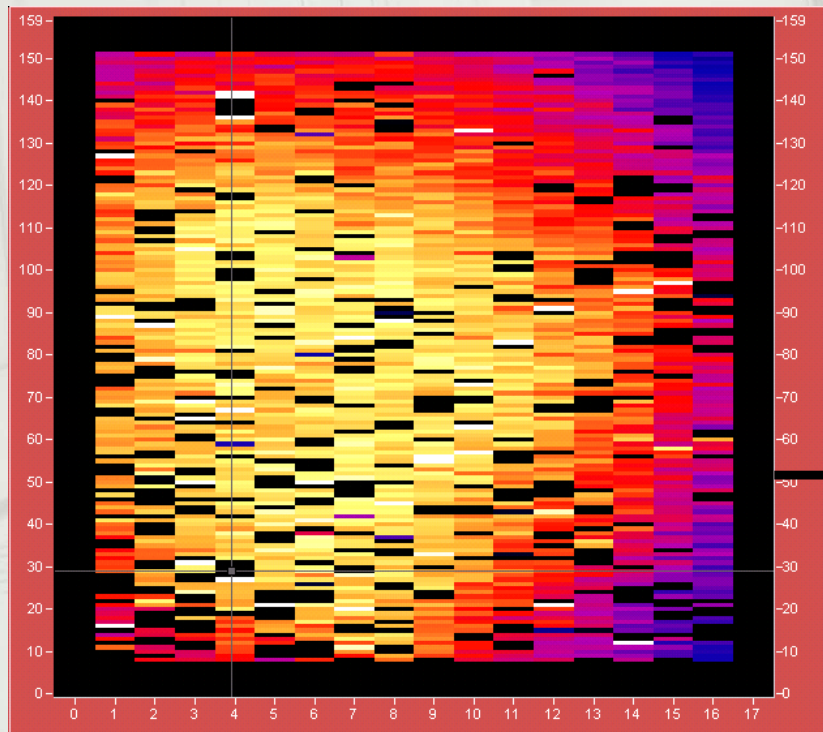
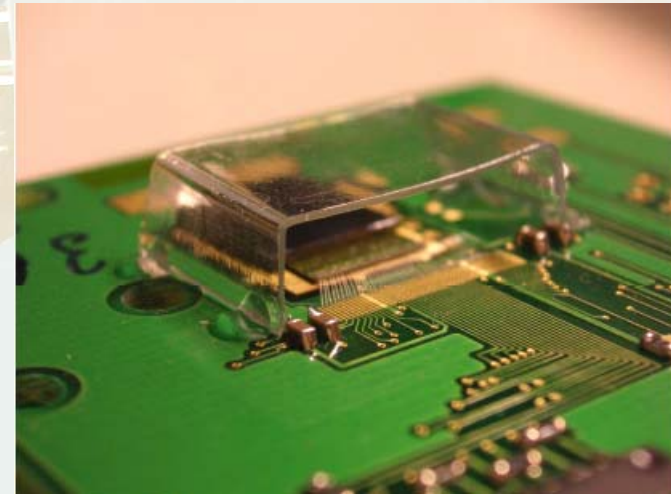
Average leakage current measured on ATLAS FE-I3 chips with  $\approx 2700$  pixels, 3E and 4E configuration.

Inter pixel / inter strip resistance measured at 60V between n-electrodes in adjacent pixels

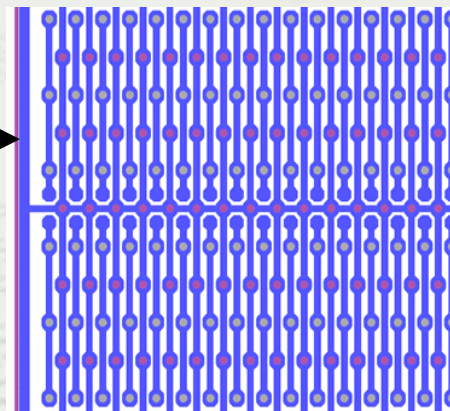
| Configuration | 2E                 | 3E                 | 4E                 | Baby strip       |
|---------------|--------------------|--------------------|--------------------|------------------|
| Resistance    | 600-800 M $\Omega$ | 300-500 M $\Omega$ | 100-300 M $\Omega$ | 6-6.5 G $\Omega$ |

# Testing after bump-bonding

- Noise was too high for a good convergence
- Lowest noise close to breakdown of the detector
- All modules suffered from irreversible breakdown after typically one day of operation
- Problems caused by device structure, that is n-readout on n substrate with active edge part of pn-junction.



- One module successfully recorded particles from an Am-241 source

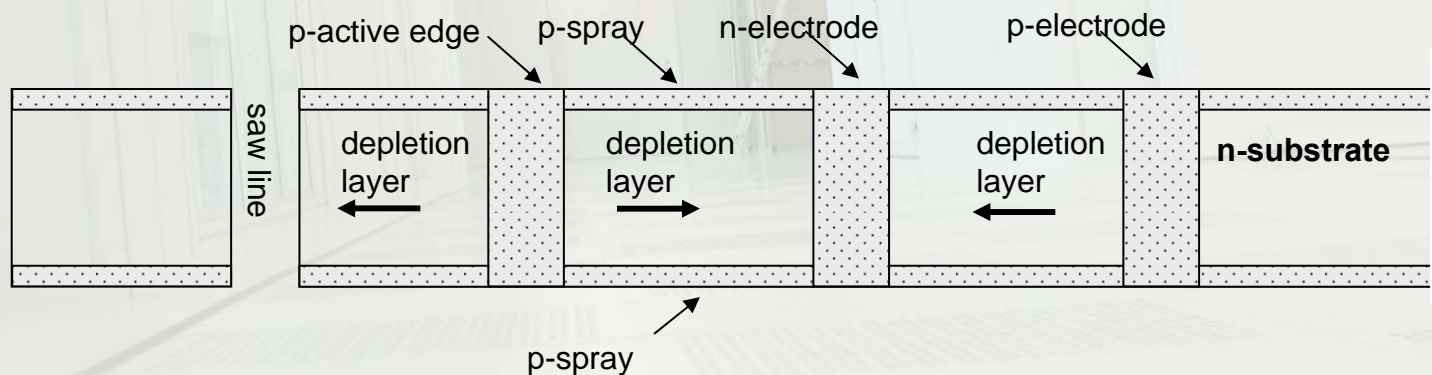


Each square corresponds to the number of hits per pixel

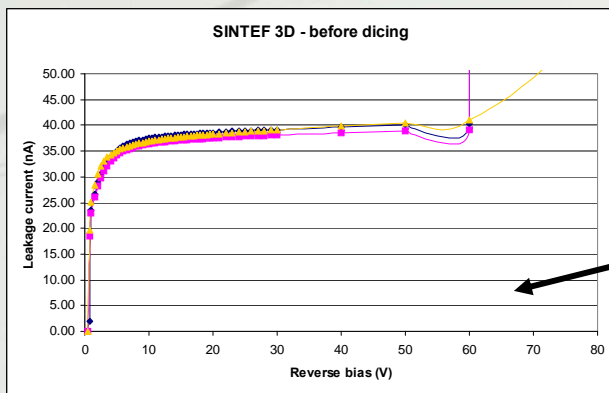
\*data taken by E. Bolle, H.Gjersdal and O. Rohne at the University of Oslo

# Inherent weakness of n-read out device with p-active edge made on n-substrate

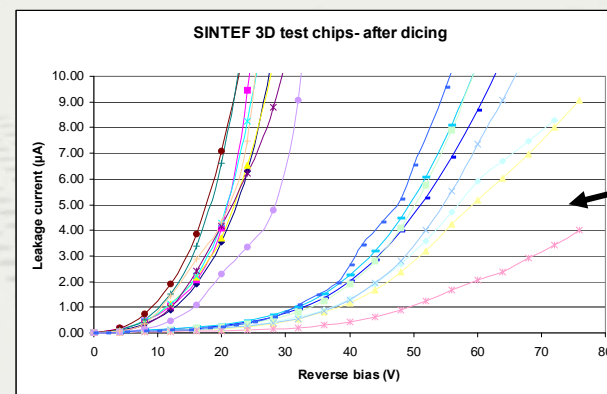
- All pixels share common pn-junction through the p-bias electrodes
- pn-junction also includes active edge and p-spray
- Cuts through pn-junction (p-spray) when dicing
- Depletion layer spreads out from active edge to non-passivated saw line



n-readout on n-substrate. oxide and metal not shown



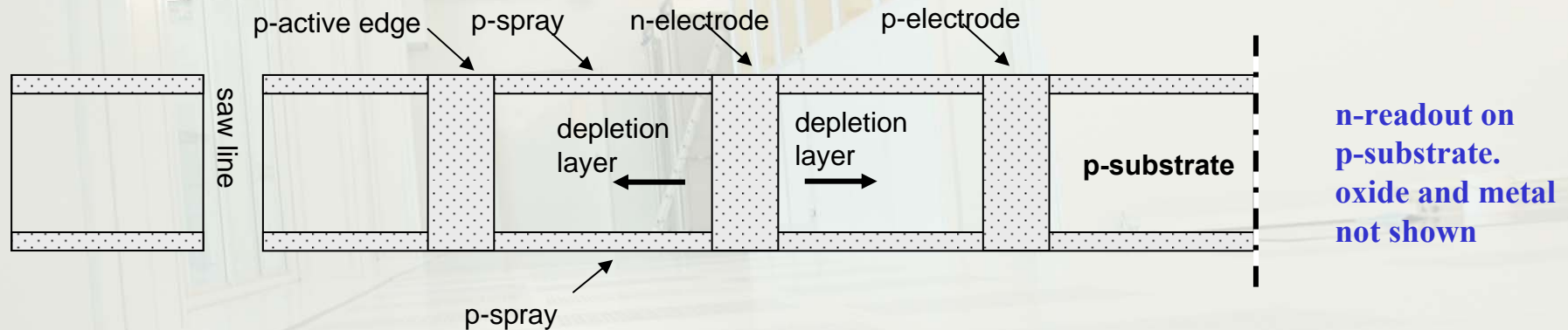
FE-I3 chips total leakage current  
Before dicing



After dicing  
highly increased leakage

## Second 3D-run at SINTEF (B-series)

n- readout devices on p-wafers.  
Active edge serves as depletion stop.  
n-readout pixels decoupled.  
P-spray not part of pn-junction



### Wafer specifications:

- 4 – inch,  $\geq 10000 \Omega\text{cm}$
- Thickness: 200  $\mu\text{m}$ , 17 pcs, 285  $\mu\text{m}$ , 6 pcs

### Process improvements based on experience from first run focus on:

- Reduced wafer stress, bow, topography and breakage
- New AMS 200 ISPEEDER “IPROD” used for DRIE etching

# MASK LAYOUT FOR 2<sup>nd</sup> RUN

Includes ATLAS, CMS and Medipix type devices.

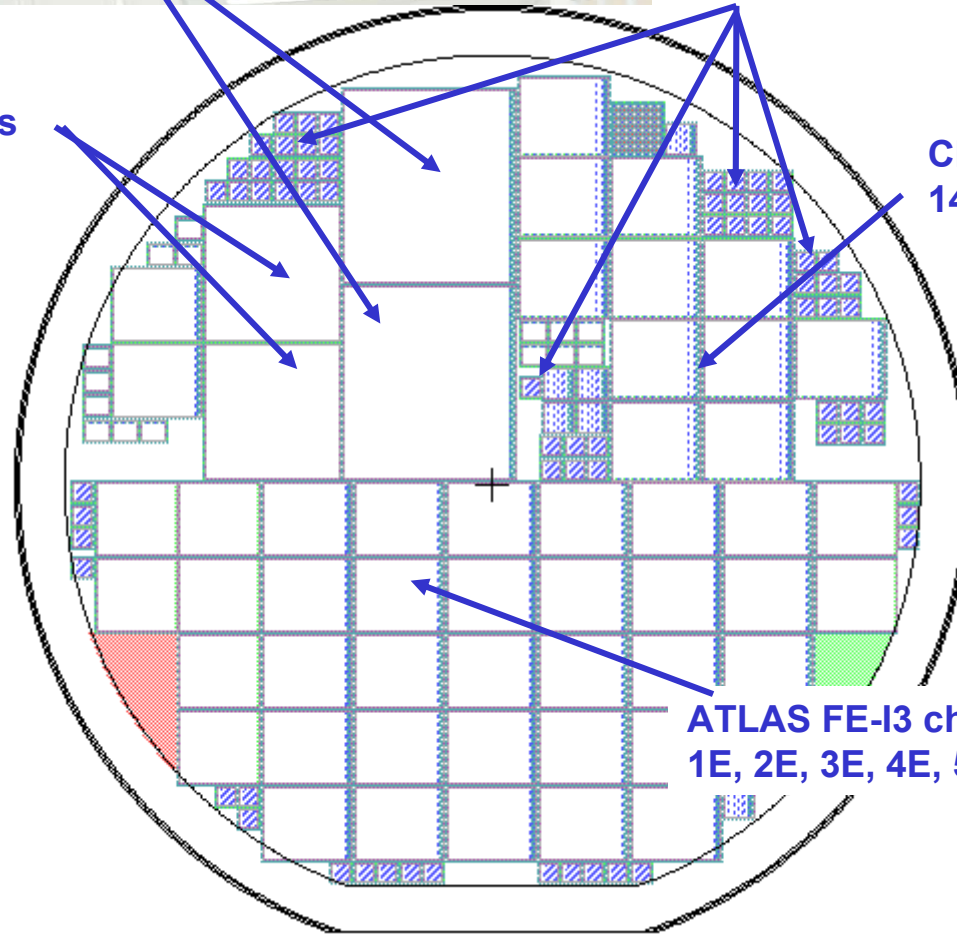
1E, 2E, 3E, 4E and 5E configurations

Atlas FE- I4 chips  
2E configuration

1E, 2E, 3E, 4E, 5E test structures

Medipix chips

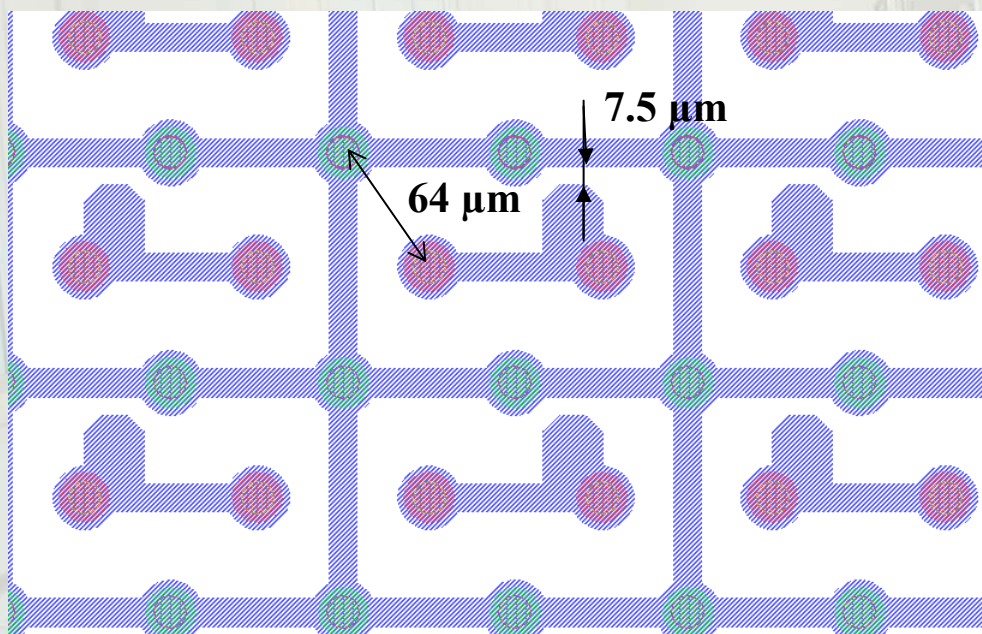
CMS 1ROC, 2E, 4E configurations  
14.6 % of wafer area



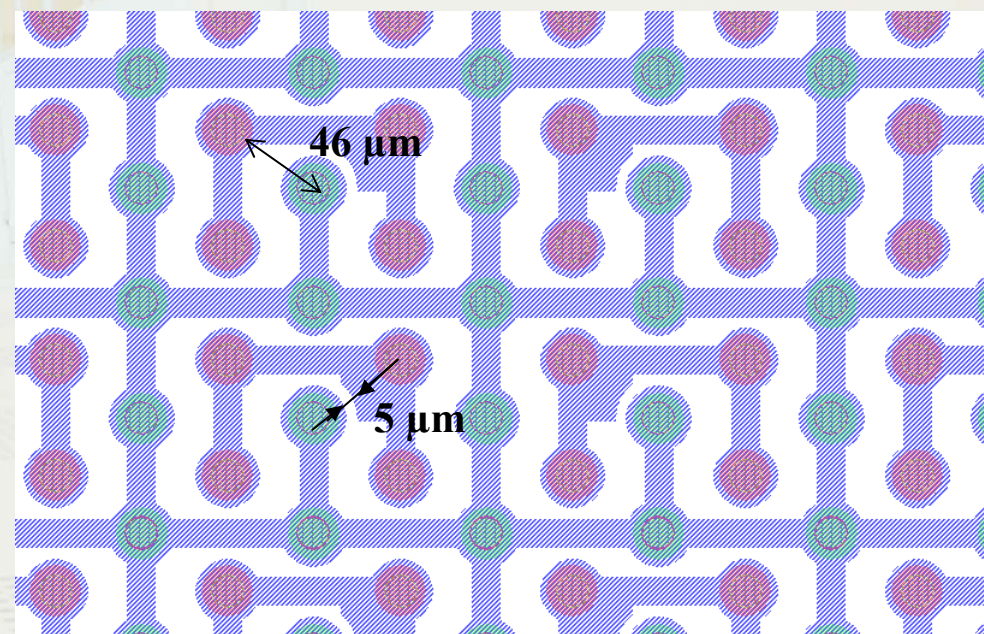
ATLAS FE-I3 chips  
1E, 2E, 3E, 4E, 5E configuration

# CMS 1ROC 2E and 4E configurations

Original design by Gino Bolla, slightly modified by SINTEF



2E configuration



4E configuration

## Configuration geometries and estimated depletion voltage

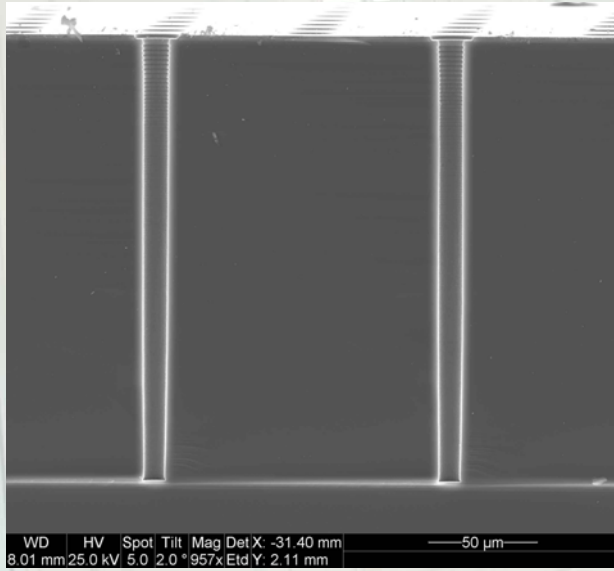
| Substrate specific resistivity: $\geq 10000 \Omega\text{cm}$ |        |        |        |       |       |          |                    |
|--|--------|--------|--------|-------|-------|----------|--------------------|
| Configuration  | ATLAS  |        |        |       |       | CMS 1ROC |                    |
|  | 1E     | 2E     | 3E     | 4E    | 5E    | 2E       | 4E                 |
| n - p electrode distance ( $\mu\text{m}$ )                   | 201    | 106    | 76     | 54    | 47    | 64       | 46                 |
| Max depletion voltage planar model                           | 40.5 V | 11.3 V | 5.8 V  | 2.9 V | 2.2 V | 2.2 V    | 4.1 V              |
| Max depletion voltage square cell model <sup>1</sup>         | 190 V  | 32 V   | 11.8 V | 3.9 V | 2.4 V | 6.9 V    | 2.4 V <sup>2</sup> |

1. V. Eremin, E. Verbitskaya, "Analytical Approach for 3D Detectors Engineering", 2008 IEEE Nuclear Science Symposium conference Record
2. Square cell model should apply well to 1ROC 4E configuration

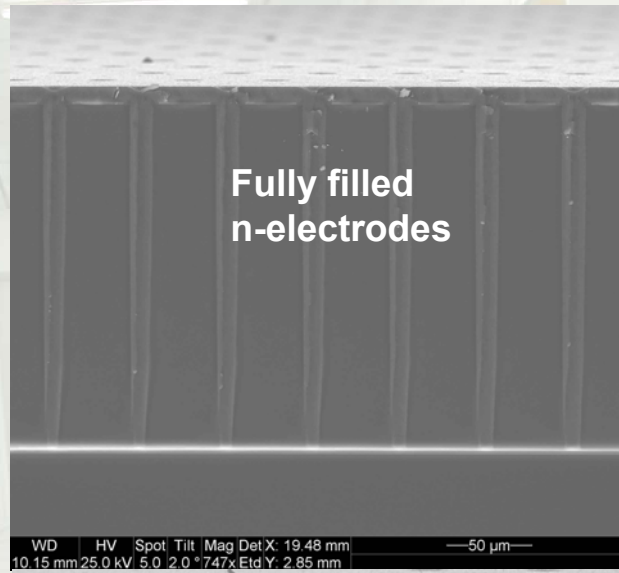


# Fabrication steps – second 3D-run

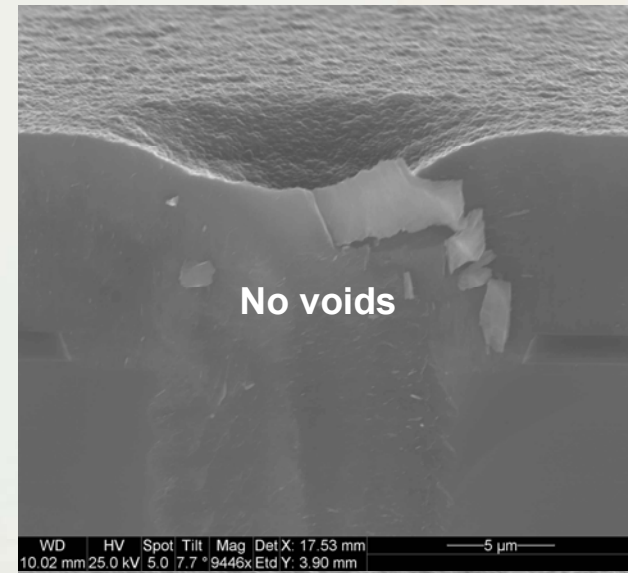
After DRIE



After poly filling

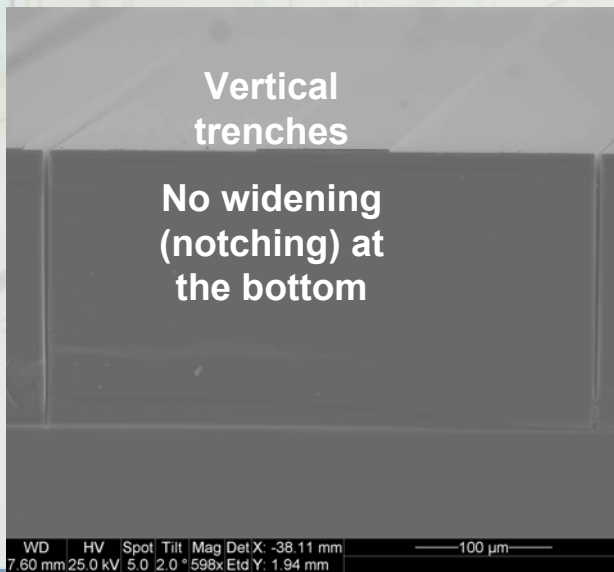


After poly filling

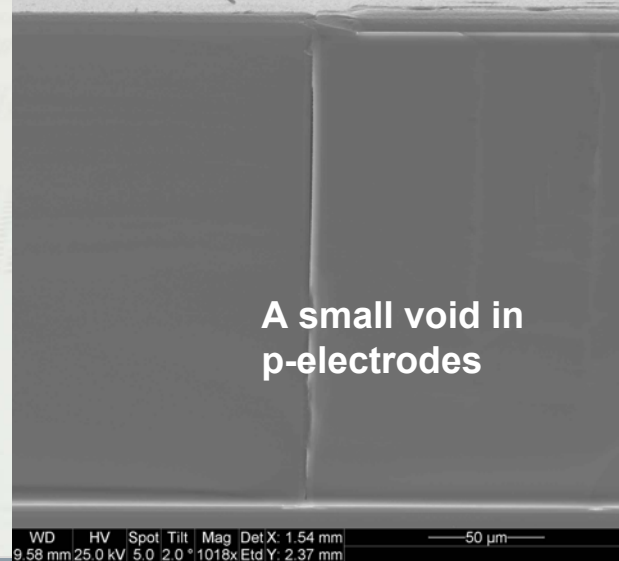


Vertical trenches

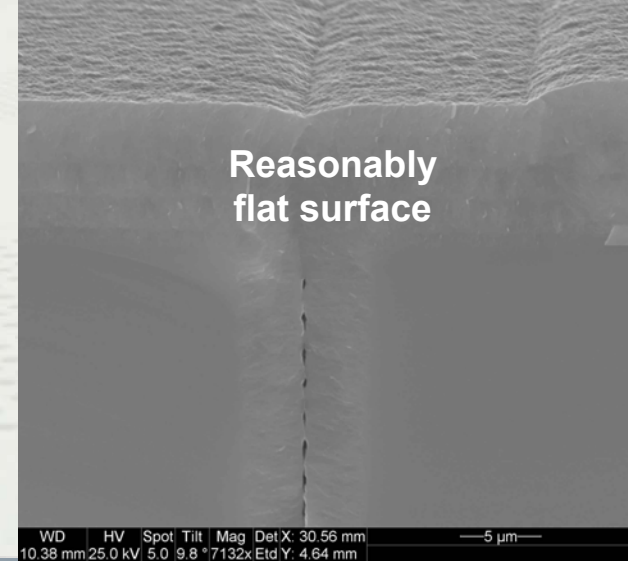
No widening (notching) at the bottom



A small void in p-electrodes

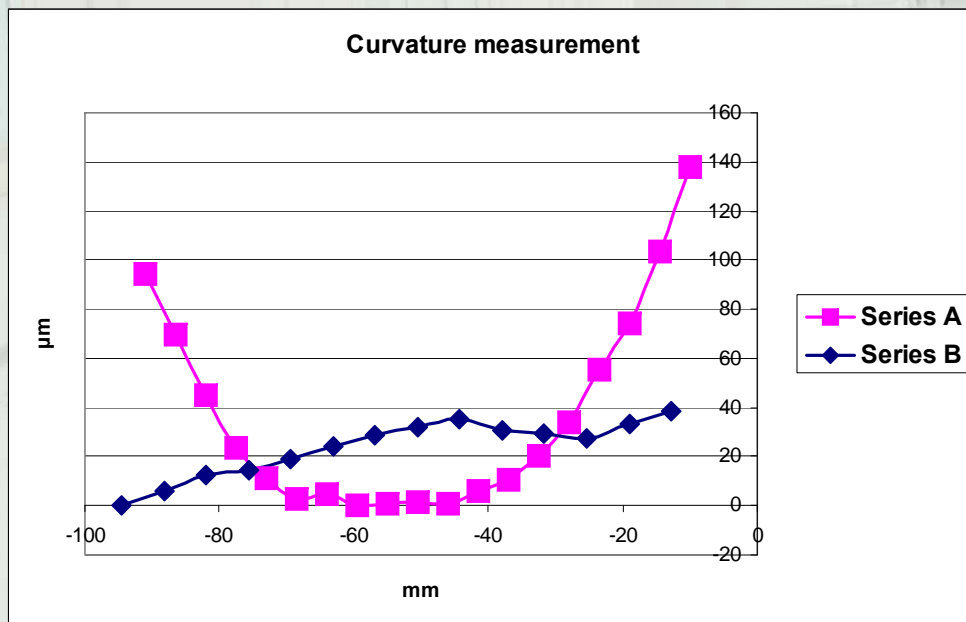
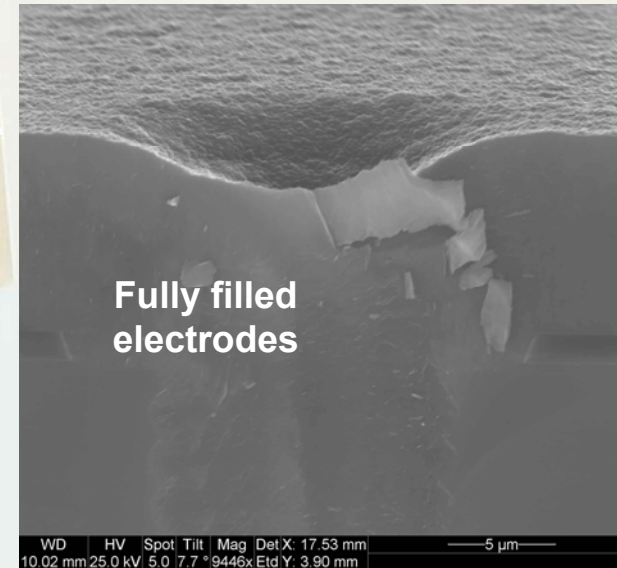


Reasonably flat surface



## SINTEF 3D: Series B improvements

- P-type wafers
  - Active edge will serve as depletion stop
  - More robust configuration
- Narrower trenches (4  $\mu\text{m}$ )
- Improved hole profiles
- Extra nitride layer
  - A better doping barrier
  - Protects the field oxide
  - Keeps symmetry on both back and front side



### Result of improvements

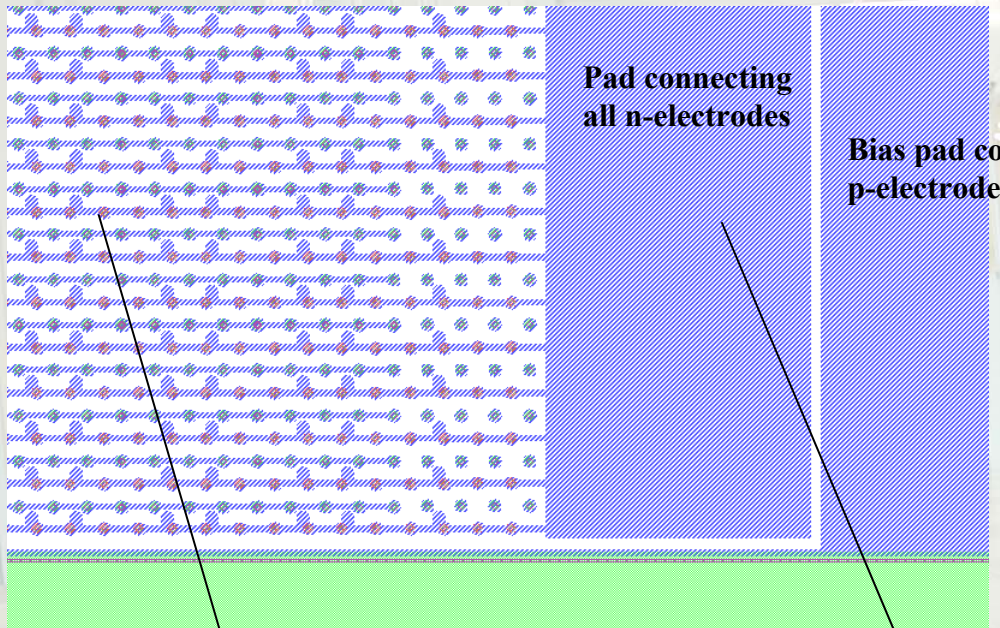
Much reduced stress, bow and breakage

Wafer yield: 18 out of 23

Improved electrode filling reduce topography and allow easier and better lithography

# Test metal for electrical measurement

Short circuits all n-electrodes. Later removed and replaced by final metal



Detail of CMS 1ROC chip 2E test metal

Test metal allows measurement of total chip leakage in one measurement. However, the positive potential on the metal pads / lines induces surface inversion (“MOS” effect). This may cause a large and possibly dominating contribution to the total leakage. May also determine breakdown. Thus the measurements are only indicative.

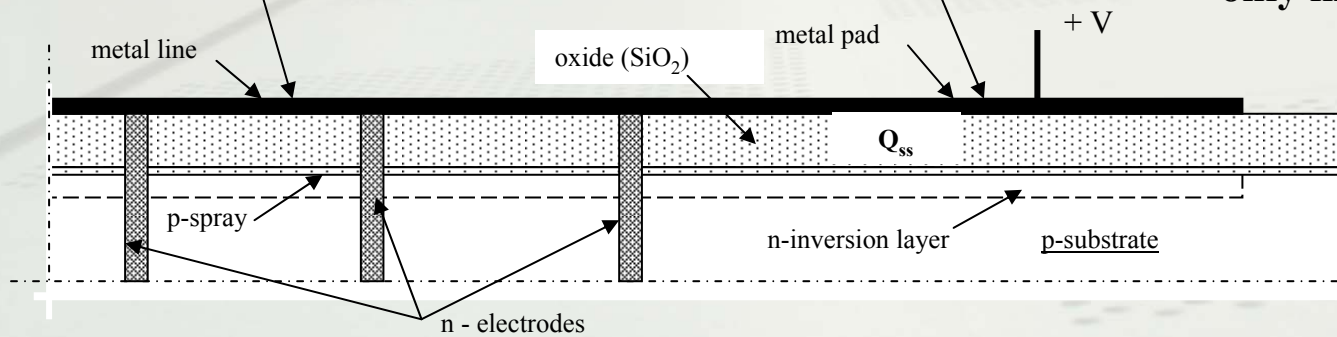
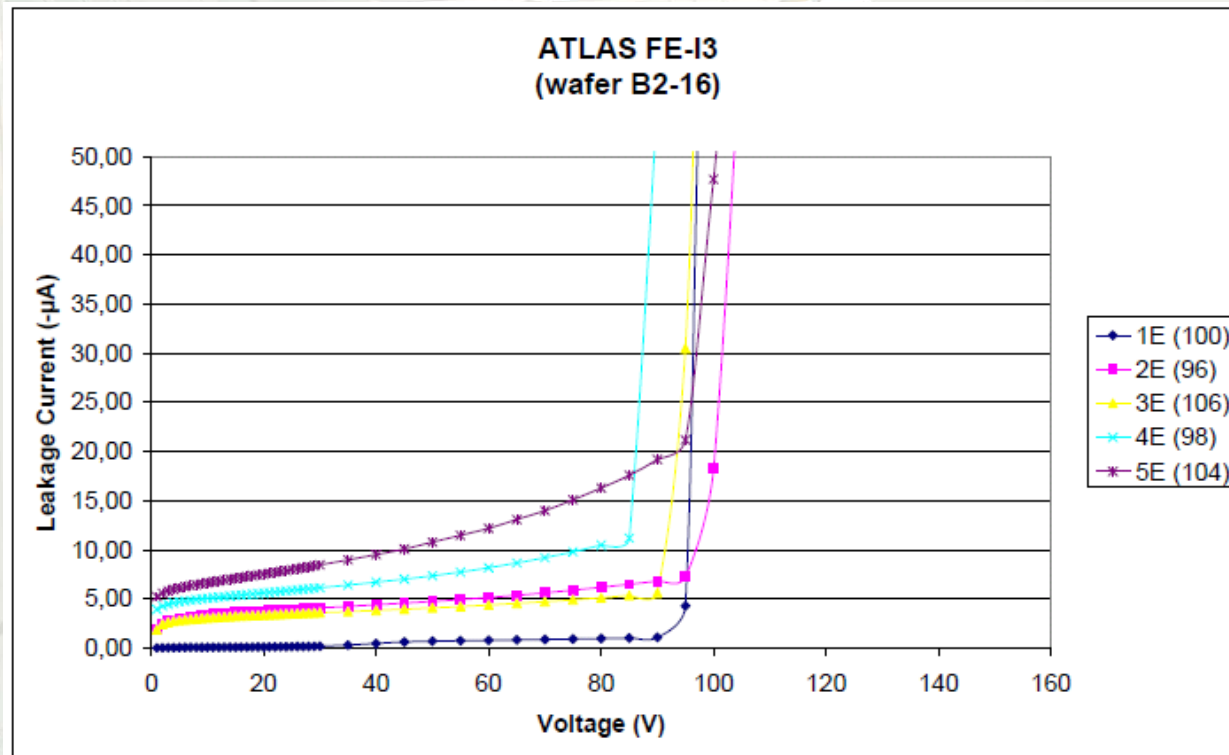


Illustration of MOS effect  
Turns on between 5 and 30 V depending on p-spray and oxide charge  $Q_{ss}$ .

# Measured IV-characteristics ATLAS FE-I3 chips

Summary of measurements of good chips on wafer B2-16 (200  $\mu\text{m}$  thick).  
Measured with test metallization which short circuits all pixels (n-electrodes).



Total leakage from  $\approx 2700$  pixels as function of bias.

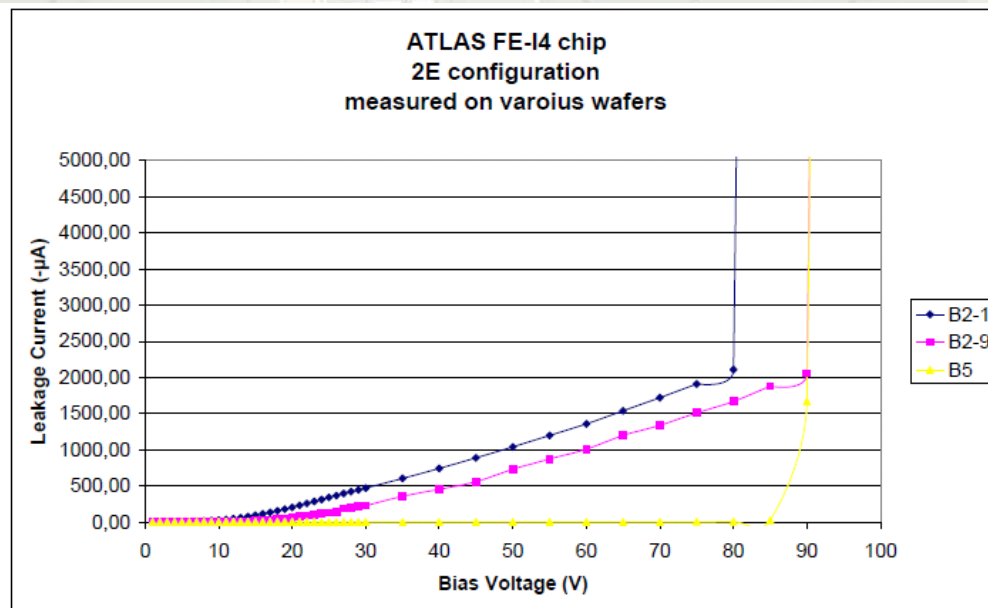
Corresponds to  $\approx 2700$  (1E) to  $\approx 13500$  (5E) electrodes.

Leakage Includes “MOS” effect and possible bad electrodes.

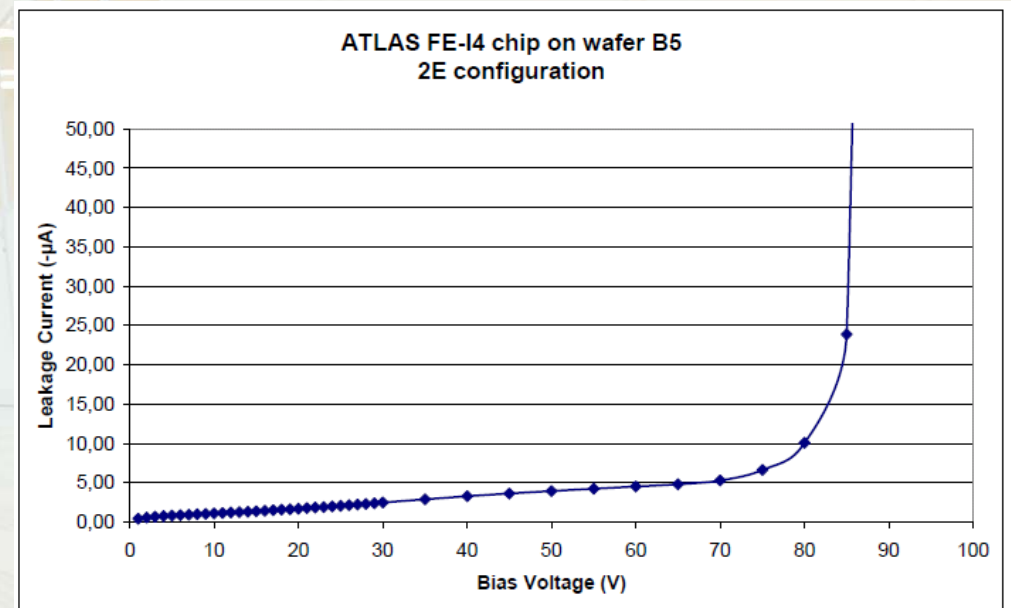
Yield of good chips on wafer typically 50% (preliminary result from 6 wafers)

# Measured IV-characteristics on ATLAS FE-I4 chips

Total leakage from 20376 pixels (40752 electrodes)  
including MOS effect and possible bad electrodes



I-V measurements on FE-I4 chips from wafers B2-1, B2-9 (200 µm thick) and B5 (280 µm thick)

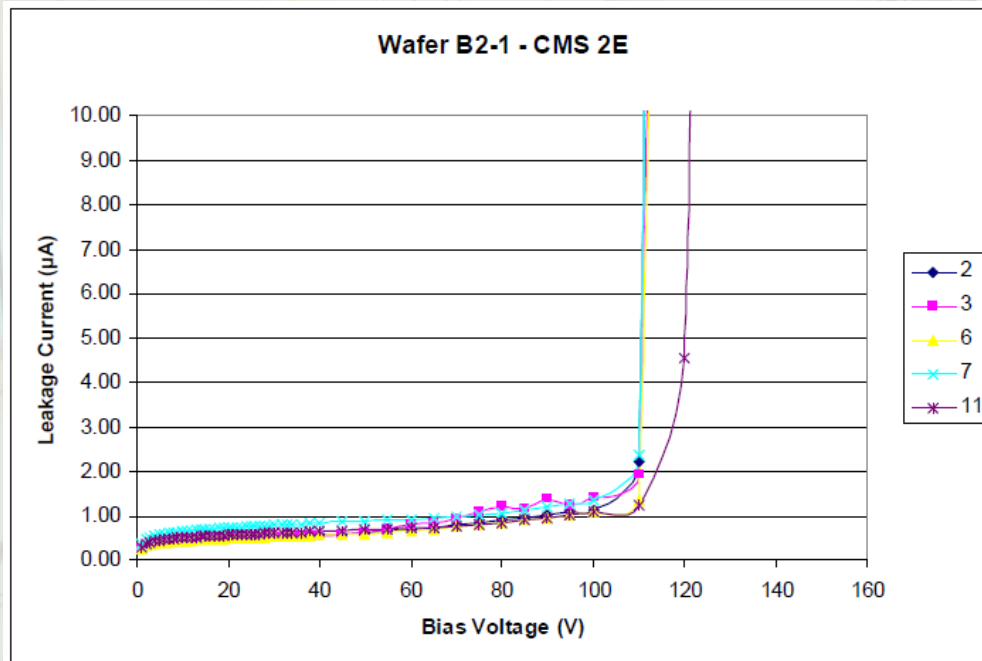


I-V measurements on FE-I4 chip from wafer B5 (285 µm thick). Chip at wafer edge.

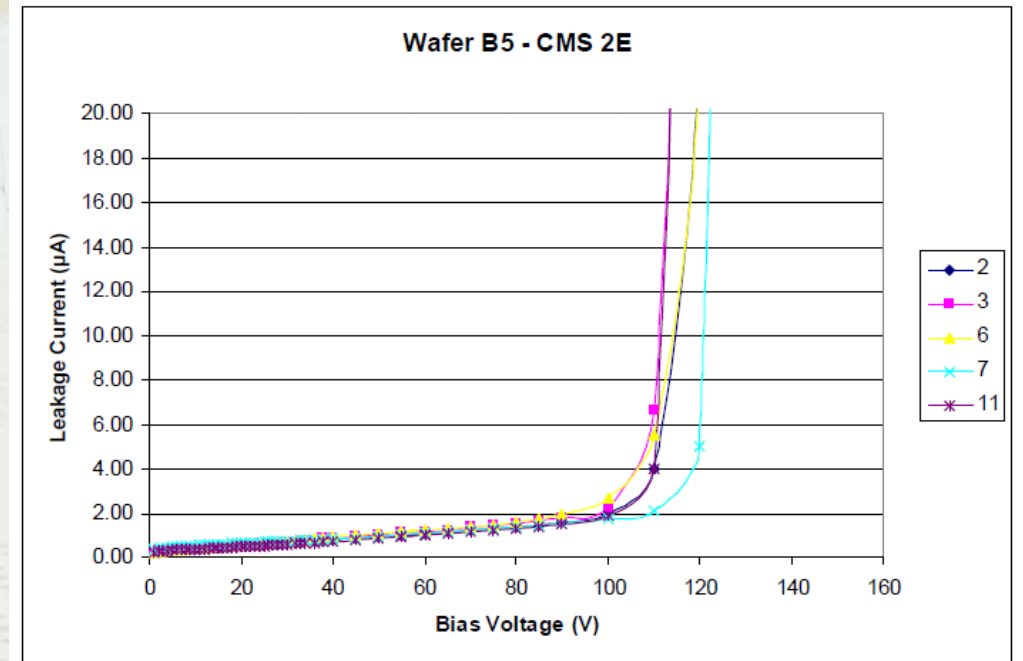
Active edge trench and electrodes not opened in upper left corner due to masking ring. Probably only  $\approx 34000$  electrodes opened (17000 pixels).  $< 100$  pA / electrode in full depletion including MOS effect.

# Measured IV-characteristics CMS 1ROC chips 2E Configuration

5 good chip from wafer B2-1 (200  $\mu\text{m}$  thick) and B5 (280  $\mu\text{m}$  thick)  
Measured with test metallization which short circuits all pixels (n-electrodes).  
Total leakage includes contribution from “MOS” effect and possible bad pixels  
Chip includes  $\approx 2000$  pixels ( $\approx 4000$  n-electrodes)



Wafer B2-1  
200  $\mu\text{m}$  thick



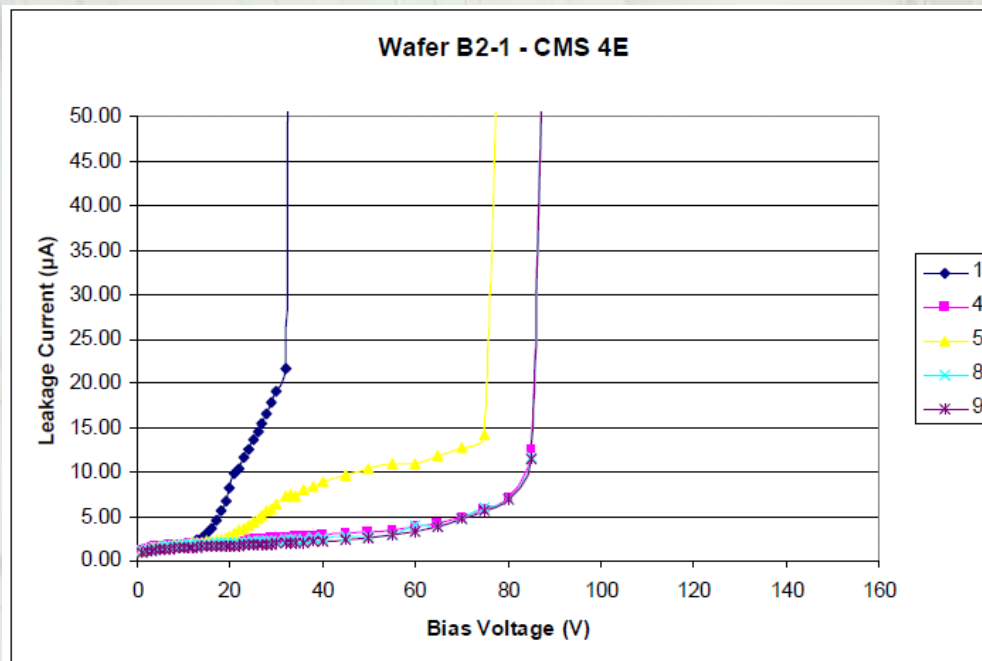
Wafer B5  
280  $\mu\text{m}$  thick

# Measured IV-characteristics CMS 1ROC chips 4E Configuration

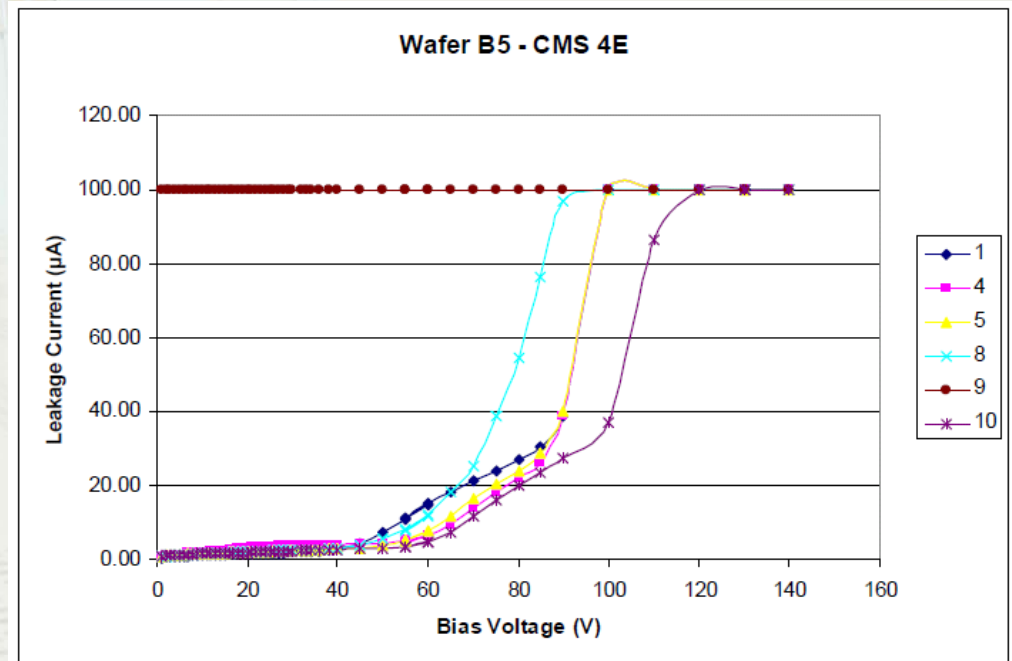
5 chips from wafer B2-1 (200  $\mu\text{m}$  thick) and B5 (280  $\mu\text{m}$  thick)

Measured with test metallization which short circuits all pixels (n-electrodes).  
Total leakage includes contribution from “MOS” effect and possible bad pixels

Chip includes  $\approx 2000$  pixels ( $\approx 8000$  n-electrodes)



Wafer B2-1  
200  $\mu\text{m}$  thick



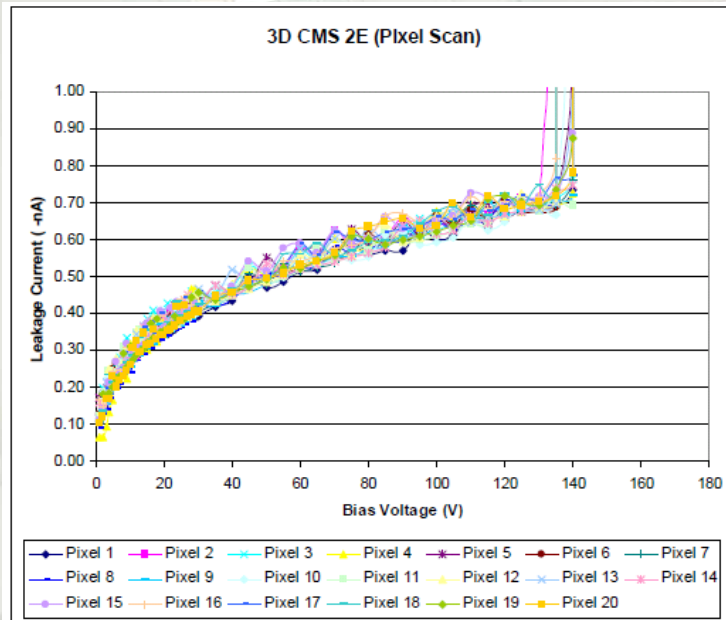
Wafer B5  
280  $\mu\text{m}$  thick

# CMS 1ROC 2E and 4E Configurations

Single pixel IV-measurements on chips with final metal.

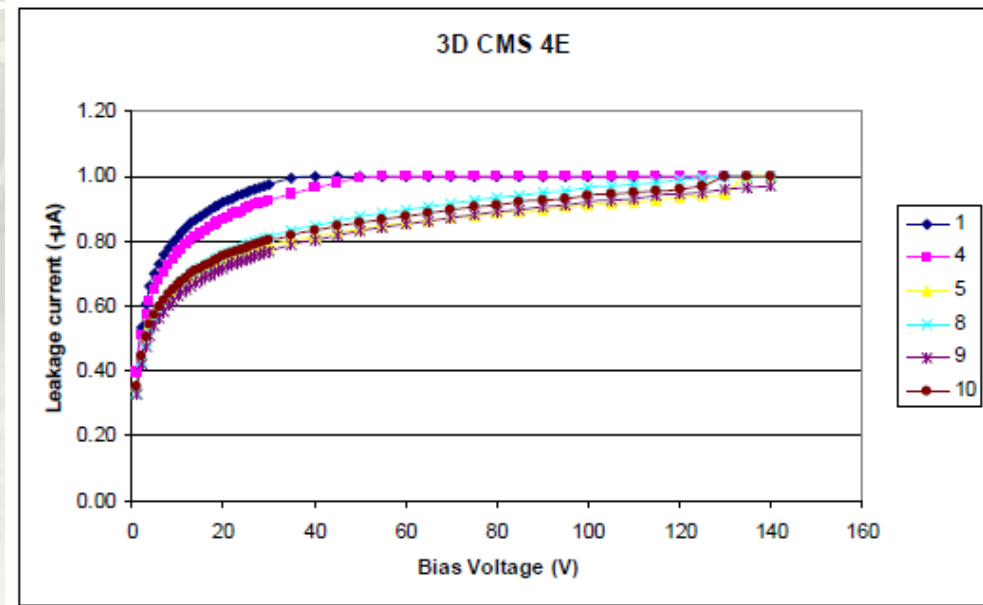
Other pixels floating and measurement include pick up from adjacent pixels.

Chip include  $\approx 2000$  pixels (4000 – 8000 n-electrodes)



## 2E configuration

IV-Measurement on 20 pixels from same chip. Very uniform leakage. Includes pick up from adjacent pixels



## 4E configuration

IV-Measurement on 6 pixels from same chip. Includes pick up from most of chip area



## Conclusions

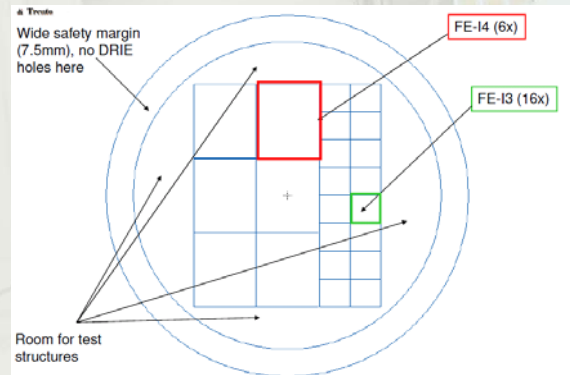
1. Technically 2<sup>nd</sup> SINTEF 3D-lot did run smoothly. New IPROD DRIE tool gives high quality electrode holes and fast etch times. However, reliability of IPROD tool not convincing with 3 long down periods. Large delays compared to project plan
2. p-type substrate wafer gives more robust configuration as active edge act as depletion stop and is not part of pn-junction. Final proof after dicing and bump-bonding
3. Process changes considerably reduced wafer stress and warping, improved electrode filling and lithography compared to first run. Low breakage and much improved wafer yield, 18 out of 23 wafers survived the process.
4. Typical pixel average leakage current 0.5 to 1 nA in full depletion measured with a test metallization that short circuits all pixels (n-electrodes) and includes possible bad electrodes and a contribution from the “MOS” effect. Confirmed by single pixel measurements on chips with final metallization. Real pixel leakage probably  $\leq 100$  pA.

## Further work

1. Further testing and characterization. Single pixel measurements
2. Develop processes for DRIE removal of support wafer and dicing
3. 4 wafers sent to IZM for bump-bonding on October 14, 2009. 2 will be bonded to FE-I3 and CMS readout chips and diced. 2 will only be metallized (UBM) and sent back to SINTEF for removal of support wafer and dicing by DRIE. Then sent back to IZM for bump-bonding of single chips.
4. Transfer technology to 6-inch wafers

# Further work for ATLAS

- Process wafers with common floor plan together with CNM (Barcelona), FBK (Trento) and Stanford. Different 3D-configurations, but common metallization and alignment masks for bump-bonding. Includes 6 FE- I4 sensor chips



Not final design, FE-I4 chips to be placed symmetrically on wafer

- Deliver prototype FE-I4 3D-sensor chips for prototype hybrids with FE-I4 readout ASIC. To qualify 3D-technology for IBL in competition with n-on-p and diamond detectors.

# Further work for CMS ??????

*Thank you for your attention!*

