DEPFET Seminar

DEPFET pixels for the ILC vertex detector

M. Trimpl

DEPFET – collaboration:

MPI/MPE Munich

U Mannheim
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U Prague
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U Aachen
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• **Introduction**: ILC project, vtx-d and requirements

• **DEPFET technology**:
  principle, present production and thinning approach

• **Sensor characterization**: clear, rad. tolerance

• **Overview**: ILC DEPFET-System

• **R/O - electronics (CURO- FE)**:
  architecture, circuit realization and results

• **Results** with present system (lab, beam test)

• **Summary and Outlook**
Activities in the SILAB

ATLAS pixels

large experience in ASIC design and detector instrumentation

new materials

signal current from alpha particles at different bias voltages

X-Ray Imaging

TCT – transient current technique

DEPFET ILC vtx-d

CdTe 2x2 module

ATLAS pixels

7.4 mm

11 mm

Fermilab, 17.07.2006

Marcel Trimpl, University of Bonn
International Linear Collider

• design phase: ILC - TDR 2007, starting 2017?
• 3 detector concepts: LDC (TESLA), SiD, GLD
• precision measurements: $\delta(1/p) = 5 \cdot 10^{-5} / \text{GeV}$
  (1/10 LEP, LHC)

• superconducting accelerating cavities ( $>25\text{MV/m}$ ):

- no synchrotron-radiation: $\Delta E_{\text{sync}} \propto E^4/m^4$

- defined initial state e+ e- 

- luminosity $L = 3 \cdot 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$, $E_{\text{CM}}$ up to 1 TeV

- linear accelerator

- electron-positron collision
- high energy physics experiments
- positron source
- aux. positron and 2nd electron source
- electron sources (HEP and x-ray laser)
- linear accelerator
- damping ring
- positron preaccelerator
- electron-positron collision
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- electron sources (HEP and x-ray laser)
**Beamstrahlung (e⁺e⁻ Pairs)**

\[ \delta_{BS} = \frac{\Delta E}{E} \propto \frac{E_{cm}}{\sigma_z} \left( \frac{N}{\sigma_x^* + \sigma_y^*} \right)^2 \]

**bunch structure:**

- 2820 bunches
- \( \Delta t_{\text{bunch}} = 337\text{ns} \)
- 950 µs
- 199 ms
- 950 µs

**occupancy:** 20% (readout once !!)

**R/O:** 50µs (20x per bunch train)

**Beamstrahlung:**

- 950 µs
- 199 ms
- 950 µs

5Hz repetition rate

**Graph:**

- [Graph showing Hits / BX vs. Radius [cm]]

- 800 GeV, 3T
- 500 GeV, 3T
- 800 GeV, 4T
- 500 GeV, 4T

**Layer 1:** 0.05 hits / mm² / BX

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ILC Vertex Detector (LDC)

- 5 layers, r: 15mm … 60mm
- pixel size: 20-30 µm, spatial resolution of a few µm
- module: ~ 13 x 100 mm², 22 x 250 mm²
- overall ~ 1GPixel
- thin sensors d=50µm: 0.1% X₀ per layer
- low power consumption (simple gas cooling)
- radiation tolerance: 200 kRad (5 years)

Impact Parameter Resolution ($d_o$)

$$\sigma = \sqrt{a^2 + \left(\frac{b}{p \sin^2 \theta}\right)^2}$$

- $a < 5\mu m$ (point precision)
- $b < 10\mu m$ (multiple scattering)

$p > 1..2$ GeV

$b : 300\mu m$
$c, \tau : 75\mu m$

Technologies:
- CCDs / ISIS
- MAPS/CMOS
- DEPFET
DEPFET principle of operation

principle

- FET-Transistor integrated in pixel (first amplification)
- charge generation in whole substrate (d=50µm, ENC=100e⁻: S/N > 40)
- charge collection due to electric field
- figure of merit: internal gain (g_q = ΔI_D/ Δq)

potential distribution:

[TeSCA-Simulation]
DEPFET Fabrication

design, fabrication and testing of DEPFETs at the **HLL MPI Munich**:

- 800m² clean room (class 1),
- 6” process line,
- min. feature size 1.5µm

HLL located at the Siemens plant in Neu-Perlach (founded 1992)

direct wafer writer (UV laser):

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DEPFET Applications

**XEUS**

- Imaging spectroscopy
- X-ray astronomy
  - 7.68 x 7.68 cm²
  - 1024 x 1024 pixels
  - 1 MPix
  - 75 µm
  - 300 ... 500 µm
  - < 4 el. ENC

**ILC**

- Particle tracking
- HEP
  - 1.3 x 10 cm² (x 8)
  - 520 x 4000 pixels (x 8)
  - 1GPix
  - 25 µm
  - 50 µm
  - ~100 el. ENC
  - 1.2 ms
  - 2.5 µs
  - 50 µs / frame
  - 50 ns / line

- Energy resolution:
  - 126 eV FWHM @ Fe⁵⁵ - kα line
  - Corresponding to 4.9 e⁻ ENC

**XEUS pixels on same PXD4 wafer run as ILC**

**T = -50° C**

- Mn-α
- K
- Mn-Kβ

Counts

Energy (keV)

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sensor production for the ILC

**fabricated**: matrices with up to 128x64 pixel, 450µm thick
linear double pixel structures (22x36 µm² pixels) (high density layout)

- **new production** started recently 03/2006:
  - matrices up to 512x512 pixel
  - full ILC length column & row test structures

special **clear gate**
to support clear operation
DEPFET clear operation

- remove charge via „clear“ contact
- remove all charge → complete clear
  no „reset-noise“, needed at the ILC
DEPFET clear operation (details)

• ‘clear gate’ to lower the clear barrier
  Clocked and static operation possible
• deep high-E n-implantation in some devices
to lower clear voltages
clear efficiency

- Measurements on mini matrix devices
- ‘noise’ becomes minimal if clearing is complete!

• complete clear achieved with static clear gate!
• required voltages small (5 - 7 V) – important for future SWITCHER!
• clear (gate) operation does not decrease after irradiation (1MRad)

Complete clear in only 10 ns:

- various designs (high-E, no high-E)
- geometries (length of clear gate)
- operating conditions (static or clocked clear gate)

[C. Sandow, Bonn]
radiation tolerance: sensor

irradiation up to 1MRad using $^{60}$Co

single pixel spectrum

$^{55}$Fe
shaping-time = 6µs, @ RT
~ 1MRad

from iron-peak: ENC ~ 15 e$^{-}$
(comparable with preirrad. structures)

- shift: - 4...- 6 V
- saturation after 200 kRad

[L.Andricek, MPI Munich]
matrix operation

- low power consumption,
- low multiple scattering
  but line rate: \( \geq 20\text{MHz} \)

pedestal + signal
pedestal

signal

amplifier / multiplexer
ILC - DEPFET module (L1)

sensor: \(\sim 50\mu m\)

frame: \(\sim 300\mu m\)

cavities in frame can save material

chips 50µm thick & bump bonded

thinned sensor (50 µm) in active area

thick support frame (~300 µm)

material budget (1st layer, incl. steering chips and frame) \(\sim 0.11 \% X_0\)
Producing thin DEPFETs

1. implant backside on sensor wafer
2. bond wafers with SiO₂ in between
3. thin sensor side to desired thick.
4. process DEPFETs on top side
5. etch backside up to oxide/implant

**wafer bonding:**

[thinned silicon sample

‘holes’ to reduce material]
ILC DEPFET-System

Clear Switcher
DEPFET Matrix (450μm thick)
64x128 pixels, 36 x 28.5μm²

Gate Switcher
Analog board with ADCs, DAQ …

USB 2.0 based digital interface board

Current Readout CURO II

Hybrid-PCB

Marcel Trimpl, University of Bonn

[Fermilab, 17.07.2006]
steering chip SWITCHER

Features:
- produced 1/2003
- 2 x 64 channels (‘A’ and ‘B’)
- switches up to 25 Volts
- ground levels arbitrary
- internal sequencer (flexible pattern)
- daisy chaining of several chips for modules possible
- 0.8 µm AMS HV – technology
- radiation tolerance may be problematic!

- functionality proven ✓
- RAM & sequencer (digital) tested up to 80 MHz
- power consumption ~ 1mW / channel @ 30MHz

Switching 20V @ 30MHz

20 ns

[1. Peric, Mannheim]
SWITCHER: speed

>50% Layout size!

I.Peric, Mannheim

VDDA = 10V
VDDA = 15V
VDDA = 20V

nmos (Vlow):

- typ value: < 200 Ω
- C_{row} = 15\text{pF}
- \tau = 3\text{ns}

( fast steering! )
DEPFET readout: drain vs source

**source (follower) R/O**

- constant bias current $I_B$ provided
- charge in internal gate translates into source voltage node change

\[ \tau \approx 2.2 \times \frac{C_L (1+C_{gs}/C_{gd})}{g_m} \approx \mu s \]

**drain R/O**

- keep $V_{DS}$ constant, measure $I_{Drain}$ directly
- fast response: limited by RC time of $R_{in}$ (CURO) and $C_L$

\[ \Delta I \]

→ few ns @ $C_L = 40pF$

**no option for ILC**
readout mode @ ILC

ILC: no „trigger“ → hit detection / 0-suppression in readout chip

advantage:
- 0-suppression while processing one row
- fast CDS (suppresses 1/f noise)

needed:   - complete „clear“ (demonstrated !)
overview: CURO-Architecture

CURO – Current ReadOut

- current based readout
  → low input impedance by regulated cascode

- pedestal + signal is stored in current memory cell

- pedestal current is subtracted at input node after reset (fast CDS)

- signal current buffered (alternating) in 2 cells
  → hit-identification, FIFO storage

- FIFOs digital part is scanned by HIT-Finder

- Hit-Finder finds up to 2 hits per cycle:
  - analog currents to outA, outB
  - digital hit position stored in HIT-RAM
CURO I (testchip)

- TSMC 0.25µm
- 5metal layer
- contains all building blocks of CURO-Architecture
- radiation tolerant layout rules with annular nmos
- 05/2002

r/o concept proven!
CURO II

- **Pads** (communication):
  - Fast signals: LVDS

- **Digital part**:
  - Hit-Finder,
  - RAM, FIFO

- **Steering unit**:
  - ~20 steering signals

- **Analog part**:
  - Current memory cells, comparator

- **128 input channel**
  - (DEPFET - Matrix)

- **12x 8bit DACs**
  - Biasing, test currents, thresholds

- **TSMC 0.25µm**
- 5 metal layer
- 4.5 x 4.5 mm²
- 11/2003
input cascode

control dynamic behavior
(pole-zero cancellation)

\[ \tau \approx C_L \cdot R_{in} \]

\[ V_{gr} = \frac{g_{m2}}{2\pi C_L} \]

higher \( g_m \) by higher \( I_{Bias} \) \( \rightarrow \) speed vs. power

present-matrices: 7.5pF; final ILC-matrices: \( \approx 40pF \) !!

CUROIIB: power down feature

\( I_{Bias} = 1\mu A \) static operation \( \rightarrow \) fix input potential

500\( \mu A \) \( \rightarrow \) high speed operation

CASCODE compensates load capacitance
current memory cell (principle)

charge: input (S1) and sample-switch (S2) closed
→ charge gate-capacitance of M1

d sample: open input (S1) and sample-switch (S2)
→ voltage at capacitance „same“
→ current „same”

transfer: close output-switch (S3)
(right after “sampling”)
→ \( I_{\text{out}} = -I_{\text{in}} \) at output node

\[ I = I_{\text{in}} + I_B \]

store current ??

[Hughes/Toumazou]

(use of cascode techniques !)
current memory cell (advantages)

advantages:

- high dynamic range (with reduced supply voltage)
- precise current subtraction easy
- drivers not needed

\[ I = I_{in} + I_B \]
\[ I_{out} = I_1 - I_2 \]

[Hughes/Toumazou]

(use of cascode techniques !)
noise vs. time response

**noise contribution**

\[ <v^2> = \frac{kT}{C} \]

\[ <v_{th}^2> = 4RKT\Delta V \]  

(independent of R)

\[ <i^2> \approx g_m^2 \frac{kT}{C_G} \]

\[ C_G + \frac{1}{g_m} \approx \frac{kT}{C_G} \left( \frac{C_{BUS} + 2/3C_G}{C_{BUS} + C_G} \right) \]

- \( g_m \) small, \( C_G \) large, \( C_{BUS} \) minor importance

**time response**

- switch optimizes time response
- noise vs. bandwidth
- minimize bus capacitance

\[ \tau = \frac{C_G + C_{BUS}}{g_m} \]
two stage sampling cell

schematic:

layout:

(+) improves linearity
(non-linearity due to charge injection)

(-) more complex steering! (all signals generated „on-chip“)

different designs:

coarse stage: fast, noise does not contribute
fine stage: „slower“, optimized for noise

calculated noise: ~25nA, bandwidth: 50MHz
Linearity + Pedestal Subtraction

**Linearity:**
- Transfer gain: \(1.00 \pm 0.01\)
- INL = 2.3 %
  (Integral Non Linearity)

**Pedestal Subtraction:**
- \(5 \mu\text{A} \ (10\%)\)
- Pedestal dispersion
  \(\rightarrow 75\text{nA}\) after pedestal subtraction

**Graph:**
- **Gain:** 1.0005
- **Offset:** -1.67 \(\mu\text{A}\)
- **Non-linear:** 0.287 \(\mu\text{A}\)

**Integral non-linearity:**
- \(0.287 \mu\text{A}\)

**Pedestal dispersion:**
- \(\rightarrow 75\text{nA}\) after pedestal subtraction

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Fermilab, 17.07.2006
Marcel Trimpl, University of Bonn
Noise & Dispersion

- noise:
  DEPFET r/o with CURO:
  ENC ~ 90e⁻
  \( g_q = 500\text{pA/e}^{-} \)

- Dispersion:
  \( \sigma \approx 35\text{nA} \)
  after calibration
  dispersion < noise

\[ \sigma = 43 \pm 1\text{nA} \]

\[ \sigma = 32\text{nA} \]
range = 160nA

\[ \sigma = 425\text{nA} \]
range = 1385nA

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**fast 0 - suppression**

**parallel** tree architecture
- finds up to 2 hits per clock cycle
- propagation delay:
  \[ 2^{\log(_{2} \text{channels})} = 7 \text{ only!} \]

**serial** hit finding
- clock > 2 GHz needed
- "aggressive" even with 0.09 µm!

**Hit-Finder:**

```
0 0
1 x
1 1
0 0
0 0
1 x
0 0
0 0
0 x
```

Address = 2, 6, (3)

[P. Fischer]
Hit-Finder: Layout

challenge:
128 leaves
of the tree
in linear layout

overall: 3200 x 85 µm²

rad. tolerant design!
CURO II measurements (cont'd)

digital tests:

expected mean rate (1. layer):
1-2 hits @ 20MHz

works fine up to: 110MHz

→ 250W for whole vtx-d (continuous operation)
bunch structure 1:199
→ pulsed mode (1:30) ~ 10W

total power consumption:

\[
P \text{ [mW]} = \begin{cases} 
2.15 \text{mW/channel @ 20 MHz} & \text{[2.5 V, RT]} \\
\end{cases}
\]

\[
\begin{array}{c|c}
\hline 
frequency \text{ [MHz]} & P \text{ [mW]} \\
\hline 
0 & 200 \\
20 & 250 \\
40 & 300 \\
60 & 350 \\
80 & 400 \\
100 & 450 \\
120 & 500 \\
\hline 
\end{array}
\]

CURO II measurements (cont'd)
System Measurements
CMOS matrix

Hybrid with CMOS-Imager Matrix in AMS 0.35µm

reset[0]  select [0]
reset[1]  select [1]

reset circuit

M5
M6  M1
M7
M2
M3
M4
reset
M8
M9
U_reset
U_ped
ped
U_out
I_out
zero suppressed r/o (CMOS matrix)

Hybrid with CMOS-Imager Matrix in AMS 0.35µm

full analog frame

lightspot of a desk lamp

zero suppressed analog readout

zero suppressed matrix r/o works
next CURO: neighbor logic

[R.Kohrs, Bonn]
ILC DEPFET-System in the lab

75 µm thick Tungsten-Mask

irradiation with $^{55}$Fe
(6keV $\gamma$, 1700 e$^-$)

system performance:

• **speed**: line rate $\sim$2 MHz
• **noise**: 220 e$^-$ (from noise peak)

---

![Graph showing signal (ADU) vs. energy (keV) for $^{241}$Am]

**$^{241}$Am**

- **Integral-Non-Linearity = 0.75% for 8500e$^-$**

INL = 0.75% (8500e$^-$ dyn. Range)

$g_q = 280$ pA / e$^-$
noise contributions: system

- Sensor
  (shot noise) $8e^{-}$ (50µs), $45e^{-}$ (current r/o)
  (1/f noise) $1.6e^{-}$ (after CDS)
  (thermal noise) $26e^{-}$ (after CDS)
- SWITCHER (kT/C) 0.92nA $3.3e^{-}$
- CURO (sampling) 45nA $160e^{-}$
- External transamp. 26.5nA $94e^{-}$

total: $\sim 190e^{-}$ (measured $\sim 220e^{-}$) ...

noise after CDS

$\langle ENC_{1/f}^2 \rangle = \frac{a_{1/f}}{2} \frac{g_{m}^2}{g_{d}^2} \cdot 2 \int_{0}^{\infty} \frac{1 - \cos(2\pi \nu_{c} \tau \cdot x)}{x \cdot (1 + x^2)} \, dx$

$x = \nu / \nu_{c}$

$\langle ENC_{th}^2 \rangle = 4kT \cdot \frac{2}{3} \frac{g_{m}}{g_{d}^2} \nu_{c} \pi \left(1 - e^{-2\pi \nu_{c} \tau} \right)$

---

switching noise:

![Switching noise diagram]
scaling potential of the DEPFET

influence of internal amplification:

\[ S/N \sim g_q \]

(when noise is dominated by readout chain)

noise improvement:

- ILC operation lower than room temperature
- redesign of CURO
- new DEPFET sensors (higher \( g_q \))

\[ \rightarrow ENC = 100 \text{ e}^- \text{ achievable} \]
Test Beam Results

- Beam T24 @ DESY, Electrons @ 6 GeV
- Reference telescope: 4 Si-strip planes

- noise ~ 16 ADU
- S/N ~110 (450µm sensors !)
- position resolution: CERN test beam in August 2006
summary

- **DEPFET pixel based vtx-d presented**
  - features: high S/N due to fully depleted bulk
  - present production (~30x30µm² pixels, matrices: 128x64 pixels, 450µm thick)
  - clear, radiation tolerance demonstrated, thinning concept established

- **Readout ASIC (CURO) using current mode techniques:**
  - pedestal subtraction, fast CDS, on chip hit-detection and 0-suppression

- **CURO II performance:**
  - noise: $< 45nA \rightarrow \sim 160 e^- (g_q=280pA/e^-) / 90e^- (g_q=500pA/e^- \approx \text{design value})$
  - analog speed: 24 MHz line rate (48MSPS), sufficient for ILC!
  - hit-identification and 0-suppression: > 100MHz, sufficient for ILC!

- **ILC-DEPFET-System:**
  - operated at $\sim 2$MHz line rate, noise: 220e⁻
  - 6GeV e⁻ test beam at DESY: S/N $\sim 110$ (450µm sensors)
outlook

System:
- increase system **speed** (2MHz → 20MHz !!)
- reduce **noise** (190e⁻ possible, next system should achieve <100e⁻)
- beam test @ **CERN** -> spatial resolution and establish pixel telescope

CURO IIb:
- on-chip **common mode computation/correction** (easy with currents)
- cluster logic (keeping at least the closest neighbor)
- improve **input cascode** (readout larger matrices)
- implement (fast) **power down feature** (pulsed mode configuration)
- on chip **ADC** (IP from nordic semiconductor)

New sensors:
- 512x512 matrices, 25x25µm²
- production of **thin DEPFETs** (longer time scale)
## references

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<th>References</th>
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<tr>
<td>Thinning:</td>
<td>„Processing of ultra thin silicon sensors for future linear collider experiments“, L.Andricek et al., IEEE TNS (51), No3, pp.1117-1120</td>
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</tr>
<tr>
<td>Sensor:</td>
<td>„Design and Technology of DEPFET Pixel Sensors for Linear Collider Applications“, R.H.Richter, NIM A511, pp.250-256</td>
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<tr>
<td>Rad Tolerance:</td>
<td>„The MOS-type DEPFET Pixel Sensor for the ILC Environment“, L.Andircek et al., Pixel 2005, submitted to NIM (A)</td>
<td></td>
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</table>
Potential during collection - 3D Poisson equation (Poseidon)

(50µm thick Si, $N_B=10^{13}$ cm$^{-3}$, $V_{Back}=-20$V)

Sources
Drain

External (internal) Gates

n+ clear contacts

Cell size 36 x 27 µm$^2$
Along the channel

Metal 2

Metal 1

Oxyd

Poly 2

Perpendicular to the channel

Clear

Gclear

Channel

n+

Deep p

Deep n

p
a) oxidation and back side implant of top wafer

b) wafer bonding and grinding/polishing of top wafer

c) process → passivation

open backside passivation

d) anisotropic etching from backside (TMAH)
Multiple Scattering

- During passage through matter Coulomb scattering on nuclei leads to deviation from original track

\[ \theta_0 = \frac{13.6 \, \text{MeV}}{\beta cp} z \sqrt{x / X_0} [1 + 0.038 \ln(x / X_0)] \]
Uncertainty in predicted position

\[ \sigma_{\text{tot}}^2 = \sigma_{\text{DEPFET}}^2 + \sigma_{\text{intrinsic telescope}}^2 + \sigma_{\text{multiple scattering}}^2 \]

- Remember: \( \sigma_{\text{MS}}^2 \sim 1/E_{\text{tot}}^2 \)
- Using these scans both errors can be estimated and corrected for assuming:
  - Resolution proportional to pitch
  - Telescope performance equal in X and Y
- Note:
  - August: error MS + intr=8-9\(\mu\)m
  - January: error MS + intr≈6.2\(\mu\)m
  - (Daniel: 6.94\(\mu\)m)
Position resolutions

<table>
<thead>
<tr>
<th>Hybrid</th>
<th>$X_{\text{CoG}}^{\text{corr}}$</th>
<th>$Y_{\text{CoG}}^{\text{corr}}$</th>
<th>$X_{\eta}^{\text{corr}}$</th>
<th>$Y_{\eta}^{\text{corr}}$</th>
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<td>6.2</td>
<td>3.0</td>
<td>5.3</td>
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<td>5.8</td>
<td>4.2</td>
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<td>4.0</td>
</tr>
<tr>
<td>1B</td>
<td>5.8</td>
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<td>4.9</td>
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<tr>
<td>GCG</td>
<td>6.2</td>
<td>3.8</td>
<td>5.2</td>
<td>4.6</td>
</tr>
</tbody>
</table>

- Note that these values are estimated. Expected to be better. However, subtracting 6.2 or 6.9 make huge difference.
- $\eta$-distributions in Y asymmetric, magnitude depending on seed odd or even
Estimated Power Dissipation

- For $V_{\text{Drain}} = 5\, \text{V}$ and $I_{\text{Drain}} = 100\, \mu\text{A}$ (conservative values): $P_{\text{DEPFET}} = 0.5\, \text{mW per active device}$

- **Layer1** (8 Modules x 2 sides x 512 = 8192 pixels), duty cycle = 1/200 (idealistic case):
  
  Sensor: only active pixels dissipate power
  
  $\Rightarrow 8192 \times 0.5\, \text{mW} / 200 = 20\, \text{mW}$

  SWITCHER:
  
  $6.3\, \text{mW per active channel at 50MHz (measured)}$
  
  $\Rightarrow 16 \times 6.3\, \text{mW} / 200 = 0.5\, \text{mW}$

  CURO: 5 mW / channel (extrapolated)
  
  $\Rightarrow 8192 \times 2.8\, \text{mW} / 200 = 220\, \text{mW}$

  **Sum:** $\sim 240\, \text{mW}$

- Scaling up from 18.7 Mpixels (L1) to $\sim$493 Mpixels for **5 layers** gives:
  
  **Total:** $\sim 6.3\, \text{W}$

- **Note:** Largest dissipation (CUROs) is outside active area where cooling is less problematic!

- This calculation assumes that all chips can be switched into a stand-by mode with $\sim$zero power dissipation between bunch trains. This feature must be included in future chip versions.

- given a safety margin **total power still < 10W**