Detector challenges for LCLS-II FLORA: LCLS/SLAC and Fermilab collaboration

Gabriella Carini

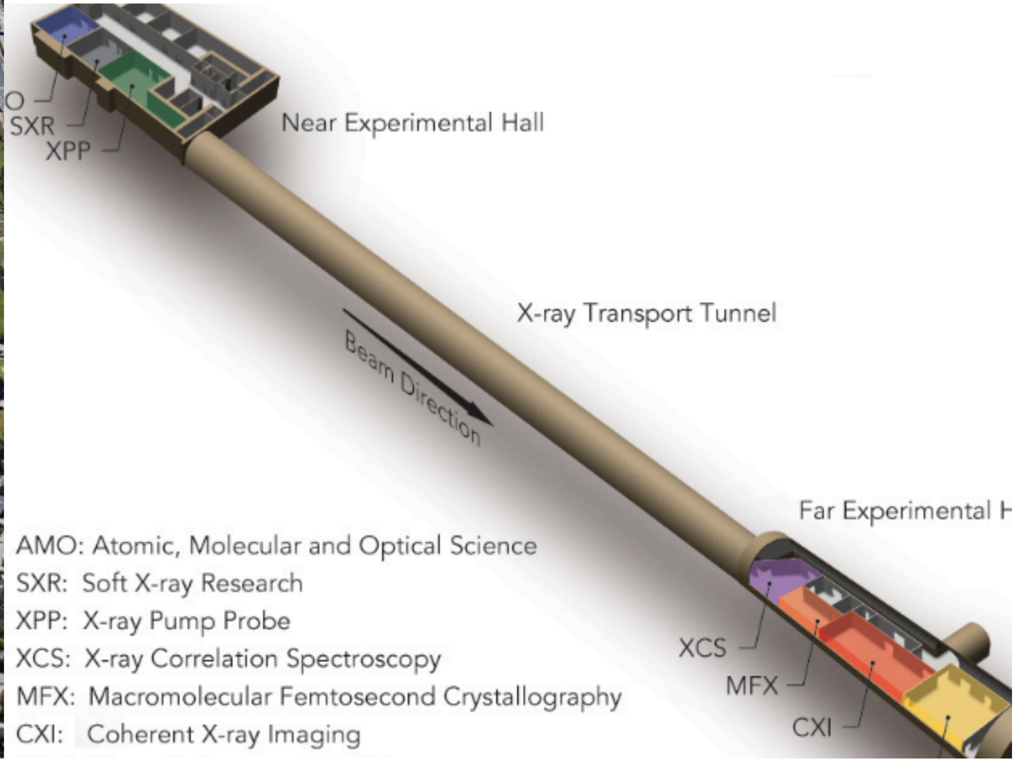
2017/06/20

U.S. DEPARTMENT OF ENERGY
Office of Science
SLAC NATIONAL ACCELERATOR LABORATORY

LCLS: the first hard x-ray FEL source

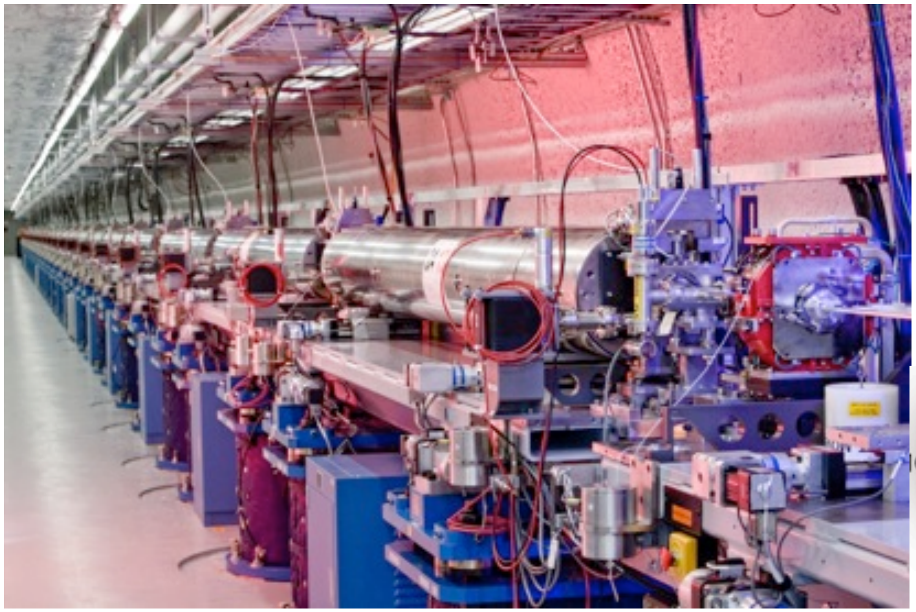
LCLS – main characteristics

- Pulsed (up to 120 Hz)
- Pulses are very short (~10 – 100 fs)
- Monochromatic
- Extreme peak brightness
- Spatially coherent



LCLS: the first hard x-ray FEL source

Operational since 2009



LCLS - Undulators Hall

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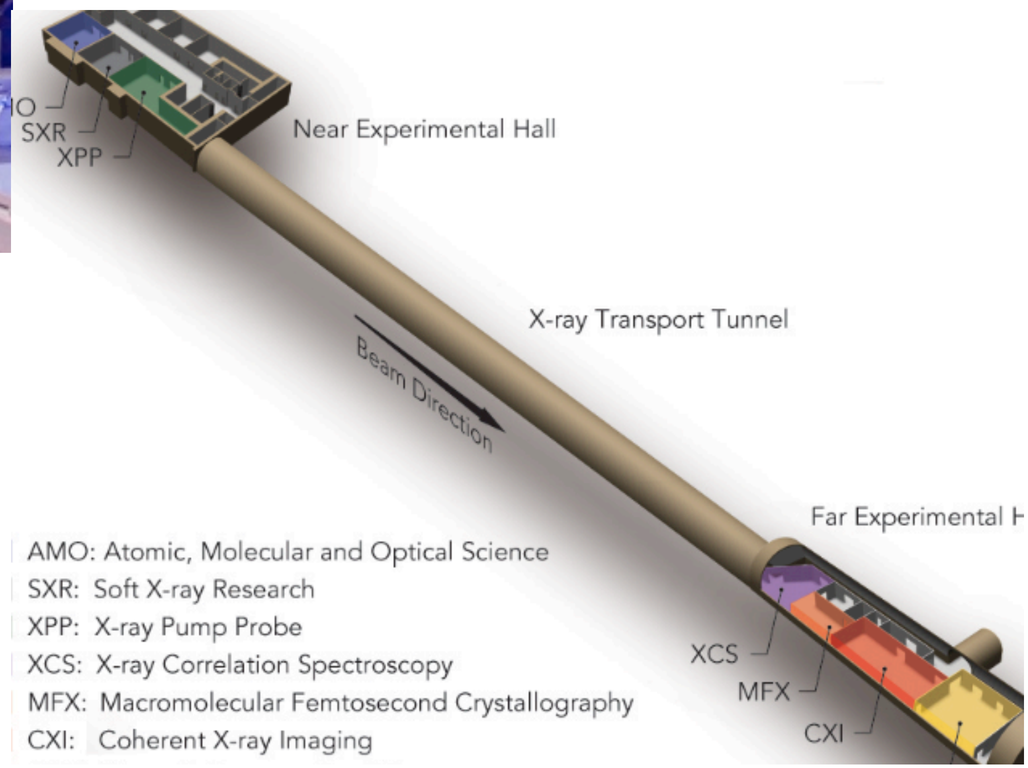
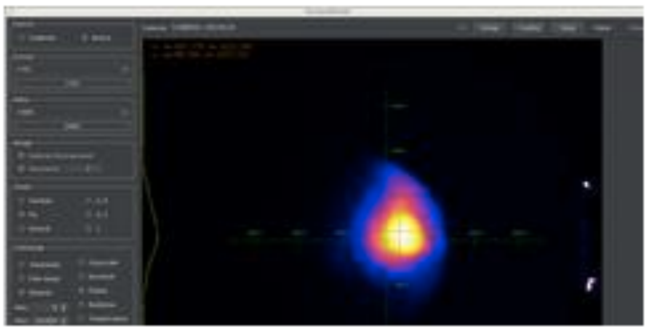


Other FELs

- FLASH - (since 2005, DESY, Germany)
- SACLA XFEL - (since 2011, Japan)
- FERMI – (since 2012, Italy)
- PAL XFEL - (since 2016, South Korea)
- SwissFEL - (Swiss - 2017)
- European XFEL - (Germany – 2017)

LCLS: the first hard x-ray FEL source

LCLS – main characteristics



16 May 2017

SWISSFEL - FIRST LASING AT A WAVELENGTH OF 4.1 NM

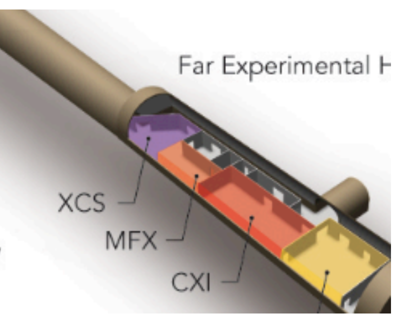
SwissFEL first Lasing at a wavelength of 4.1 nm The electron beam energy of SwissFEL was recently increased to above 900 MeV by successfully bringing two new accelerating modules into ... more »

04 May 2017

EURPEAN XFEL - FIRST LASING

First Lasing at European XFEL With its first lasing, the European XFEL reaches the last big milestone before the official opening In the metropolitan region of Hamburg, the European XFEL, the ... more »

AMO: Atomic, Molecular and Optical Science
SXR: Soft X-ray Research
XPP: X-ray Pump Probe
XCS: X-ray Correlation Spectroscopy
MFX: Macromolecular Femtosecond Crystallography
CXI: Coherent X-ray Imaging



FEL science

SLAC

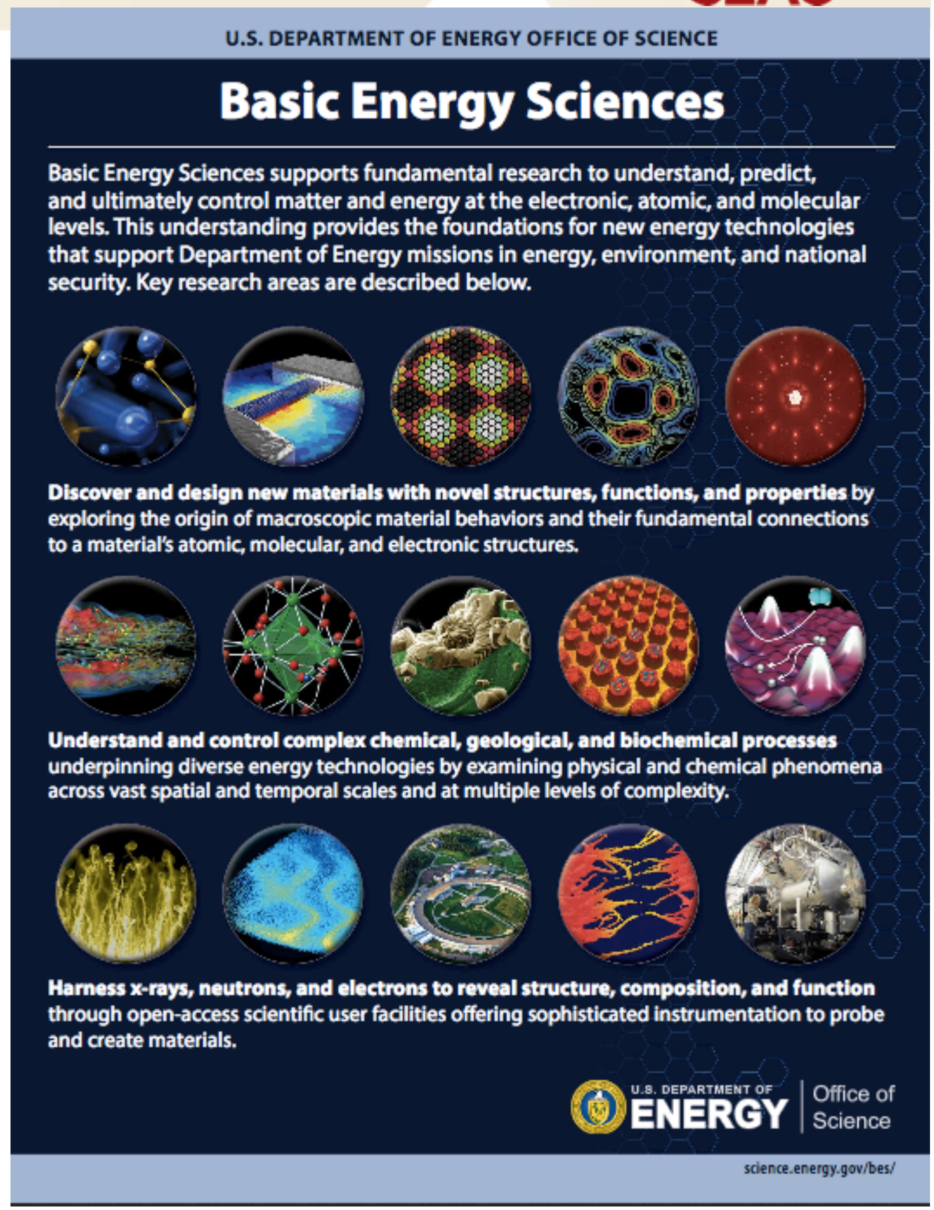
FELs are unique tools to probe matter (any kind of) at atomic length and time scale.

New materials (e.g. quantum materials)

Femtochemistry (e.g. catalysis)

Serial Femtosecond Crystallography

Matter under extreme conditions (e.g. plasmas, high-pressure materials)

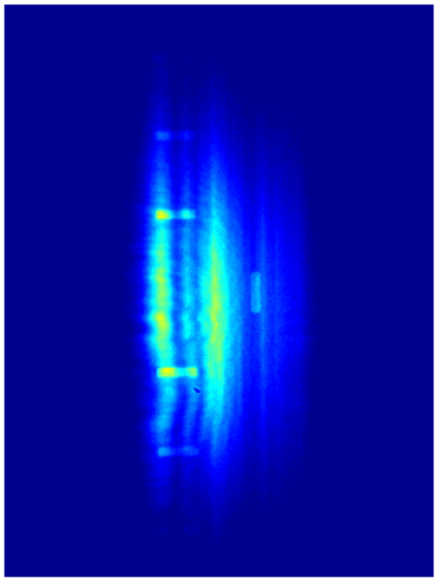


Detectors for FELs

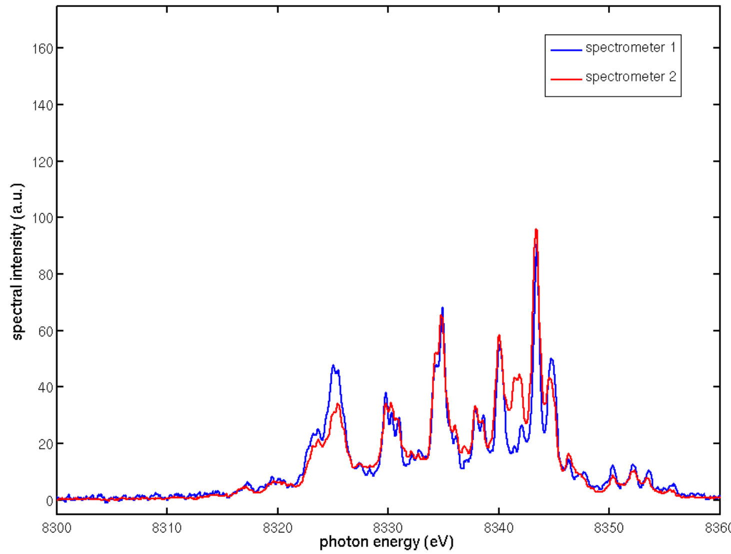
- Integrating
- Fast
- (typically) Wide dynamic range
  - Single photon sensitivity and large full well
- Soft (250 – 2,000 eV) and hard x-rays (4 – 12.8 keV)
- Challenging experimental setups
  - Compact, contamination, damage, etc.

Dealing with LCLS source fluctuations…

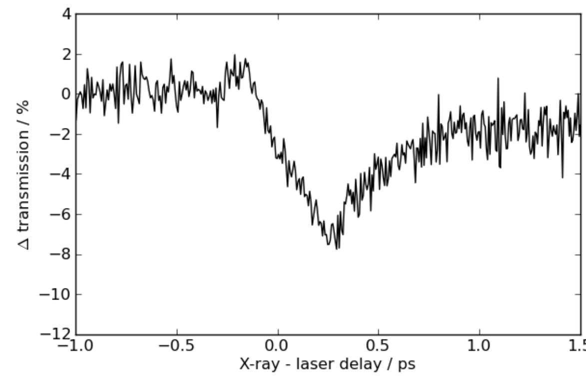
Spatial



Spectral



Temporal



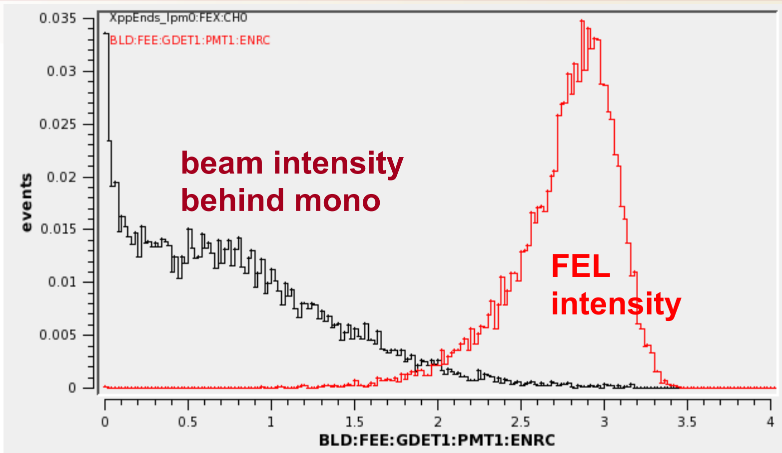
- Every pulse is different and must be diagnosed individually

Unstable sample

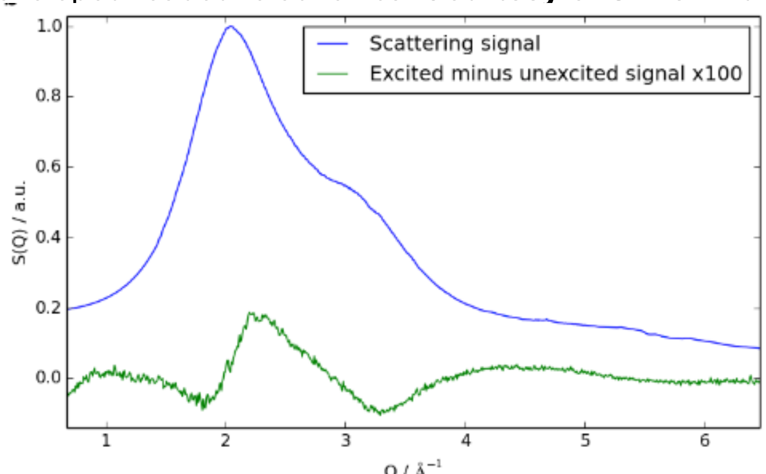
shot by shot readout of cameras and beam diagnostics required

Courtesy of David Fritz

…and be able to dig small effects



In red: intensity distribution measured with the gas detector. In black: intensity distribution downstream the monochromator measured with a PIPS diode (Canberra Inc.) and in-house developed readout electronics. **Courtesy of S. Herrmann.**

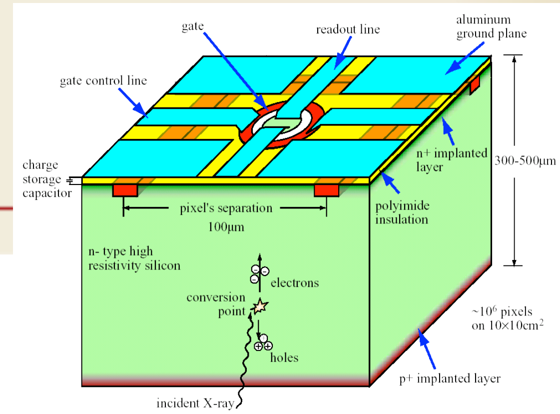


Typical solution scattering pump probe experiment: Azimuthally-averaged large dynamic range signal and measured difference signals (170 pulses average). **Courtesy of H. Lemke.**

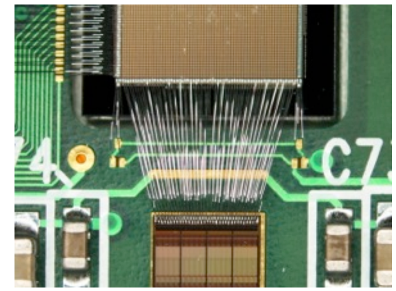
- Limitation for precision from averaging, co-adding, stacking: detector has to be *almost* perfect
  - Highly uniform across large areas
    - Tight linearity, homogeneous gain and crosstalk* constraints
    - Pixel size and position
    - Noise (Poisson and electronic)
- Averaging doesn't always reduce error
  - Significant calibration and optimization
  - Binning and data analysis
    - Need input from additional diagnostics

*At FELs all photons arrive at once >> electronics is more prone to crosstalk

First detectors for LCLS

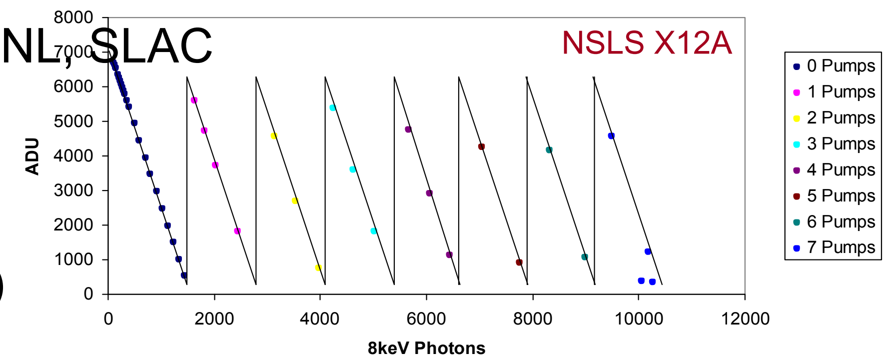


At LCLS three dedicated detector projects:



Monolithic sensor with wire-bonded electronics

- X-ray Active Matrix Pixel Sensor (XAMPS) – BNL
- X-ray Correlation Spectroscopy (XCS) – BNL, SLAC

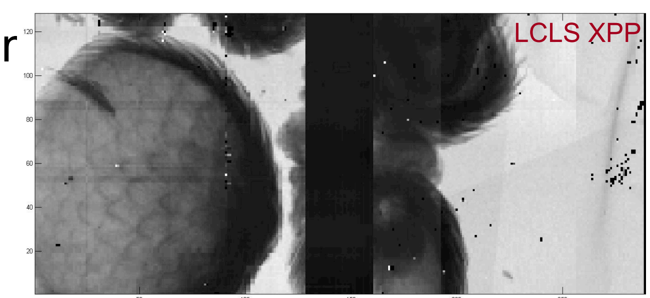


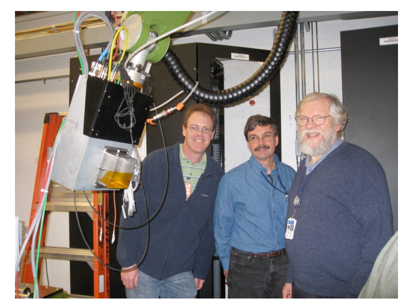
Pixel array detector

- Cornell-SLAC Pixel Array Detector (CSPAD)

Fast CCDs are a good fit for low noise, lir range applications

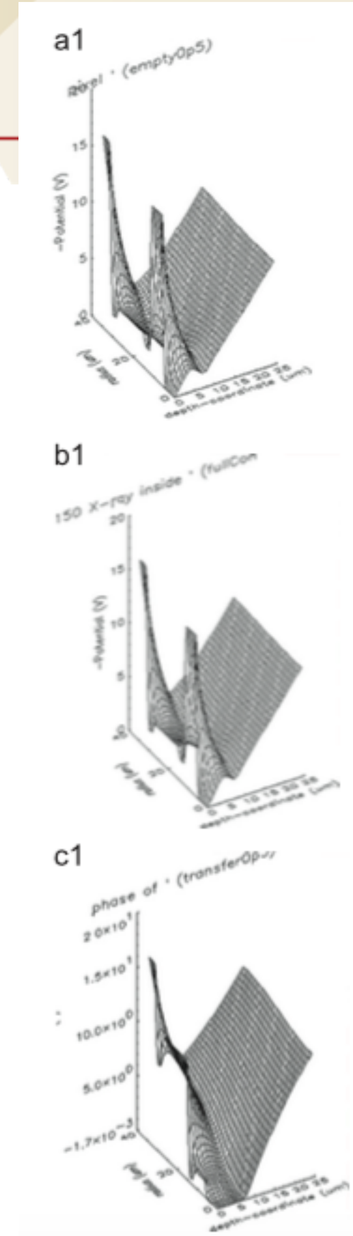
- pnCCD
- fCCD





Or for very intense signal when coupled with scintillator (e.g. Rayonix)

First detectors for LCLS



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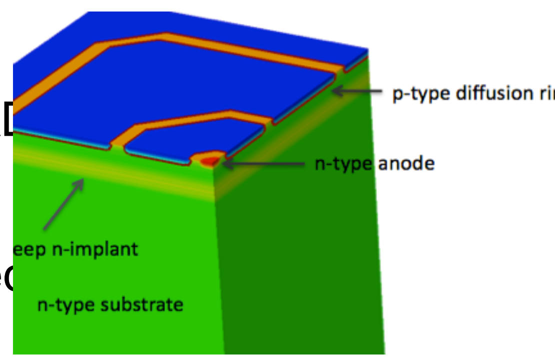
Pixel array detector

- Cornell-SLAC Pixel Array Detector (CSPAD



Fast CCDs are a good fit for low noise, limited range applications

- pnCCD
- fCCD

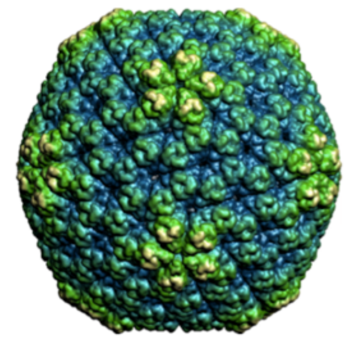
Or for very intense signal when coupled with scintillator (e.g. Rayonix)

pnCCD - LAMP

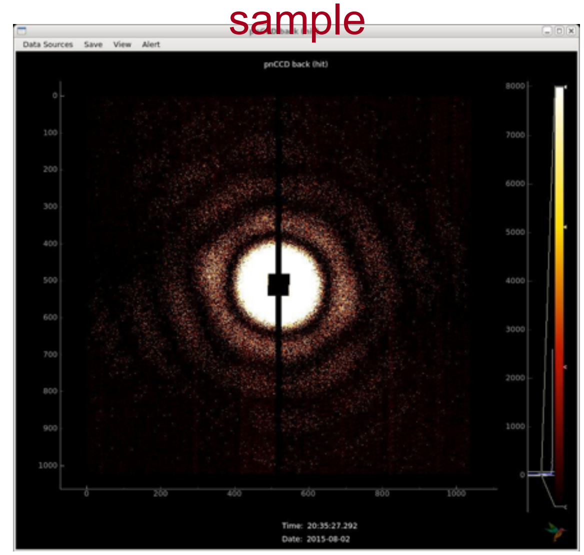
pnCCD: direct conversion, back-illuminated, fully depleted, x-ray CCD camera (based on a pn-junction CCD sensor)

- developed at the Halbleiterlabor (HLL - MPS, Germany).
- covers a large solid angle with a sizeable aperture between the two half planes of the front detector (LAMP chamber).
- typically used in soft x-ray experiments
- very delicate operation

Single Particle Imaging Initiative @ AMO



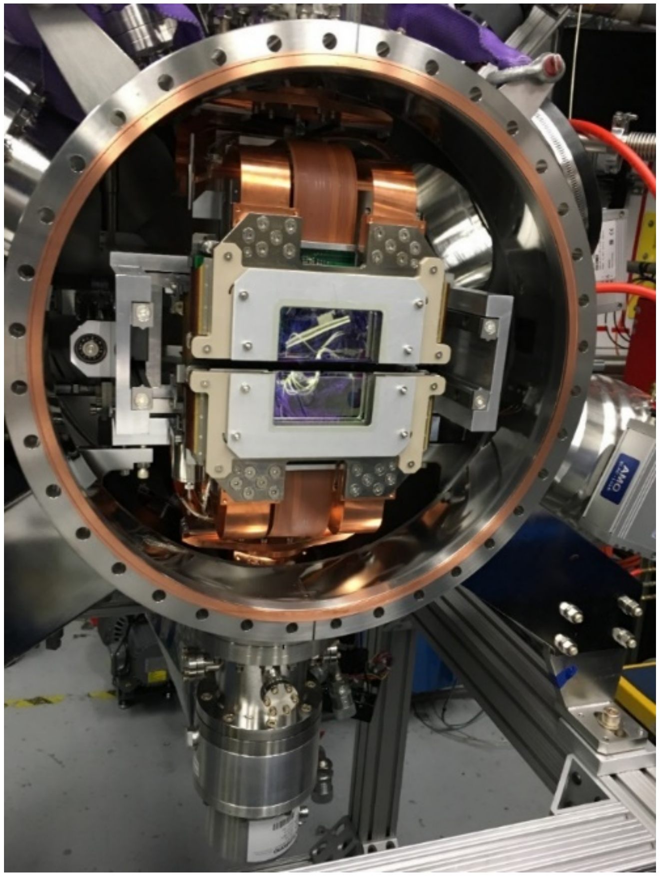
Rice Dwarf Virus ~80 nm
Single, reproducible model sample



Example single shot

Strueder *et al.* NIM A 614 (3) 483 (2010)

pnCCD - LAMP



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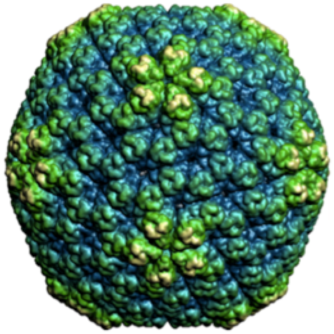

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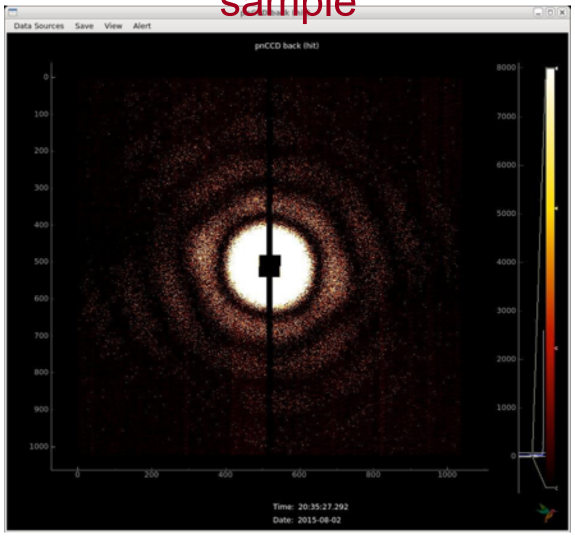
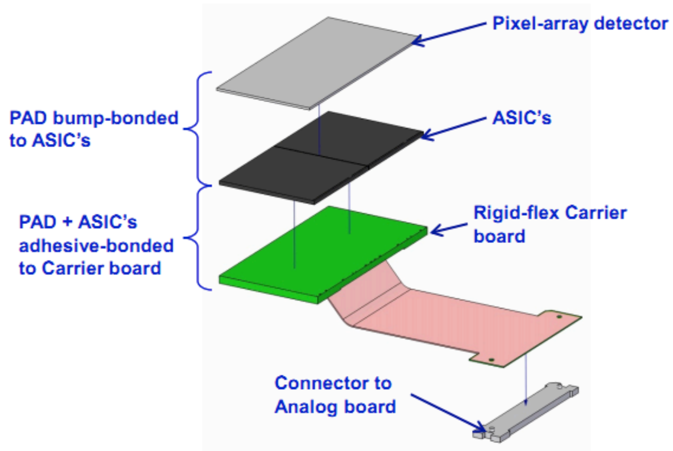


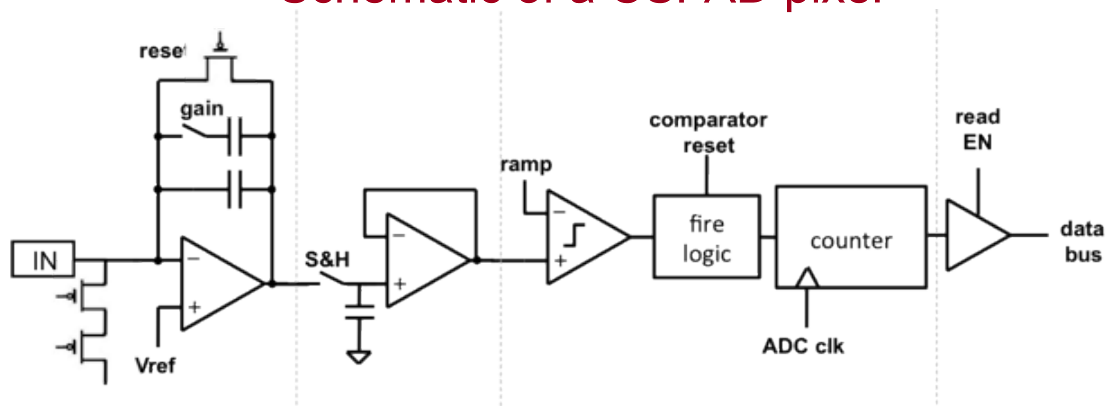
Example single shot

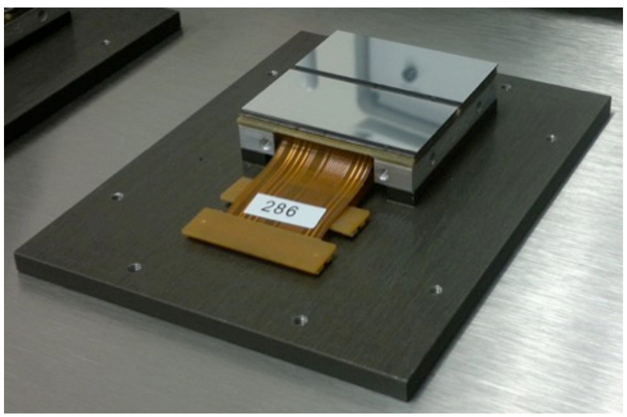
Cornell-SLAC Pixel Array Detector

SLAC



Schematic of a CSPAD pixel



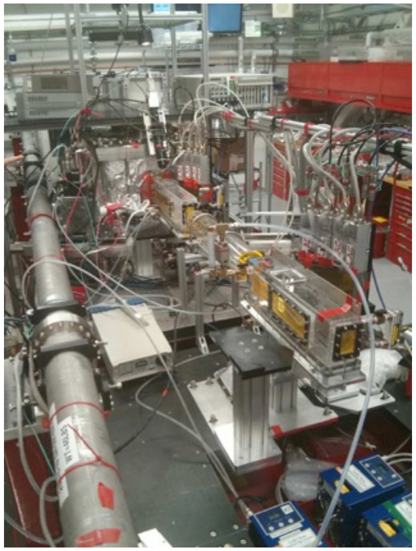


CSPAD	High Gain	Low Gain
Pixels per ASIC	194 x 185	
Pixel Size (µm)	110	
Noise r.m.s. (eV)	1,000	3,500
Maximum signal (8 keV equivalent)	350	2,700
Frame rate (Hz)	120	

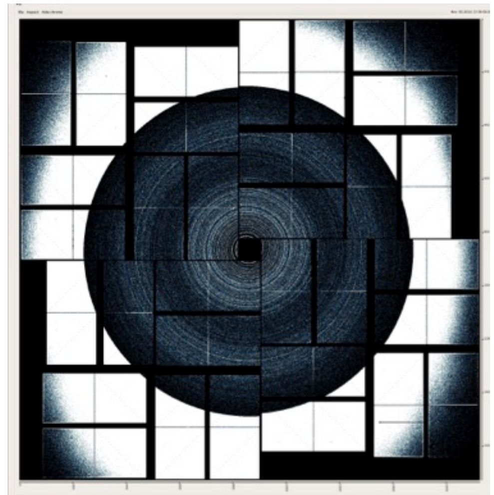
Koerner L J, Philipp H T, Hromalik M S, Tate M W, and Gruner S M 2009 *JINST* **4** P03001
Philipp H T *et al.* 2010 *IEEE Trans Nucl Sci* **57** 3795
Philipp H *et al.* 2011 *Nucl Instr Meth Phys Res A* **649** 67
Hart P A *et al. 2012 Proc SPIE* **8504** 85040C
Herrmann S C *et al. 2013 Nucl Instr Meth Phys Res A* **718** 550
Herrmann S C *et al.* J. Phys.: Conf. Ser. 493, 012013 (2014).

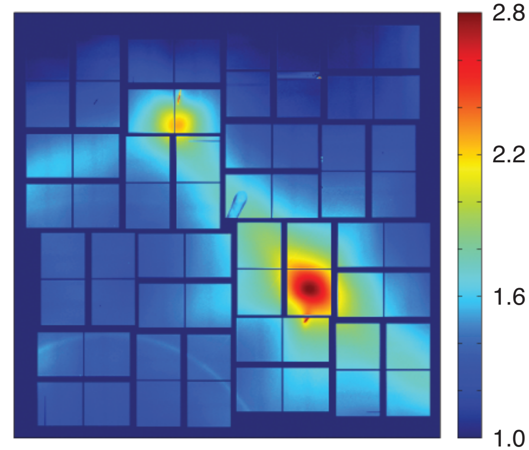
CSPAD cameras

Setup for non-linear Compton scattering experiment at CXI.

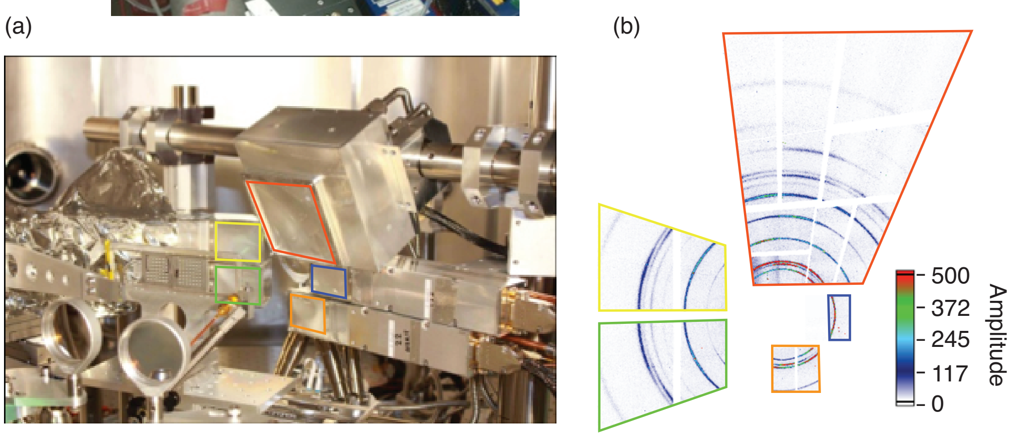


CXI camera with different gain settings. Courtesy of ***Sebastien Boutet.***

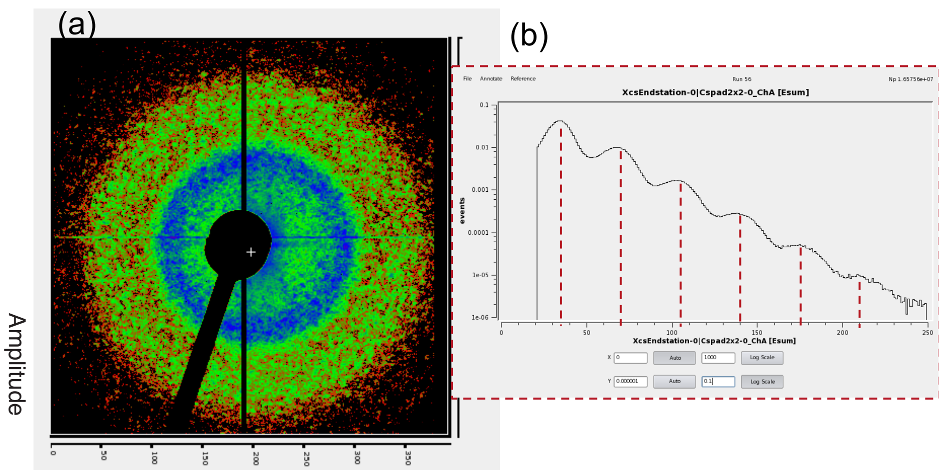




Static thermal diffuse scattering due to phonons in Ge. Courtesy of ***Mariano Trigo***.



(a) MEC chamber: experimental setup (b) Reconstructed diffraction rings from Ti samples at 10.2 keV in the various CSPAD panels. Courtesy of ***Cindy Bolme*** (Los Alamos Nat. Lab.).



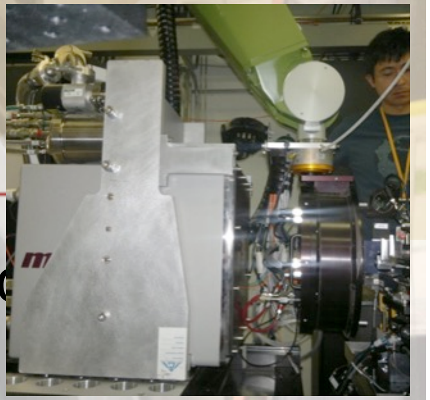
(a) Speckle pattern produced by colloidal suspension at the XCS instrument. (b) Reconstructed photon histogram.

CSPAD

- Cornell-SLAC PAD: first hybrid pixel array detector developed for an FEL.
  - Deployed as developed.
  - Needed a few iterations (characterization, new hardware, calibration, etc.) before reaching maturity.
  - 140k, 560k, 2.3Mpixelcameras

- Good general-purpose imaging detector but not sufficient to cover all needs

CSPAD



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ePix cameras to fulfill unmet needs

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High dynamic range applications: **ePix10k**

Detection of pump-probe and other small differential signals on large background, small angle scattering, femtosecond nanocristallography.

Low noise, high spatial resolution applications: **ePix100**

Detection of small scattering signals: e.g. speckle, diffuse scattering, large-***q*** scattering (large solid angle).

Blaj *et al.* J Synchrotron Radiat. 22 (3), 577–583 (2015)

ePix cameras to fulfill unmet needs

CSPAD	High Gain	Low Gain
Pixels per ASIC	194 x 185	
Pixel Size (μm)	110	
Noise r.m.s. (eV)	1,000	3,500
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Frame rate (Hz)	120	

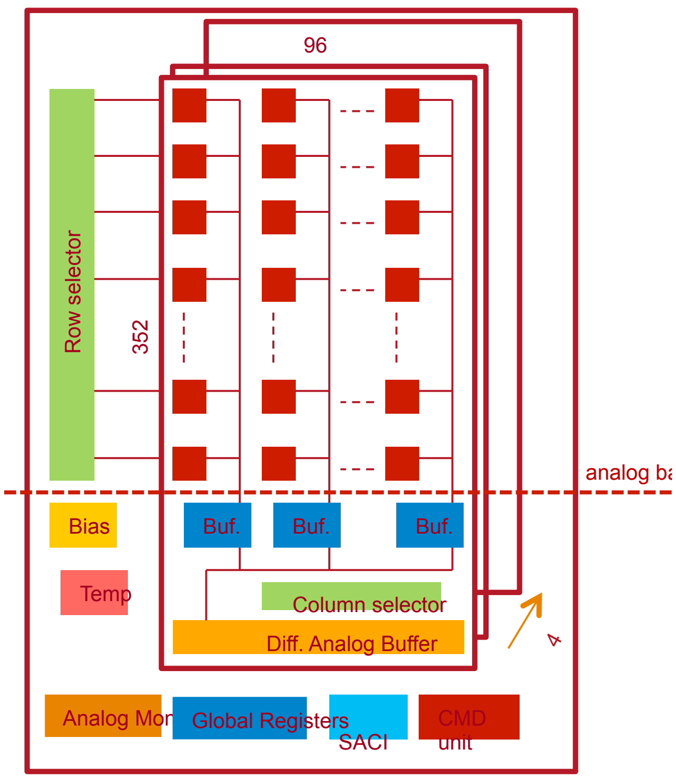
High dynamic range applications: **ePix10k**

ePix 10k prototype	High Gain	Low Gain
Pixels per ASIC	48 x 48	
Pixel Size (μm)	100	
Noise r.m.s. (eV)	650	10,800
Maximum signal (8 keV equivalent)	100	10,000
Frame Rate (Hz)	120	

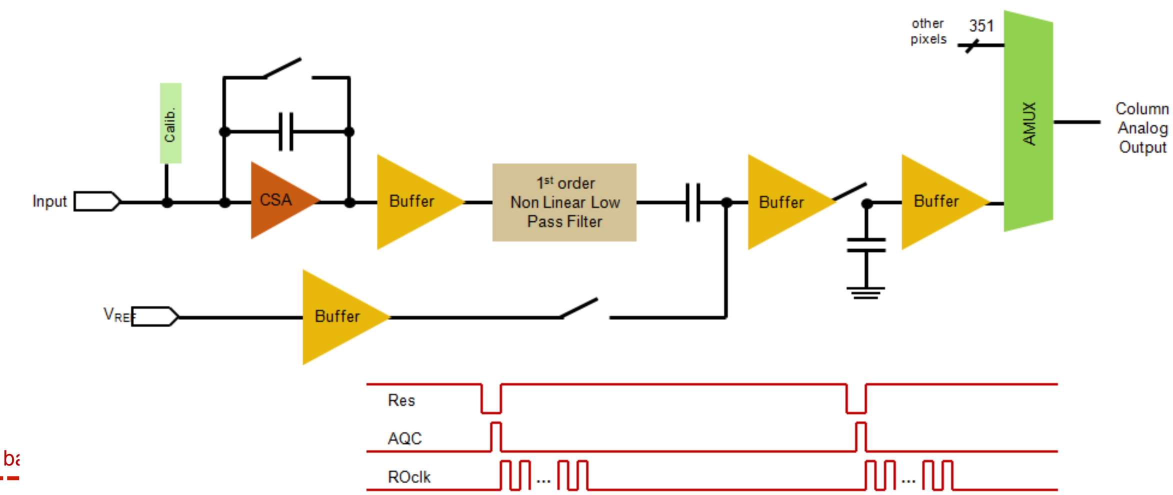
Low noise, high spatial resolution applications: **ePix100**

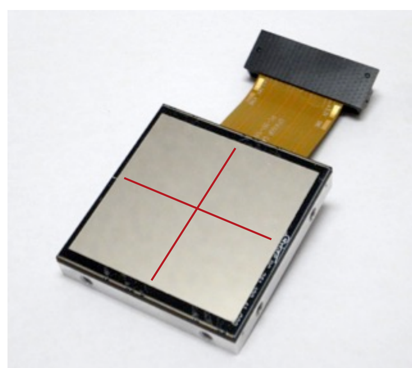
ePix 100	
Pixels per ASIC	384 x 352
Pixel Size (μm)	50
Noise r.m.s. (eV)	220
Maximum signal (8 keV equivalent)	100
Frame rate (Hz)	120

ePix100: a few details

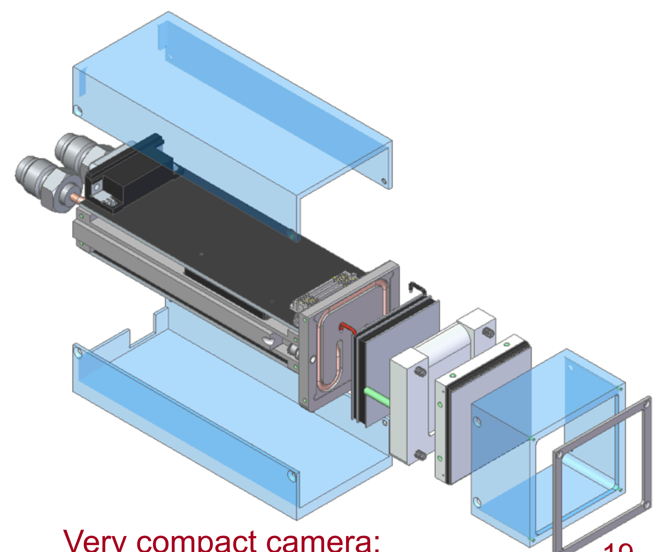


Signal Sampling Phase: Res is Low, AQC goes Low





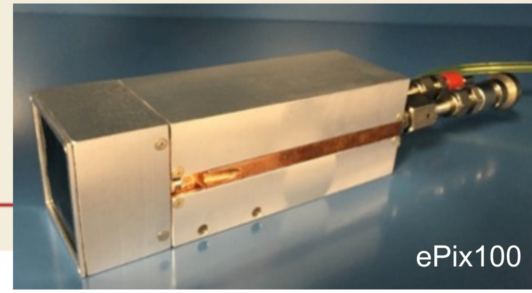
Sensor with 4 chips

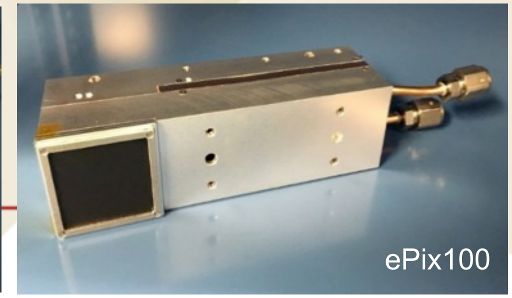


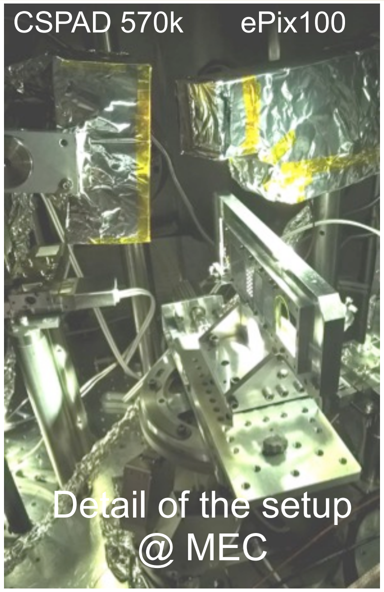
Very compact camera:
52 mm x 52 mm x 155 mm

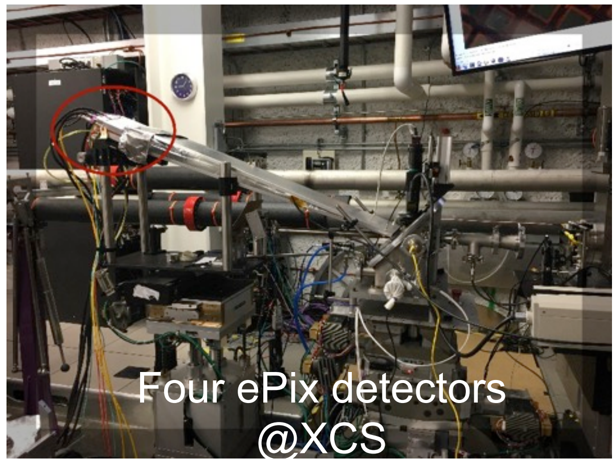
Dragone *et al*. J. Phys.: Conf. Ser. 493, 1–4 (2014)
Carini *et al.* AIP Conf. Proc. **1741**, 010001 (2016)
Nishimura *et al.* AIP Conf. Proc. **1741**, 010001 (2016)

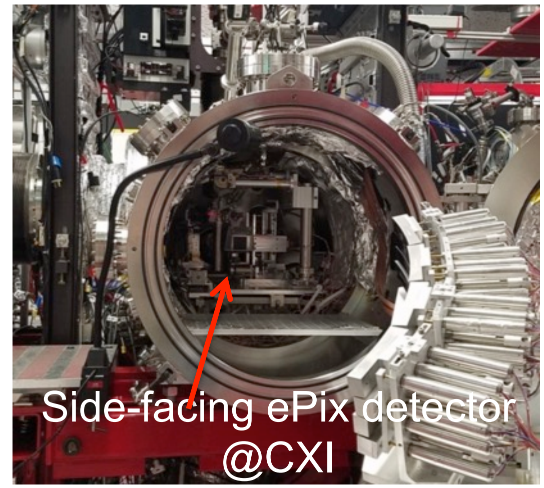
ePix100: first year

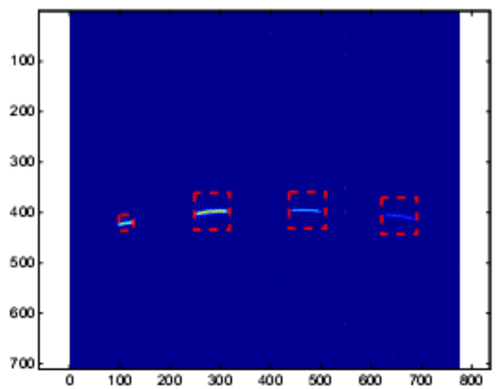




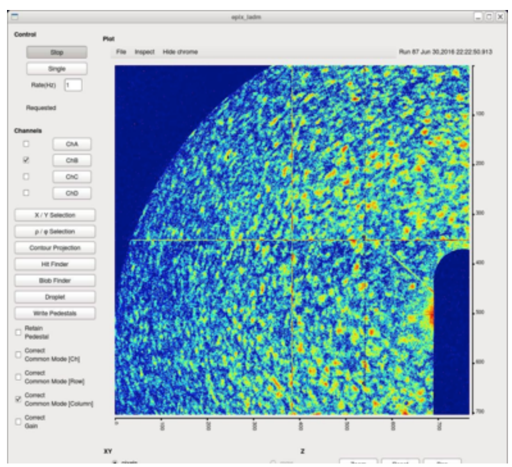




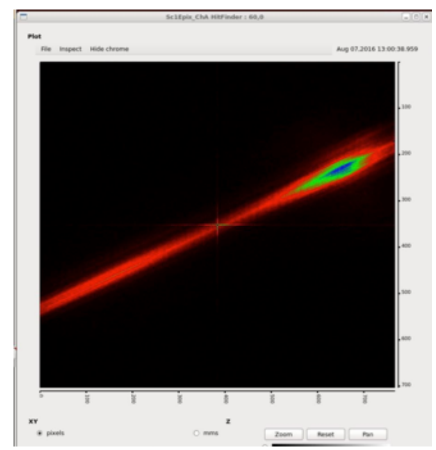




Ion acoustic waves in warm dense matter.
PI G. Monaco



Atomic-scale dynamics in liquids and glasses.
PI P. Fuoss



Fluorescence signal in coincidence with SFX measurements of photosystem II.
PI P. Fromme

LCLS-II

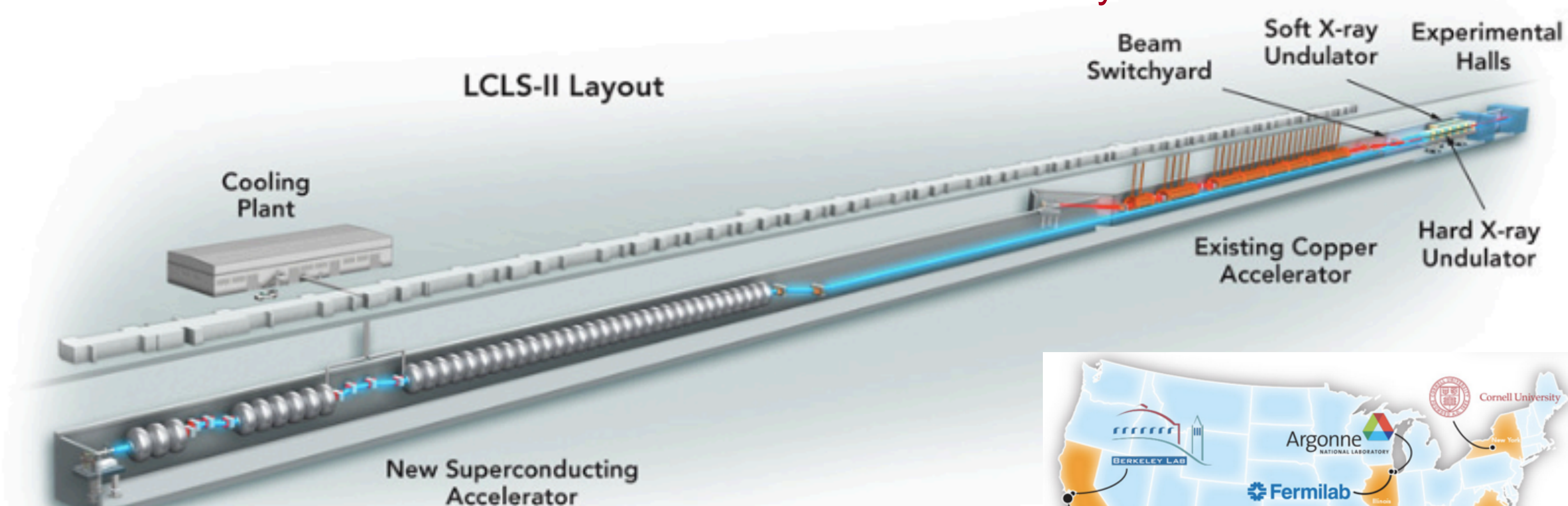
Supports the latest seeding technologies to provide fully coherent beam (at the spatial diffraction limit and at the temporal transform limit)

New 4 GeV superconducting linac in existing SLAC tunnel.

https://www.youtube.com/watch?v=t7jUZwhZdd0

LCLS-II

- Maintains the existing copper-based warm linac and upgrades parts of the existing research infrastructure to take advantage of the new configuration.
- Extends the operating range of the facility from its current limit of ~11 keV x-rays to ~25 keV.



New 4 GeV superconducting linac in existing SLAC tunnel.

THE LCLS-II DESIGN

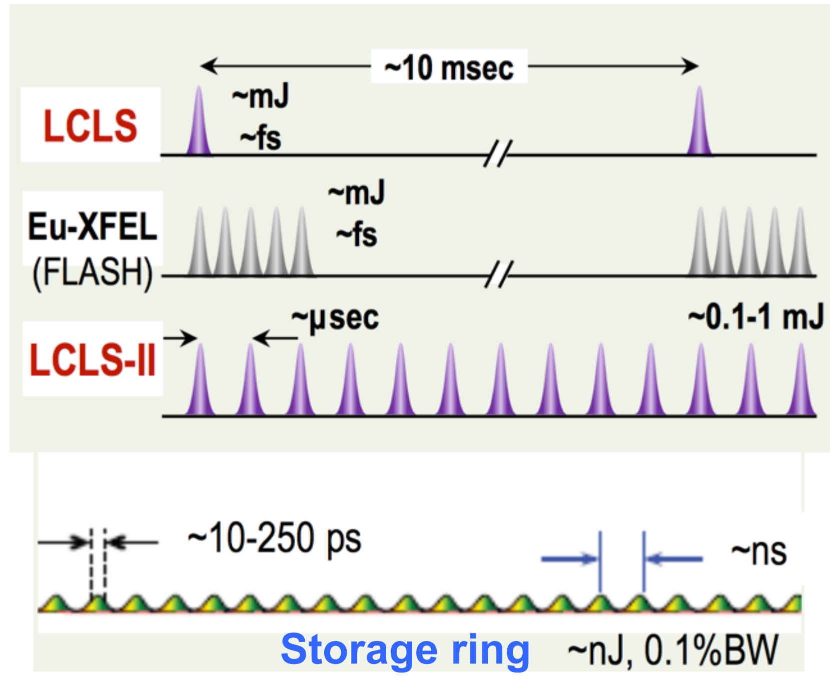
Replacing the existing undulator with two new ones.

https://www.youtube.com/watch?v=t7jUZwhZdd0

Exploiting new light sources capabilities

LCLS-II

- From 120 pulses per second to 1 million per second.
- It will be the world's only X-ray free-electron laser capable of supplying a uniformly-spaced train of pulses with programmable repetition rate.

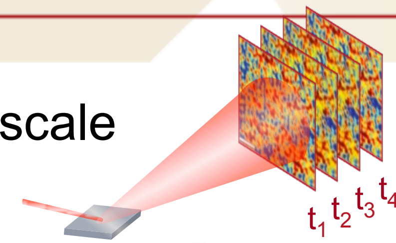


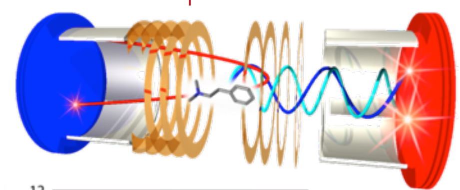
Toward higher coherent flux

- Other light sources upgrades: coherence and brightness.
- Some common needs: dynamic range and speed.

https://portal.slac.stanford.edu/sites/lcls_public/Documents/LCLS-IIScienceOpportunities_final.pdf

Detectors to Enable LCLS-II Science





Coherent Scattering, Imaging & Diffraction at the Nanoscale

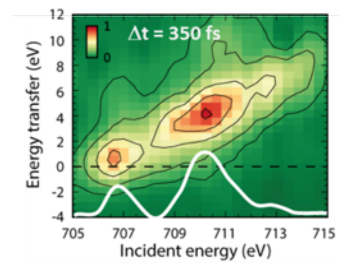
- High-speed 2D detector (multi-kHz)
- Soft X-ray (250 eV to ~2 keV), tender X-ray (up to 5 keV)

Fundamental Dynamics of Energy & Charge

- Molecular reaction microscope – 2D, MHz, e^-/ion TOF (multi-hit)
- Strong-field AMO – 2D e^-/ion TOF (multi-hit, 120 Hz)

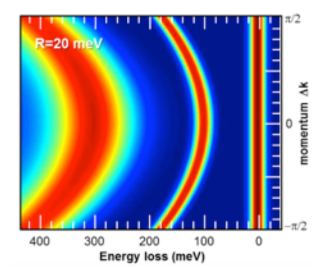
Catalysis, Photo-catalysis and Bio-spectroscopy

- Moderate resolution, high quantum (and collection) efficiency soft X-ray
- Energy-resolving detector (~0.5 eV), or 2D detector with spectrometer (pump/probe accumulating)



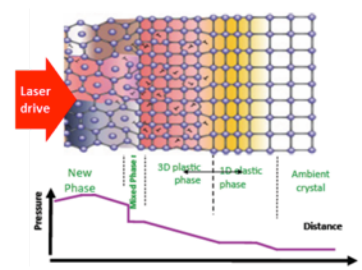
High-resolution Spectroscopy: Quantum Materials & Physical Chemistry

- 2D, high quantum efficiency soft X-rays
- Small pitch (~5 μm in energy dispersive direction) matched to high-resolution spectrometer (pump/probe accumulating)



Hard X-ray Scattering & Spectroscopy

- 2D, high quantum efficiency up to 25 keV, 120 Hz



Courtesy of Bob Schoenlein

Physics requirements for small angle forward scattering and coherent diffractive imaging experiments (LAMP)

SLAC

LCLS	Physics Requirements Document	
	Title: Forward Scattering Area Detector Physics Requirements Doc.	
	Document Number: L2SI-PR-0004-R0	Page 1 of 16

Document Approval:	Date Approved
Originator: William Schlotter SXD Scientist	
Originator: Timur Osipov, NEH 1.1 Lead Scientist	
Originator: Dipanwita Ray SXD Scientist	
Approver: Georgi Dakovski NEH 2.2 Lead Scientist	
Approver: Gabriella Carini L2S-I Detectors System Lead	
Approver: Nicholas Kelez L2S-I Dep. Director for Beamline Systems	
Approver: Mike Minitti (L2S-I Dep. Director for Instruments)	
Reviewers: David Fritz (L2S-I Director), Rebecca Armenta (LCLS Mechanical Engineer), John Joseph (LBNL), Peter Denes (LBNL), Jean-Charles Castagna (NEH 1.1 Engineer), Dan Flath (Controls), Jana Thayer (Data Systems), Ian Evans (Safety Systems),	

Revision History

Revision	Date Released	Description of Change
R0	01/17/2017	Original Release.

Detector needs for LAMP:

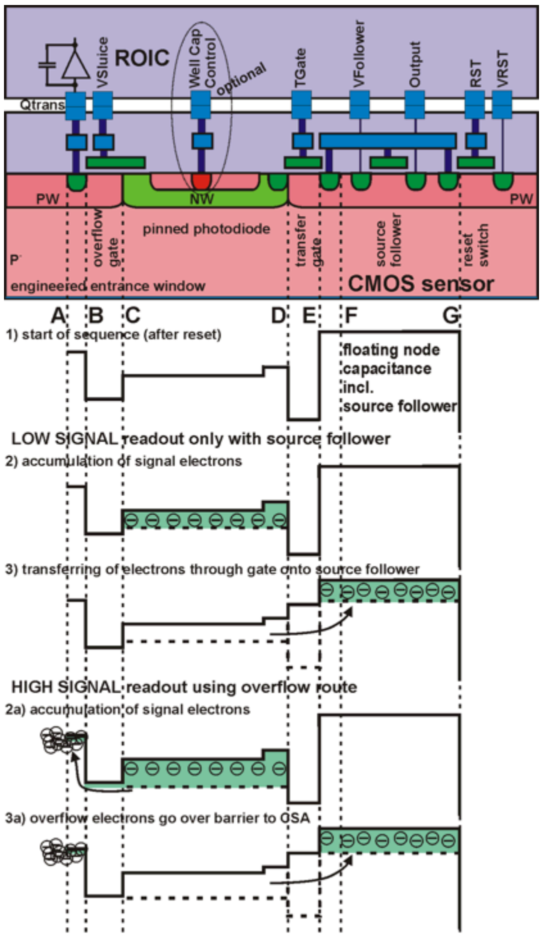
- 2D fast detector > 10 kHz (5 kHz)
- Large area: 10 cm x 10 cm (4 Mpixel)[1]
- ~50 μm × 50 μm pixel size (*square*)
- Sensitivity <1 ph (250 eV)
- Maximum signal 1000 ph /pixel/pulse
- High quantum efficiency in the soft

x-ray range[2]

[1] Detector dead edge: 1.25 – 1.5 mm

[2] Often limited by experimental conditions: filters to protect detector from samples, intense optical lasers, very high temperature, etc.

FLORA: A 3D-Integrated CMOS Detector for Imaging Experiments at LCLS-II



FLORA (**F**ermilab-**L**CLS CM**O**S 3D-integ**R**ated detector with **A**utogain)

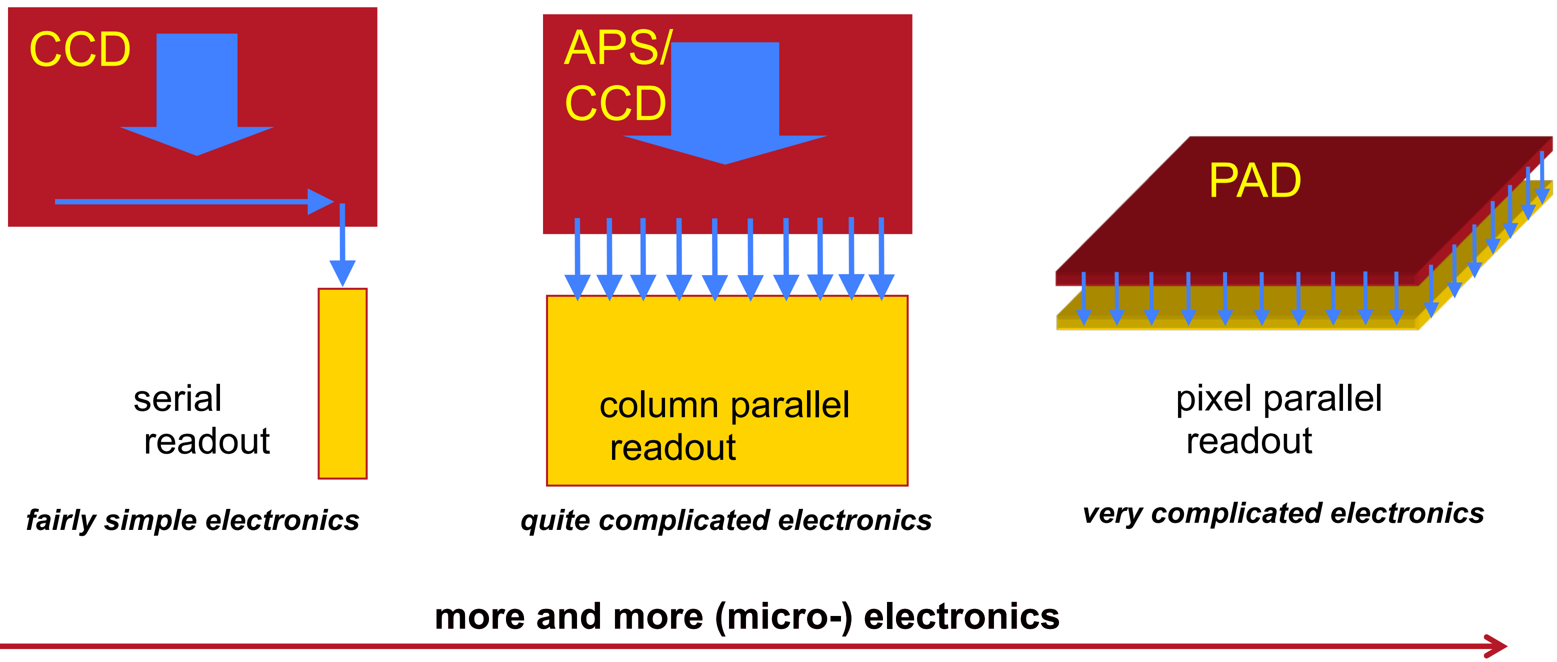
- ***To exploit high rep-rate operation at LCLS-II***
- Focus development for soft x-rays
- Concept extendable to hard x-rays
- Useful for other photon sources (rings and FELs)

- SLAC + Fermilab co-development

PI's G. Carini, G. Deptuch

Team: Farah Fahim, Philip Hart, Kaz Nakahara, Tom Zimmermann,

Speed and parallelization



For a given frame rate ***n*** fold parallelization relaxes the speed requirement for a pixel by the factor ***n***

Noise, speed, power

SLAC

thermal white noise — 1/f noise — leakage current noise

$$ENC^2 = \frac{a}{\tau} C_T^2 A_1 + 2\pi a_f C_T^2 A_2 + b\tau A_3$$

$$SNR = \frac{e_{\max}}{ENC} = 2^{ENOB}$$

$$ENC \sim C_T$$

$$ENC \sim \sqrt{\frac{1}{\tau}}$$

- doubling the speed increases noise by √2

white noise of a single MOSFET

$$a = \overline{n_{in}^{\,2}} = 4kt\gamma \frac{1}{g_m}$$

$$g_m = \sqrt{2\mu C_{ox}\left(\frac{W}{L}\right) I_{DS}}$$

$$ENC \sim \sqrt{\sqrt{\frac{1}{I_{DS}}}}$$

- to reduce the noise by √2 a power increase of factor 4 is needed

***very simplified : assuming sensor system to be white noise dominated by first input transistor of given geometry**

Pixel array detectors: two approaches

SLAC

- Fully CMOS detectors
  - CMOS Monolithic Active Pixel Sensors (MAPS).
  - CMOS Silicon On Insulator (SOI).
- *Process technology not optimal for different functionalities.*

- Hybrid pixel detectors
  - Sensors in high resistivity silicon
    - e.g. Pixel Array Detectors (PAD), DEpleted P-channel Field Effect Transistor (DEPFET).
  - Readout chip in low resistivity silicon - standard IC technology.
- *Process technologies optimized for different functionalities.*

…and combination of the above

Divide and conquer

Optimized CMOS Imager Sensor

- handles small and large signals simultaneously via separate paths
- back-side illuminated with engineered entrance window for soft x-rays
- built in commercial foundry using existing (~) OPTO-type process
- simple sensor (almost no ROIC transistors), seamless/multiple reticle stitching

Compatible ROIC ASIC

- simultaneous analog processing of signals from two paths
- in-situ digitization
- single photon sensitivity
- 10 kfps speed or better
- compatible with D2W bonding onto sensor wafer of sensor slab with multiple connections per pixel
- advanced process node

Advanced interconnects: 3D assembly/interposer

- exploiting good features of both technologies
  - multiple metal layers on sensor/interposer for routing
  - yield-optimized size of ROIC ASICs

Stacked Imagers

SLAC

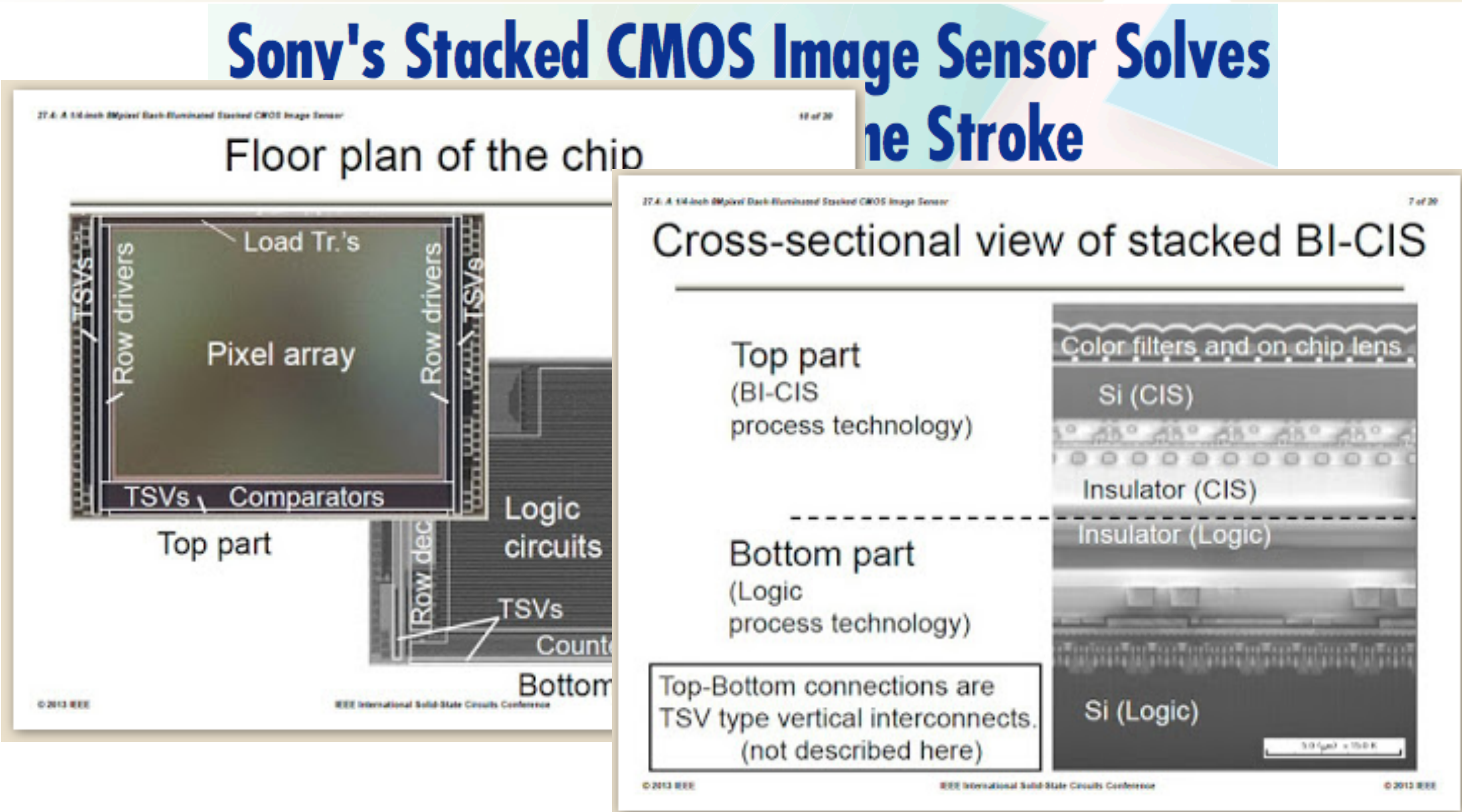
Sony's Stacked CMOS Image Sensor Solves All Existing Problems in One Stroke

In conventional CMOS image sensors, the pixels (sensors) and circuits (logic) are formed on the same silicon substrate.
Like oil and water, this coexistence of two conflicting elements makes it difficult to optimize their characteristics and also imposes other constraints.
The "stacked CMOS image sensor*1", a new generation of the back-illuminated CMOS image sensor, developed by Sony solves these problems in one stroke.
Stacking the pixel section and the circuit section enables compact size, high image quality, faster speeds and flexible integration of versatile functions.
Through this technology, Sony has created functions that will enable differentiation of final products to provide new ways of enjoying images.

*1: See press release at: http://www.sony.net/SonyInfo/News/Press/201201/12-009E/

Stacked imagers can be found in: Fujitsu tablet, Samsung Galaxy S4, iPhone 4s – 5, etc.
Being explored for x-rays: http://rsc.riken.jp/pdf/SPring-8-II.pdf

Stacked Imagers



Stacked imagers can be found in: Fujitsu tablet, Samsung Galaxy S4, iPhone 4s – 5, etc.
Being explored for x-rays: http://rsc.riken.jp/pdf/SPring-8-II.pdf

Project genesis and proposal

IEEE-NSS
San Diego, 2015

- 50 μm × 50 μm pixel size, sensor thickness > 100 μm
- Low noise ~10 e^- ENC r.m.s.
  - Built-in adaptive gain
  - Single photon resolution (in the whole energy range of interest from 0.25 - 2.0 keV)
- Large dynamic range ~10^4
  - Maximum signal ~500 ke^-/pixel/pulse
- Fast frame readout
  - 10 kHz with path towards higher effective frame rate
- High quantum efficiency in the soft X-ray range (0.25-2.0 keV)
- The concept can be extended to higher photon energies.
- Large, up to 10×10 cm^2, area (tileable) with central hole
- High vacuum compatible

Proposed approach

IEEE-NSS
San Diego, 2015

- Leveraging team expertise
- Leveraging good components of demonstrated technologies
- Add some features + stay within industrial fabrication
- Optimize both components, i.e. sensor and ASIC simultaneously

Stacked Imager: FLORA

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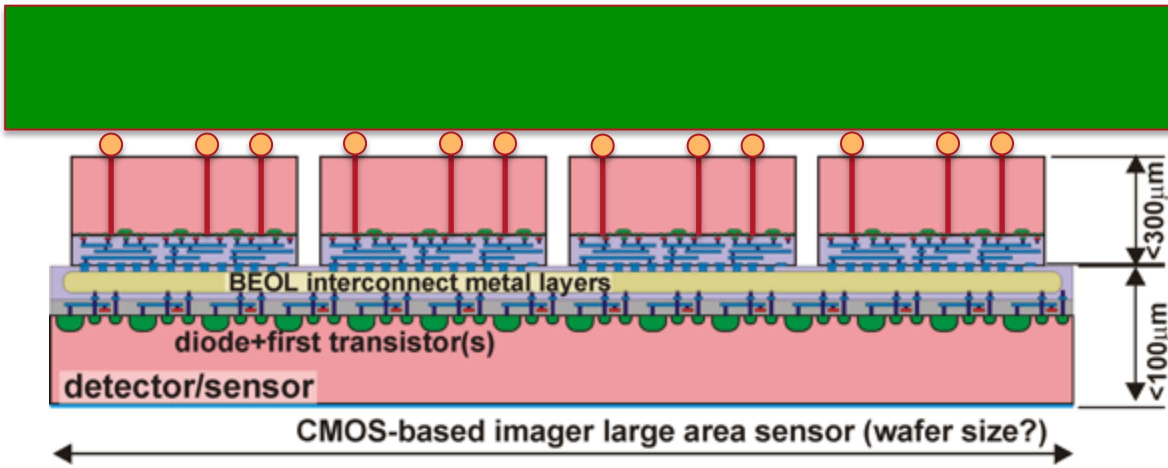


HDI module carrier

RO ASICs
(from donor wafer for D2W)

Large area CMOS imager
on HR Silicon
(host substrate for D2W)

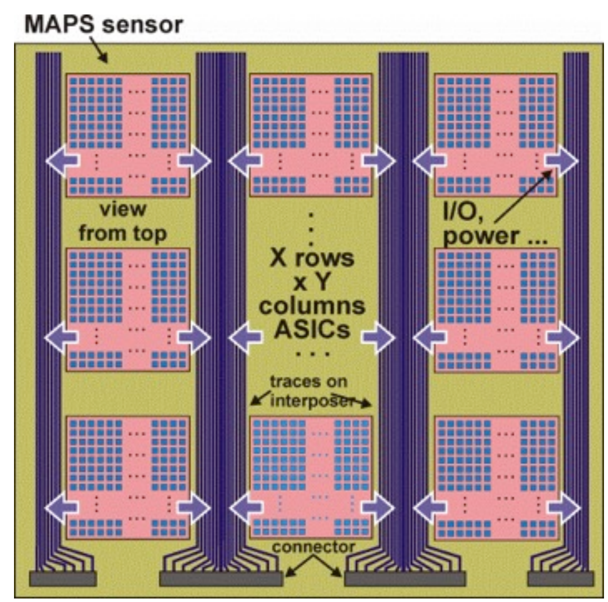
Go beyond the performance achievable with conventional detector technology

Approach: Hybrid CMOS imager (i.e. state-of-the-art imagers in cell phones)

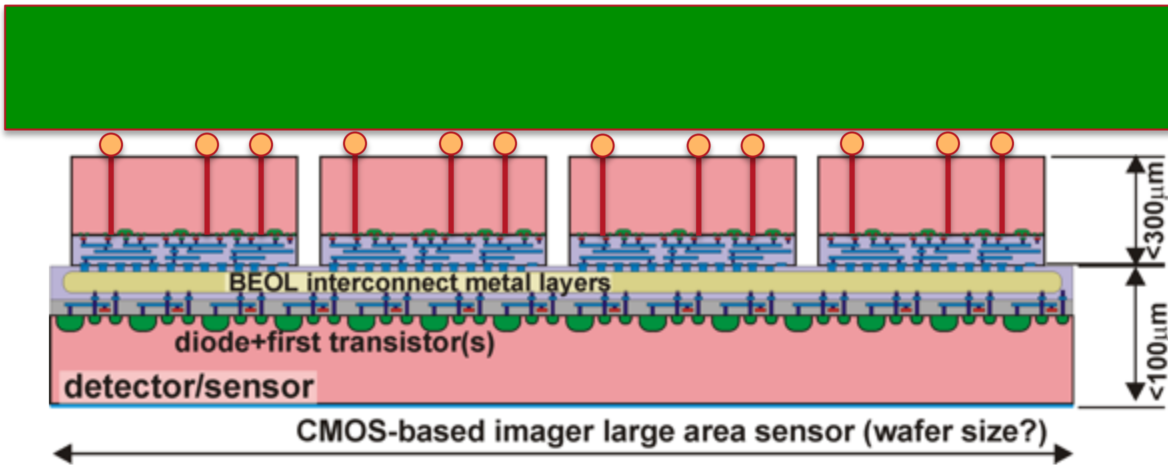
Simple CMOS sensor:
- Large area and high yield

Complex electronics:
- Standard IC technology

Advanced interconnects:
- 3D or integrated electronics
  - Low noise, low power, high speed



Stacked Imager: FLORA



HDI module carrier

RO ASICs
(from donor wafer for D2W)

Large area CMOS imager
on HR Silicon
(host substrate for D2W)

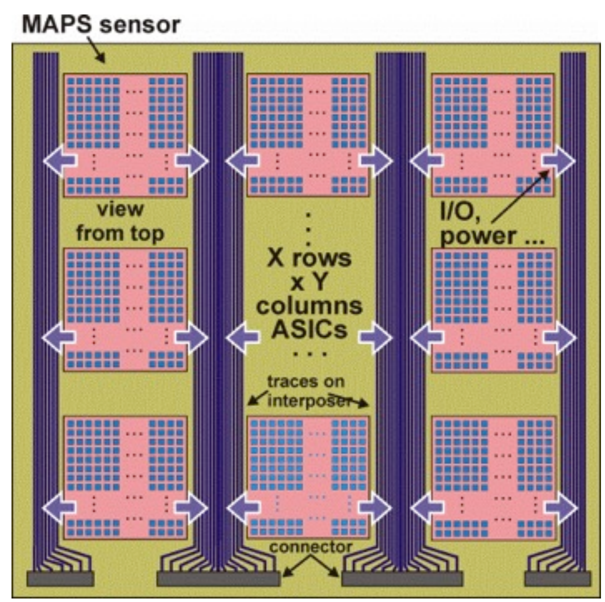
Multi-directional optimization

Optimization of signal processing:

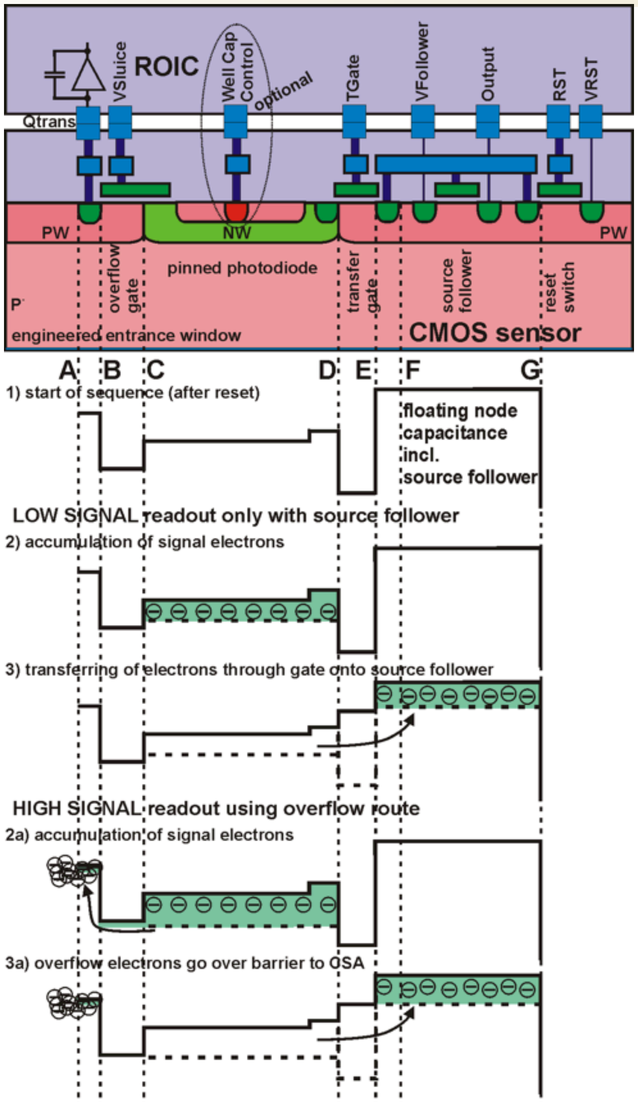
- Implementation of optimization features in both sensor and ROIC ASIC

Optimization of the detector form:

- Sensor larger than ASIC
- Multiple smaller ASIC connected to the sensor
- High fill factor



X-rays, charges, signal flow



- Charges are collected in the photodiode
- Readout uses two steps and two paths
- Overflow charge flows in the low sensitivity node and is collected by a charge sensitive amplifier in the ROIC
- Remaining charge is moved towards the high sensitivity node which utilizes on-sensor amplifier

Sensor: x-rays and optical applications

SLAC

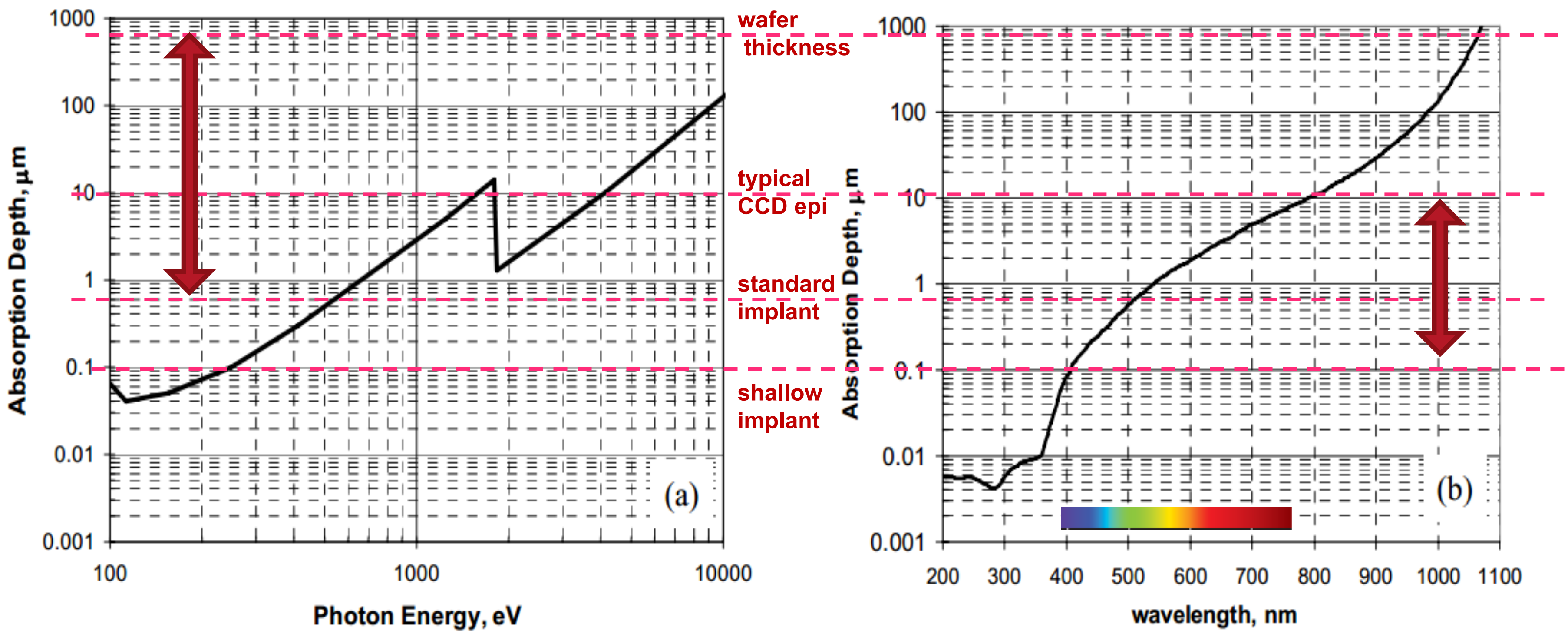
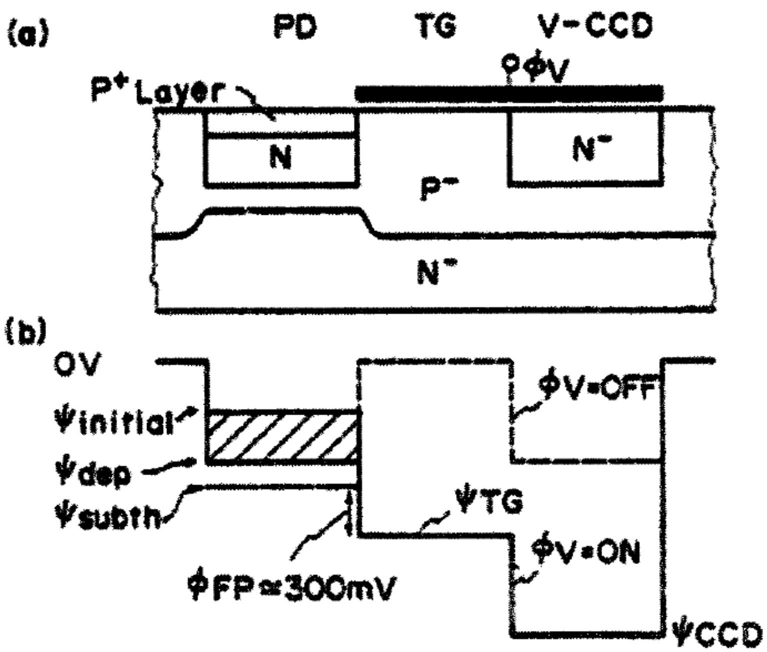


Fig. 7: Absorption depth of photons in silicon as a function of: (a) X-ray energy and, (b) the wavelengths from UV to NIR

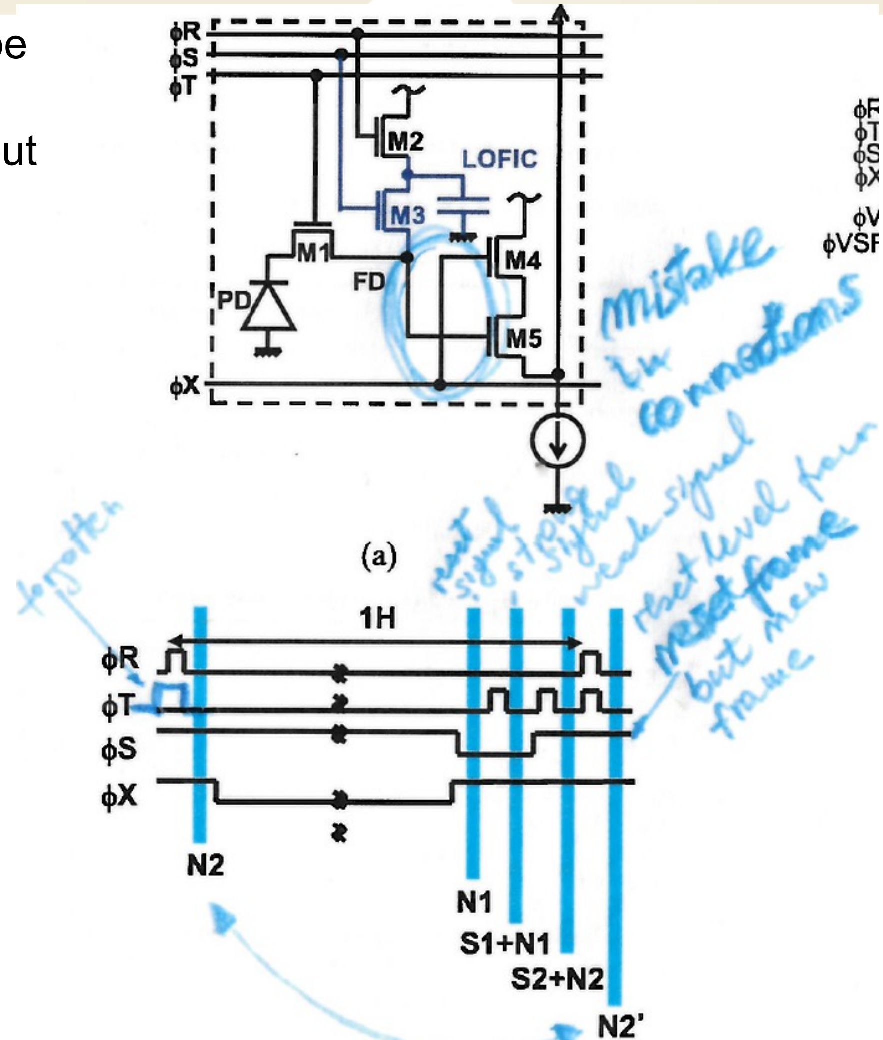
Yibin Bai et al, *Teledyne Imaging Sensors: Silicon CMOS imaging technologies for x-ray, UV, visible and near infrared*, SPIE Vol. 7021 (2008)

High Dynamic Range (**HDR**)/ Lateral Overflow Integration Capacitor (**LOFIC**) – charge sluice solution

1) pinned photodiode or buried floating diffusion type charge collecting element in pixel
2) transfer gate to floating diffusion node and readout chip through source follower – small Qs
3) overflow path (LOFIC/HDR) – large Qs
4) commercial CMOS Imager Sensor foundry



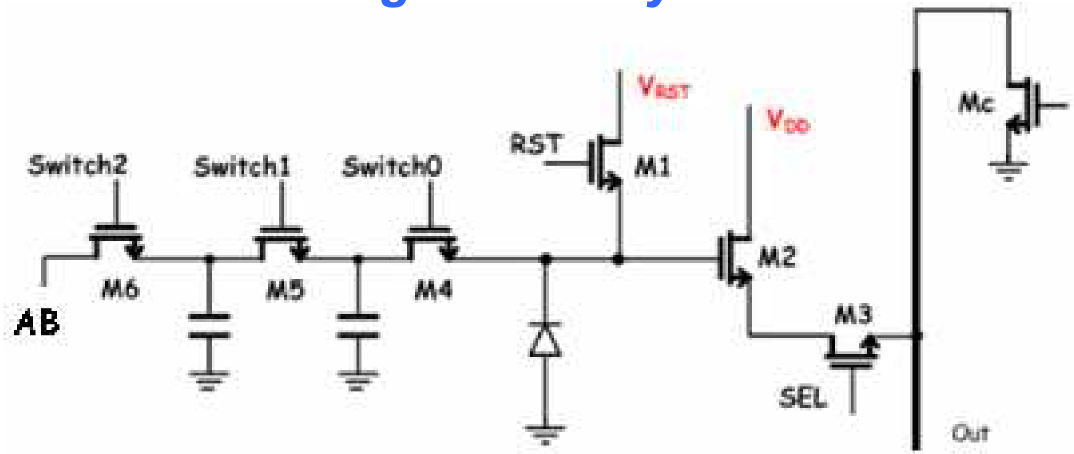
N. Teranishi, et al., "No image lag photodiode structure in the interline CCD image sensor", in Proc. IEDM, Dec. 1982, pp 324-327

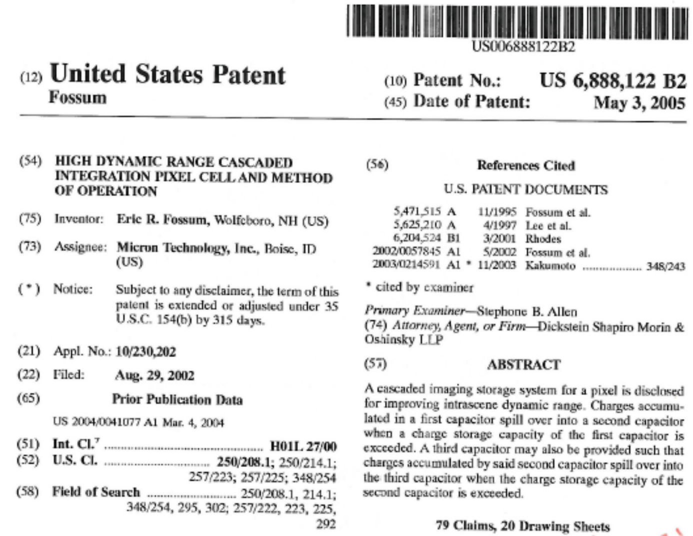


K. Mizobuchi, et al., "4.5 um Pixel Pitch 154 ke- full Well Capacity CMOS Image Sensor", 2009 IISW, Bergen, Norway, June 25-28, 2009

Example: PERCIVAL*

overflow charge for X-rays is useful!





US006888122B2

(12) **United States Patent**
Fossum

(10) **Patent No.: US 6,888,122 B2**
(45) **Date of Patent: May 3, 2005**

(54) **HIGH DYNAMIC RANGE CASCADED INTEGRATION PIXEL CELL AND METHOD OF OPERATION**

(75) Inventor: **Eric R. Fossum**, Wolfeboro, NH (US)

(73) Assignee: **Micron Technology, Inc.**, Boise, ID (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 315 days.

(21) Appl. No.: **10/230,202**

(22) Filed: **Aug. 29, 2002**

(65) **Prior Publication Data**

US 2004/0041077 A1 Mar. 4, 2004

(51) **Int. Cl.**[7] **H01L 27/00**
(52) **U.S. Cl.** **250/208.1**; 250/214.1; 257/223; 257/225; 348/254
(58) **Field of Search** 250/208.1, 214.1; 348/254, 295, 302; 257/222, 223, 225, 292

(56) **References Cited**

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6,204,524	B1	3/2001	Rhodes	
2002/0057845	A1	5/2002	Fossum et al.	
2003/0214591	A1 *	11/2003	Kakumoto	348/243

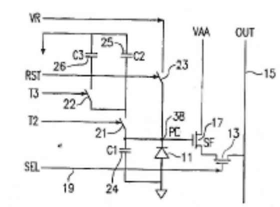
* cited by examiner

Primary Examiner—Stephone B. Allen
(74) *Attorney, Agent, or Firm*—Dickstein Shapiro Morin & Oshinsky LLP

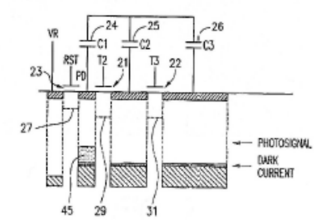
(57) **ABSTRACT**

A cascaded imaging storage system for a pixel is disclosed for improving intrascene dynamic range. Charges accumulated in a first capacitor spill over into a second capacitor when a charge storage capacity of the first capacitor is exceeded. A third capacitor may also be provided such that charges accumulated by said second capacitor spill over into the third capacitor when the charge storage capacity of the second capacitor is exceeded.

79 Claims, 20 Drawing Sheets



BASIC CONFIGURATION



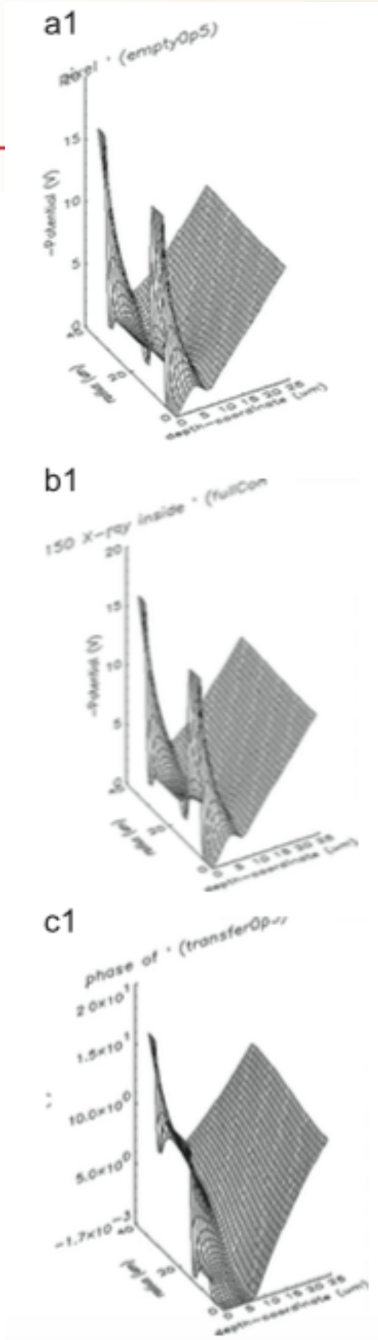
INITIAL INTEGRATION

CMOS imager based on a photodiode with a chain of capacitors collecting overflow charge and eventually read out through a source follower

- solution equivalent to industry standards HDR or LOFIC
- technology patented E. Fossum US 6,88,122 B2
- leverages commercial imaging technology, pushes to the limits monolithic approach
- ***SLOW!*** Because to read one pixel multiple clocking is necessary

*A. Marras, “Percival CMOS Imager”, FEE 2016, May 30 – June 3 2016, Krakow, Poland

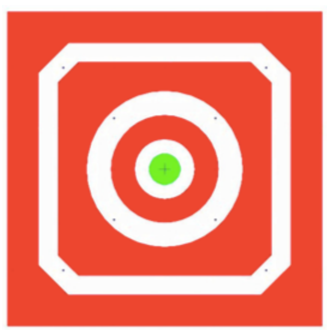
Sensor



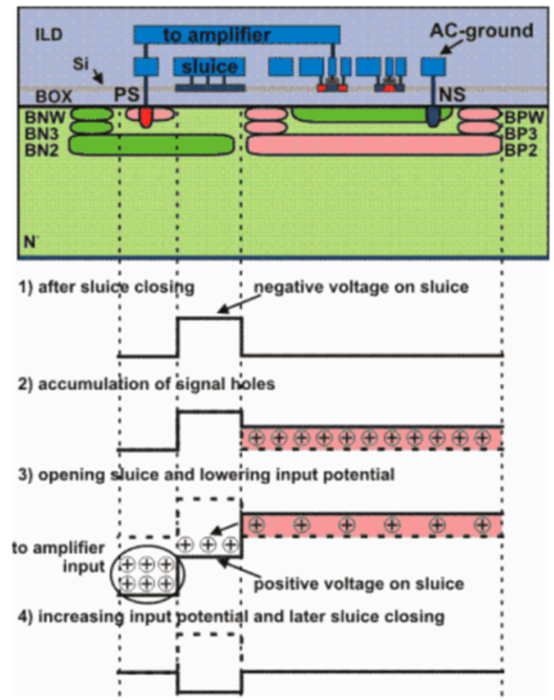
The solution resembles others proposed in the past

Left: collection and transfer of electric charge within the same pixel to a node performing the conversion to the voltage or current signal

- similar to the operation of Charge Coupled Devices
- *realized in a fully customized way*



Carini, **Rehak** *et al.* Nucl. Instr. Meth. A, 649 (2011) 75 –77



Top: charge sluice in monolithic SOI MAPS

Deptuch *et al.* internal communications

Sensor

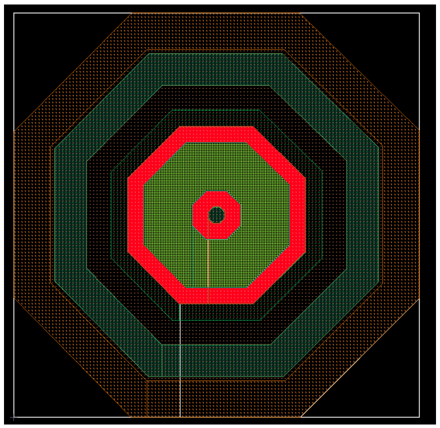
SLAC

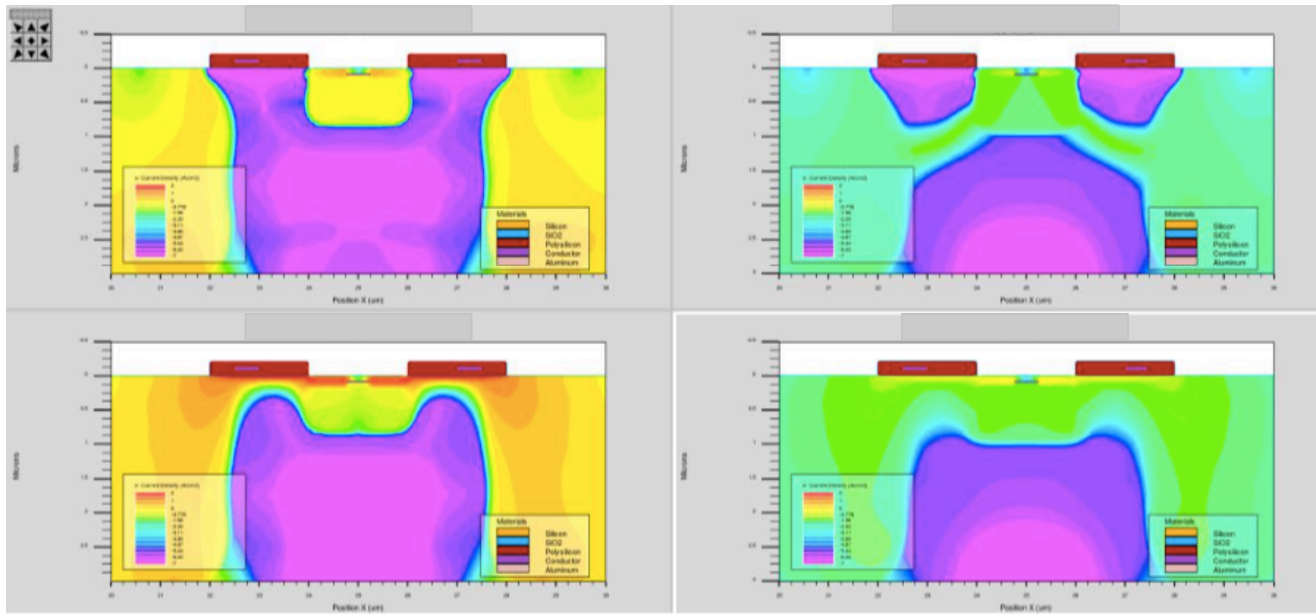
- **Identified candidate technology**
- **Established legal environment for industrial relationships (NDAs)**
- **Established industrial liaison**

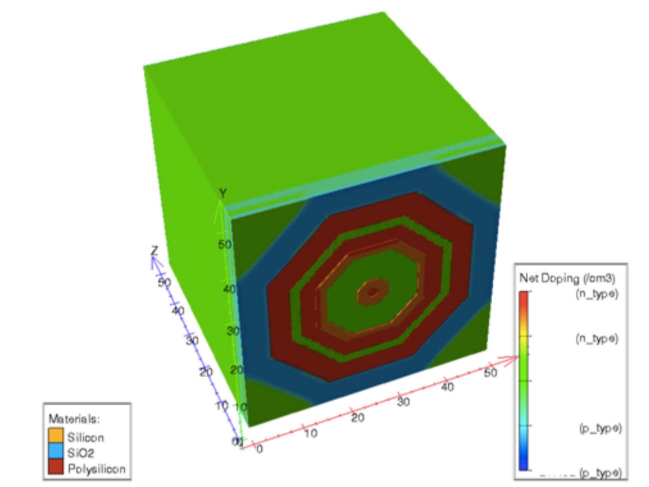
- **Studies (TCAD simulations):**
  - pinned photodiode or some sort of floating buried diffusion
  - implementation in HR substrate to be operated fully depleted
  - engineering of transfer gate and overflow (charge sluice) gates (size, channel doping, built-in field, size and photodiode location, etc.)
  - implement any full well capacity control
  - validate process technology features
  - **and certainly some more…**

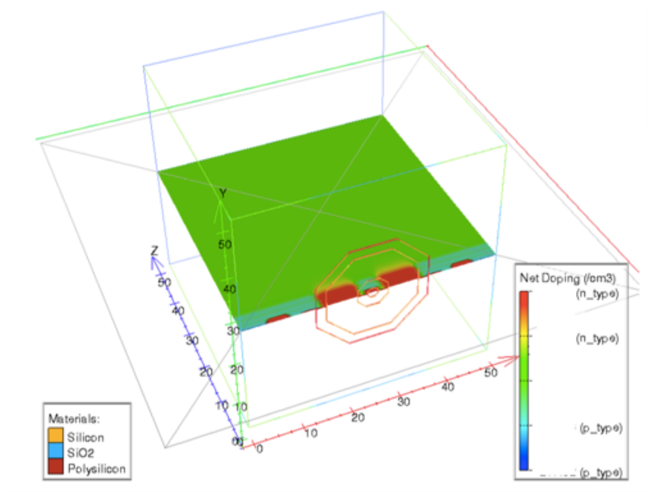
Goal for this ADR phase (first year): test 'sensor-only' (on-sensor readout) with x-rays

Sensor – pixel layout and TCAD simulations

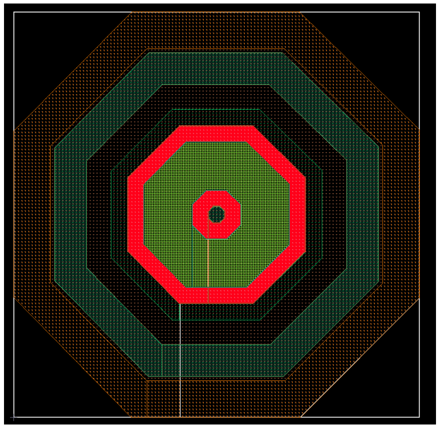


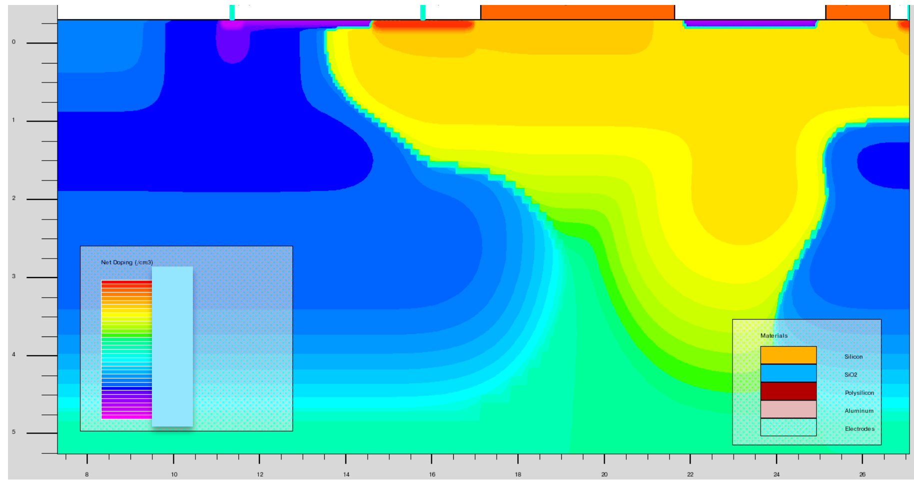


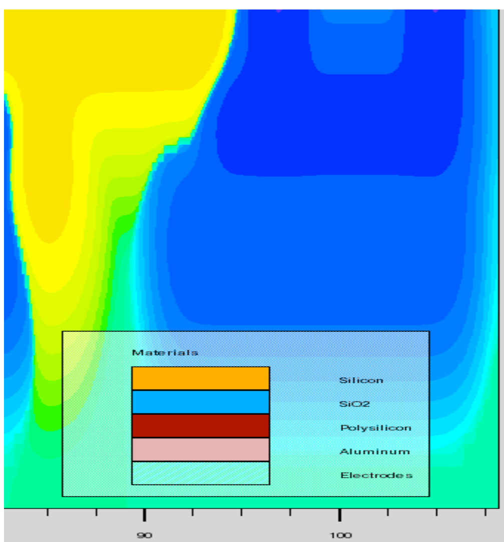


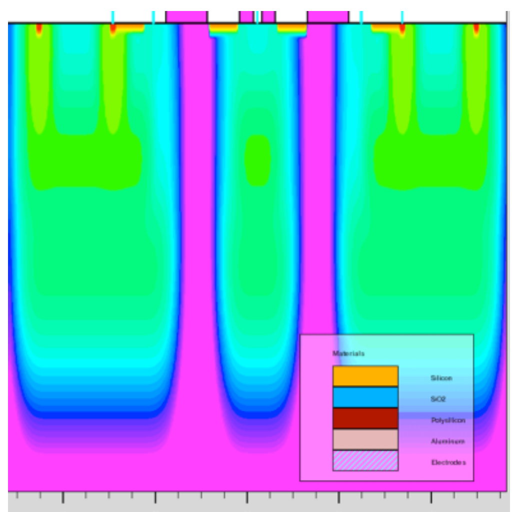


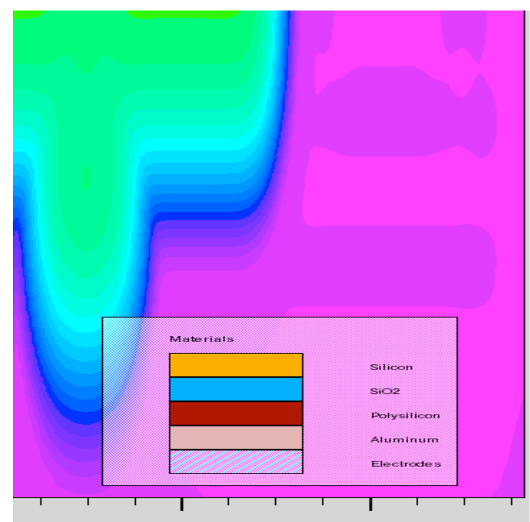
Sensor – pixel layout and TCAD simulations



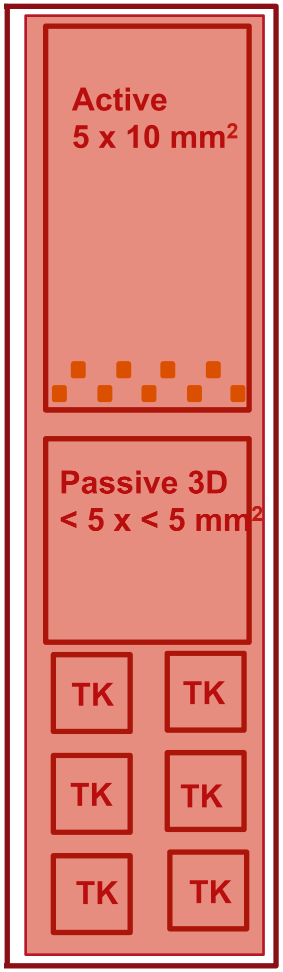








Floorplan for FLORA prototype sensor



Active: Sensor with analog readout circuitry

Passive: Suitable for 3D integration

TK: Test Keys with diodes connected in parallel for I/V characterization

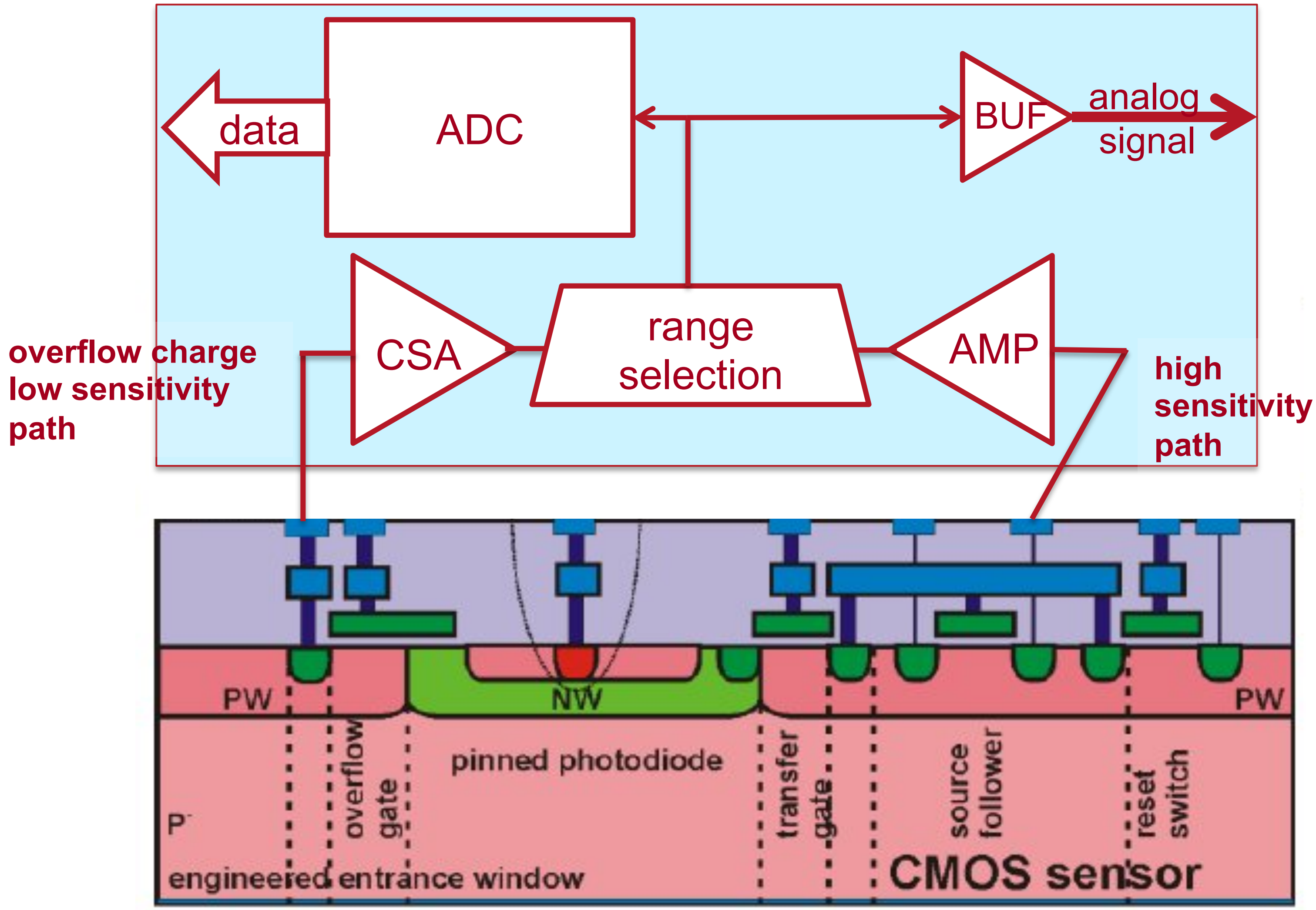
Working on packaging and electronics
Preparing in-vacuum test assembly

Other aspects – add slide on various techniques

- High quantum efficiency at low photon energies (250 eV)
  - Low temperature technology for the backside contact (entrance window).
    - Implant + rapid thermal annealing ~100 nm
    - Implant + laser annealing ~ 10's nm
    - MBE ~ 5 nm
    - Delta doping ~ 1nm
  - Molecular Beam Epitaxy (MBE) @ LBNL - P. Denes
  - Shallow implant with laser annealing (industrial 'standard')

- Radiation tolerance
  - a level of few rad/day in the worst operational conditions is expected.
    - Sensor thicker than 100 μm for 'self-shielding'
    - Rad hard design/technology

FLORA: high level pixel schematics



Requirement HIGH FRAME RATE

To address it we have chosen to:

- implement the **digitization locally** and ship the digital data off chip using proven **high speed serial links**.
- 1 ADC per pixel or 1 ADC per group of small number of pixels.
  - Parallel ADC operation would require only slow converters and the chance of being integrated at the pixel level.

A few architectures were investigated. Requirements:

- ultra low area
- ultra low power
- able to achieve 10 bit resolution

On-pixel ADC

SLAC

Analog to digital conversion architectures study

ADCs

Sigma-delta*: I used the preamp as part of the modulator (integrator). Used a switched current at the input of the preamp to perform the D/A. As is, it needs only a comparator and of course a digital filter. In the evaluation I used an ideal comparator but no decimator filter (DF). The DF appears to be challenging to implement, on a per pixel basis. Elegant but may be not the most promising. We may revisit.*

Counter/ramp based*: Easy to implement. Has been evaluated. Could be challenging because they require, in general, pow(2,n) steps to perform one conversion and the "ramp" needs to be n bit linear and not noisy.*

Successive approximation register (SAR) based*: These architectures appears to be the most promising. A conventional binary weighted capacitive SAR would not possible to implement in the available area. Instead a serial SAR ADC is proposed.*

Abderrazak Mekkaoui

All-MOS Charge Redistribution Analog-to-Digital Conversion Techniques—Part II

RICARDO E. SUÁREZ, MEMBER, IEEE, PAUL R. GRAY, MEMBER, IEEE, AND DAVID A. HODGES, SENIOR MEMBER, IEEE

Abstract—This two-part paper describes two different techniques for performing analog-to-digital (A/D) conversion compatibly with standard single-channel MOS technology. In the first paper, the use of a binary weighted capacitor array to perform a high-speed successive approximation conversion was discussed.

This second paper describes a two-capacitor successive approximation technique, which, in contrast to the first, requires considerably less die area, is inherently monotonic in the presence of capacitor ratio errors, and which operates at somewhat lower conversion rate. Factors affecting accuracy and conversion rate are considered analytically. Experimental results from a monolithic prototype are presented; a resolution of eight bits was achieved with an A/D conversion time of 100 μs. Used as a digital-to-analog (D/A) converter, a settling time of 13.5 μs was achieved. The estimated total die size for a completely monolithic version including logic is 5000 mil^2.

Manuscript received May 19, 1975; revised July 30, 1975. This research was sponsored in part by the National Science Foundation under Grant GK-40912.

R. E. Suárez was with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, Calif. He is now with the Instituto Venezolano de Investigaciones Cientificas (I.V.I.C.), Caracas, Venezuela.

P. R. Gray and D. A. Hodges are with the Department of Electrical Engineering and Computer Sciences and the Electronics Research Laboratory, University of California, Berkeley, Calif. 97420.

2-2 1975 papers that introduced serial charge re-distribution techniques.

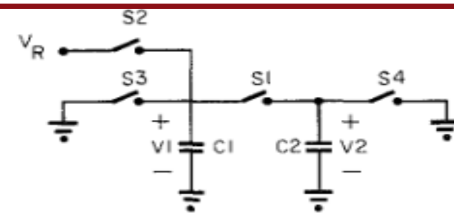


Fig. 1. Serial charge—redistribution digital-to-analog (D/A) converter.

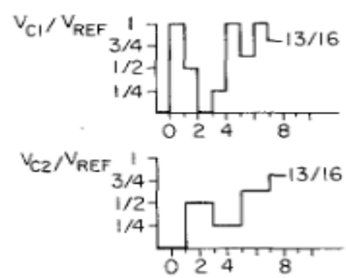


Fig. 2. Illustration of D/A conversion sequence for the input word 1101.

Converter high level schematics

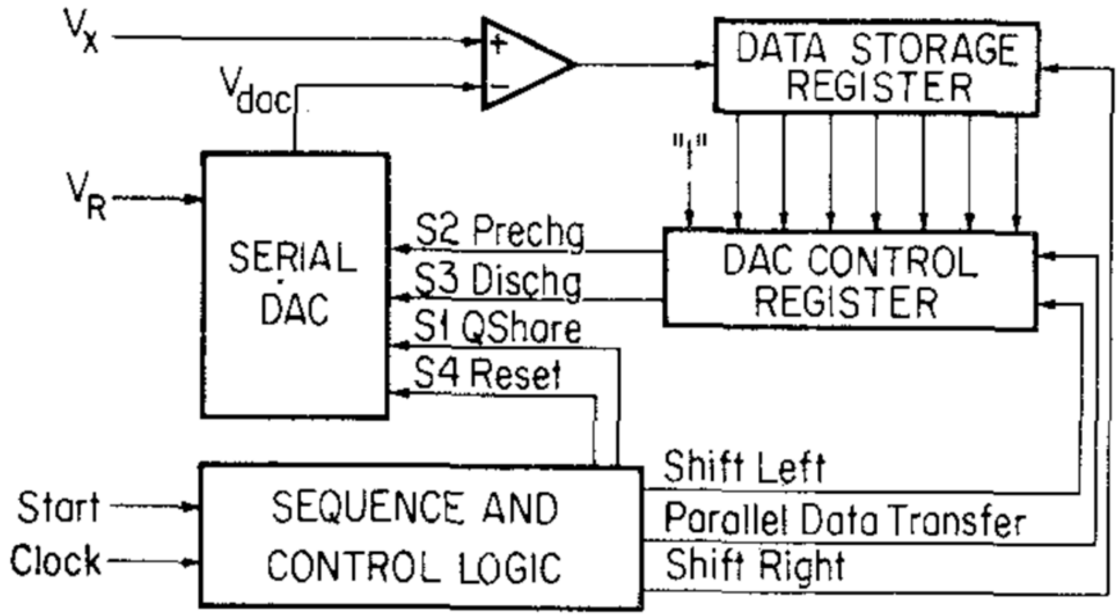


Fig. 3. Complete analog-to-digital (A/D) converter.

1975 – very compact ADC to be adapted to 2017 design

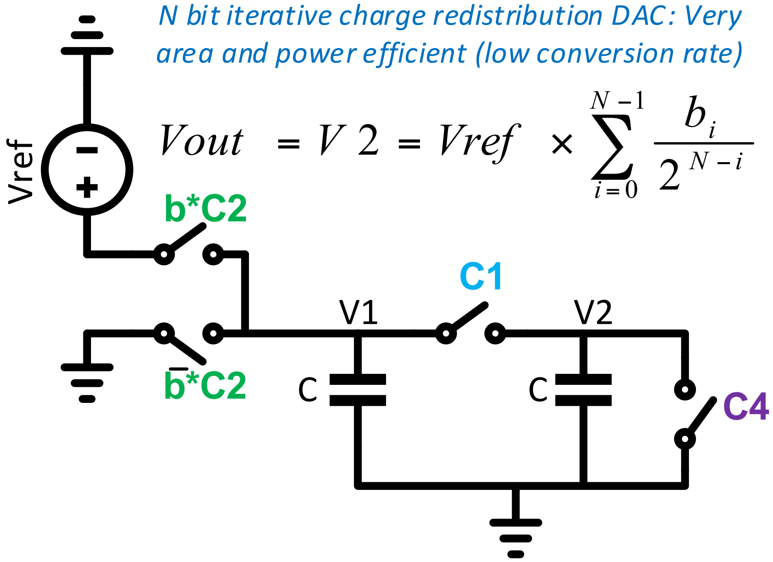
Serial charge re-distribution N bit DAC

- *A n-bit SAR ADC needs: n-bit DAC, n-bit-worthy comparator, and some rather simple logic.*
- *Serial charge re-distribution is very area and power efficient*
  - *Iteratively converts a digital word to an analog value by performing a iterative divide by two.*
  - *Bits are presented to the DAC serially one bit at a time (LSB first).*
  - *It takes N clock cycles to convert one N bit word.*
- *This technique trades speed for area and power.*
- *10 bits seem doable.*

Using such a DAC in a SAR ADC would require N(N+1) cycles with simple logic

N bit iterative charge redistribution DAC: Very area and power efficient (low conversion rate)

$$Vout = V2 = Vref \times \sum_{i=0}^{N-1} \frac{b_i}{2^{N-i}}$$



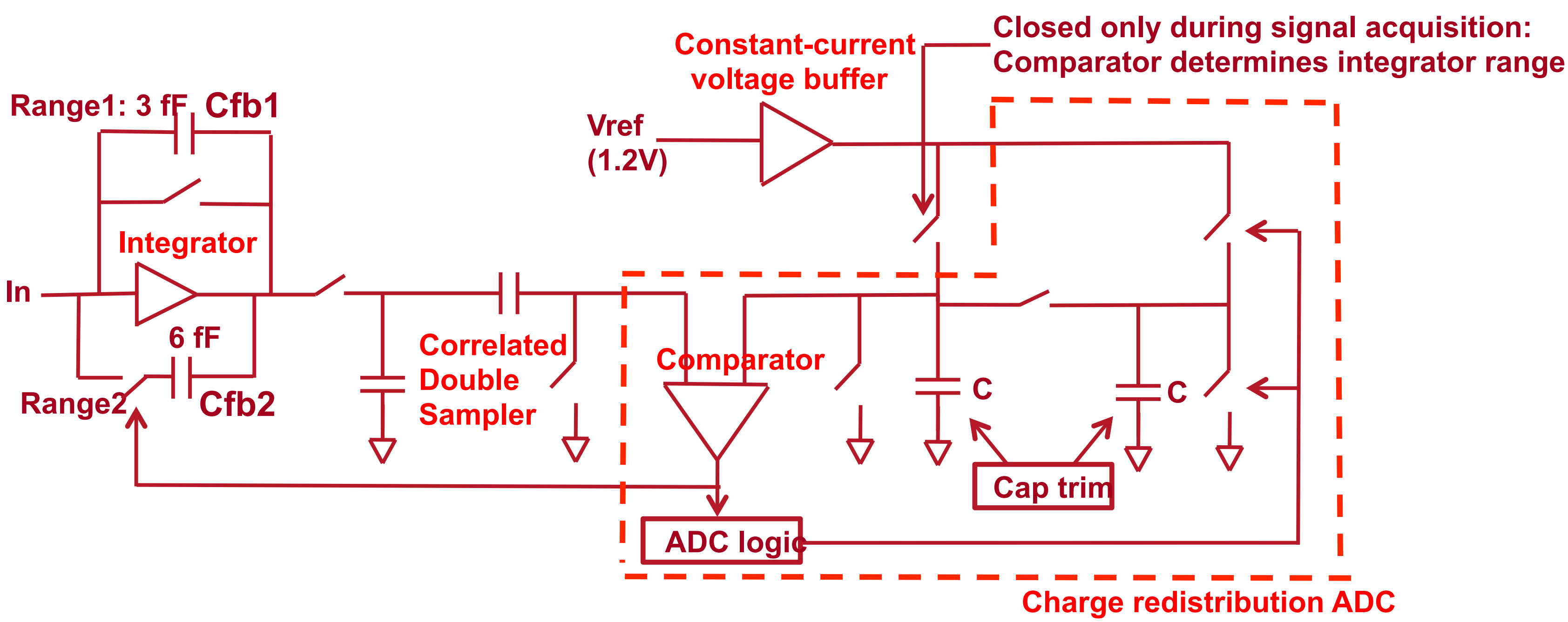
DAC uses capacitor arithmetic

The analog output is produced by connecting switches to charge or discharge the signal capacitor by flowing charge between signal and reference capacitor following a serial presentation of bits (b0, b1, b2….)

FLORA prototype: analog pixel design

The originally proposed idea is a 10-bit ADC in a 50 micron pixel:

- Integrator
- Correlated Double Sampler to store the signal. Acquire signal, *then* digitize it.
- Charge redistribution ADC, well-known technique uses minimal area



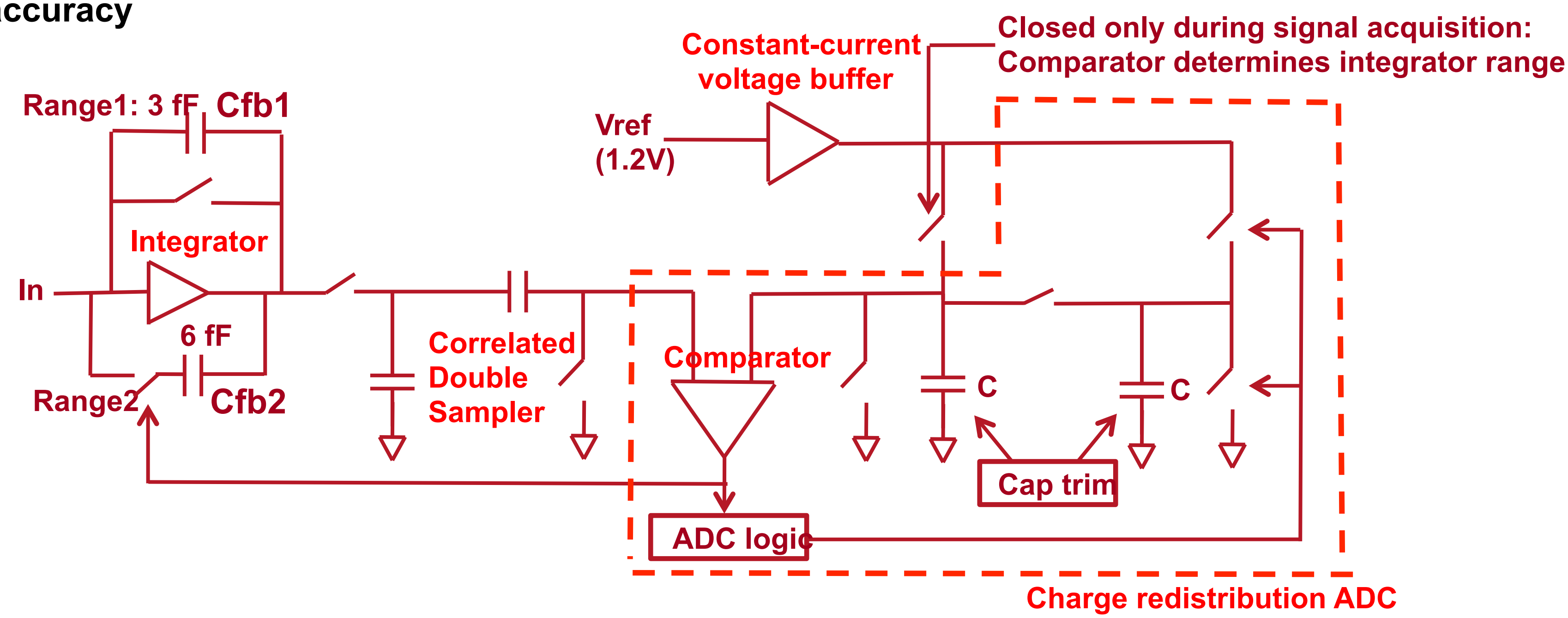
Analog pixel design is complete and simulated!

FLORA prototype: analog pixel design

SLAC

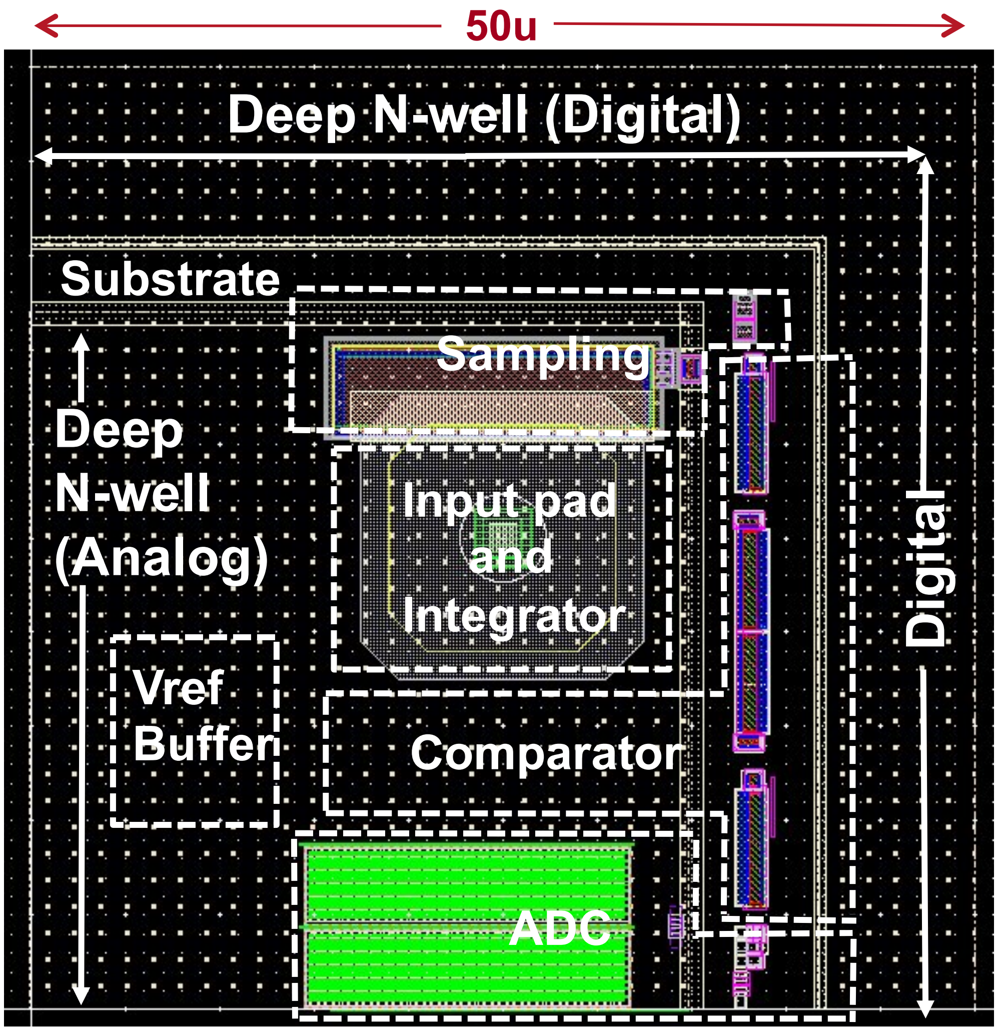
New ideas incorporated into the design:

- Multi-range integrator. Existing ADC comparator is used to switch to a 2nd integrator range for bigger signals. Range1 up to 22ke signal, allows ~10e noise at the low end. Range2 up to at least 70ke.
- ADC operation within 1.2V maximum. Allows all 1.2V logic (65 nm) – simpler, lower charge injection, accurate.
- Constant current ADC cap charging: avoids huge chip-wide dI/dt, cleaner operation
- New method for precision cap trimming allows smaller ADC caps while maintaining 10-bit accuracy

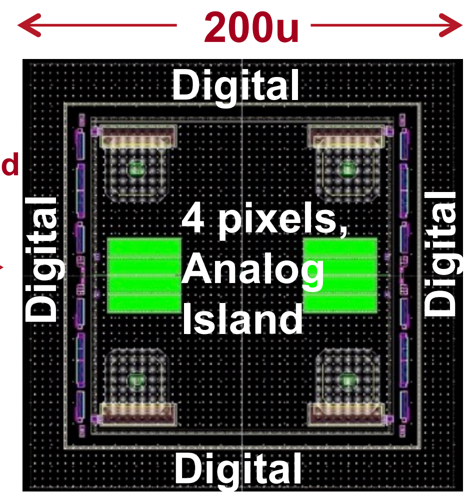


Analog pixel design is complete and simulated!

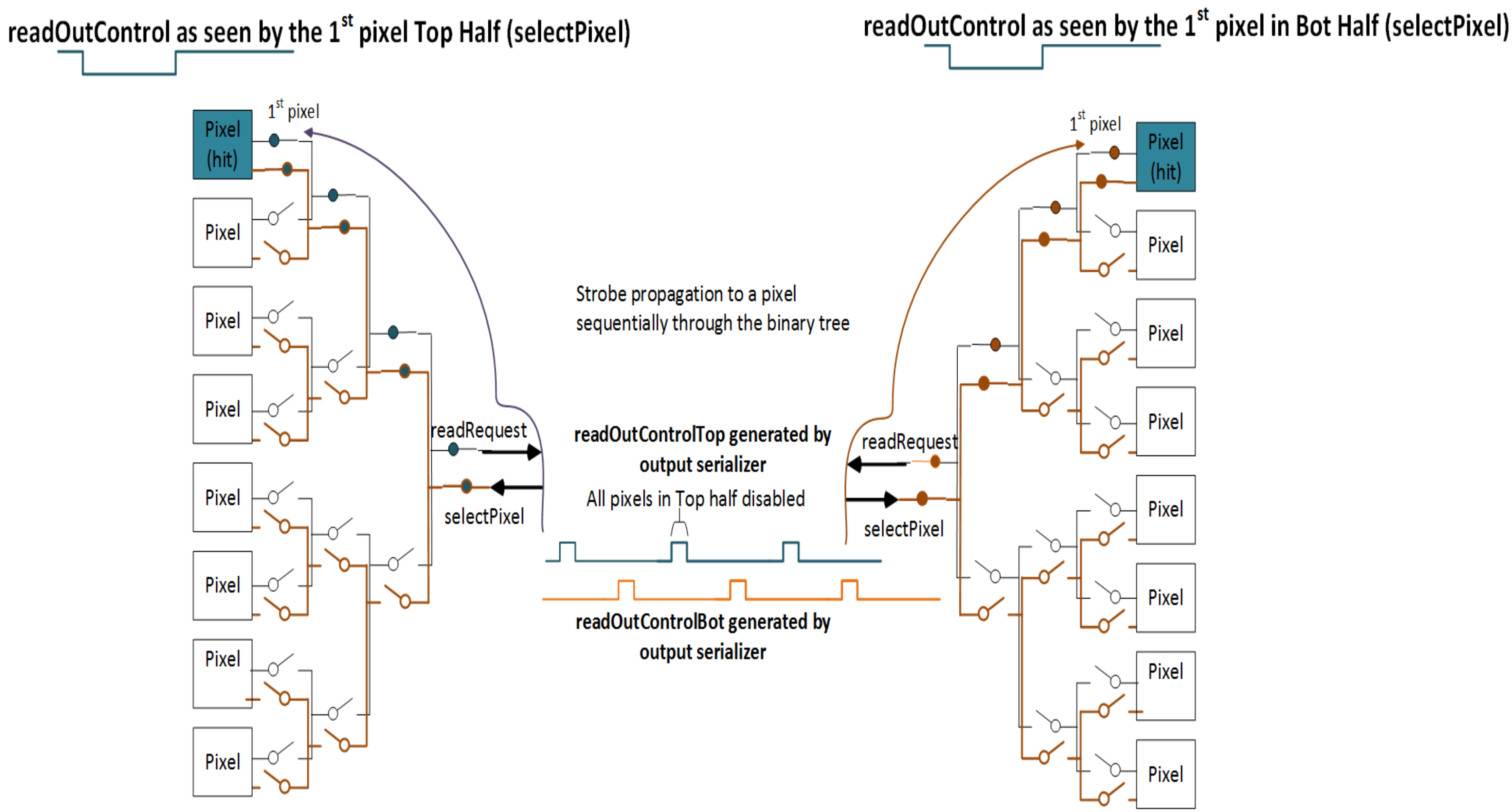
Pixel layout (in progress)



4 pixels, mirrored vertically and horizontally.



Strobeless Readout Concept



Traditional Readout vs. Strobeless Binary encoder

SLAC

Daisy chain of Shift Registers

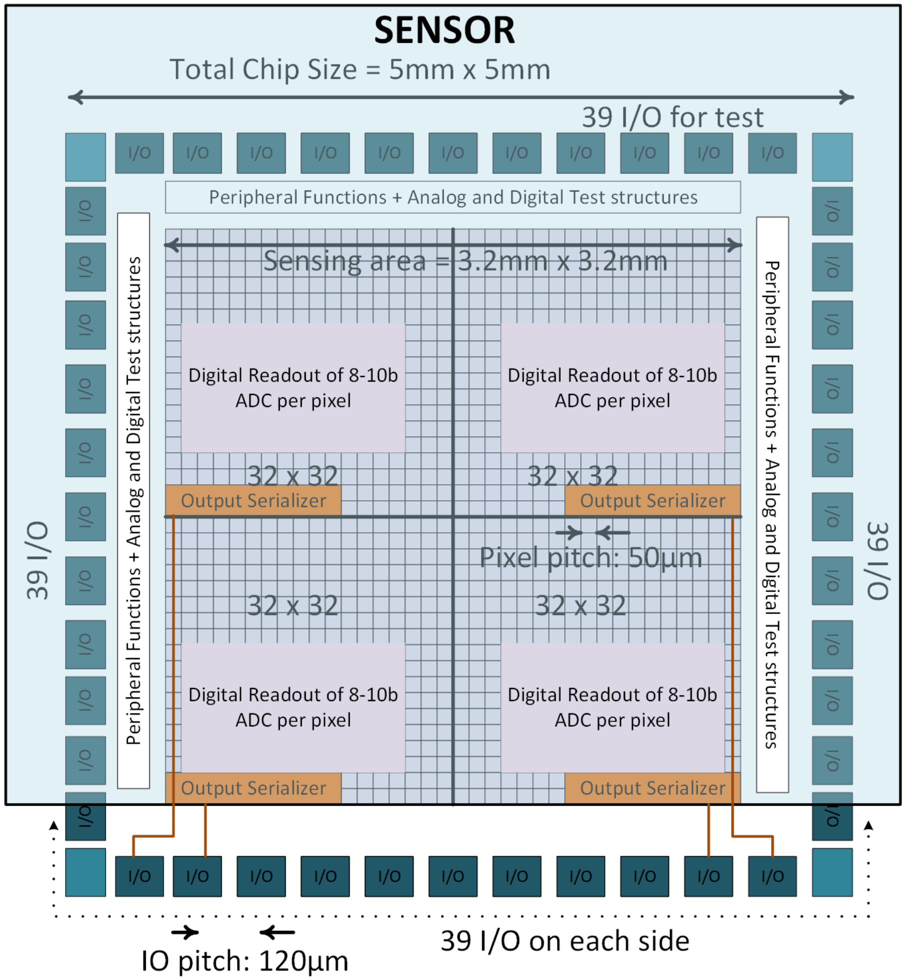
- Power consumption high (for 10bit per pixel for 1000 pixels using a 100MHz) = 16mW
- All pixels activated and hence huge glitches on power supply
- NO Deadtime
- DFF to store and shift data (larger area)

Strobeless Binary Encoder

- Power consumption low (for 10bit per pixel for 1000 pixels using a 400MHz output serializer clock) = 512μW
- Only 1 pixel is given access to the readout bus to transfer data
- NO deadtime, by creating a single stage pipeline and interleaving data from top and bottom halves.
- Latches to store data (smaller area)

Floor plan: module for prototype

- Allows for ASIC functionality tests with standard technology
- Simple sensor: pixel array detector in high resistivity silicon
- Commercial bump-bonding
- Standard chip I/O connection



Goal for this ADR phase (first year): test with x-rays

Key features of the detector module

SLAC

- 200eV – 2kev X-Ray photons (1-1000 photons)
  - Dynamic range: [70e-:700ke-]
- High dynamic range: 2 signal paths
  - Low noise (<15e-) MAPS (on the sensor) - output connected to ADC in pixel
  - Low gain via ASIC preamplifier
- ASIC has two static gain ranges (to reduce gain in the frontend x10) pre-selected per chip
- ASIC has two dynamic gain ranges (adaptive gain): 1bit range select information
- Small pixels: 50µm pitch

Key features of the detector module

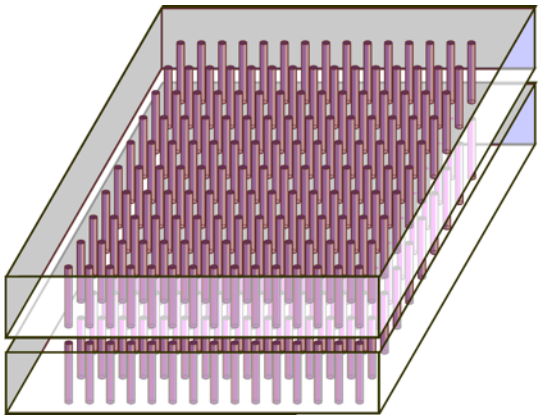
- 10bit In-pixel ADC
  - ADC: serial SAR (DAC with only 2 capacitors) with conversion time ~ 60μs to allow > 10kHz readout rate

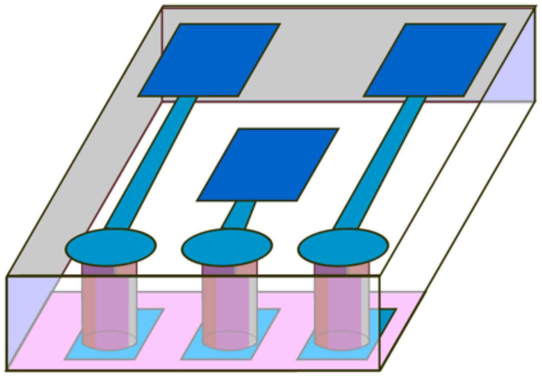
- No deadtime: Simultaneous ADC conversion and readout by loading data in latches

- Strobeless Binary tree, low noise and low power readout architecture per 1024 pixels

- Prototype ASIC: 5mm x 5mm: Active area: 3.2mm x 3.2mm, 64x64 pixels, divided into 4 easily scalable quadrants. Chip outputs on single edge at allow larger sensors to be bonded to the ASIC. Pitch of I/O pads is 120μm

Full prototype will leverage advanced interconnects



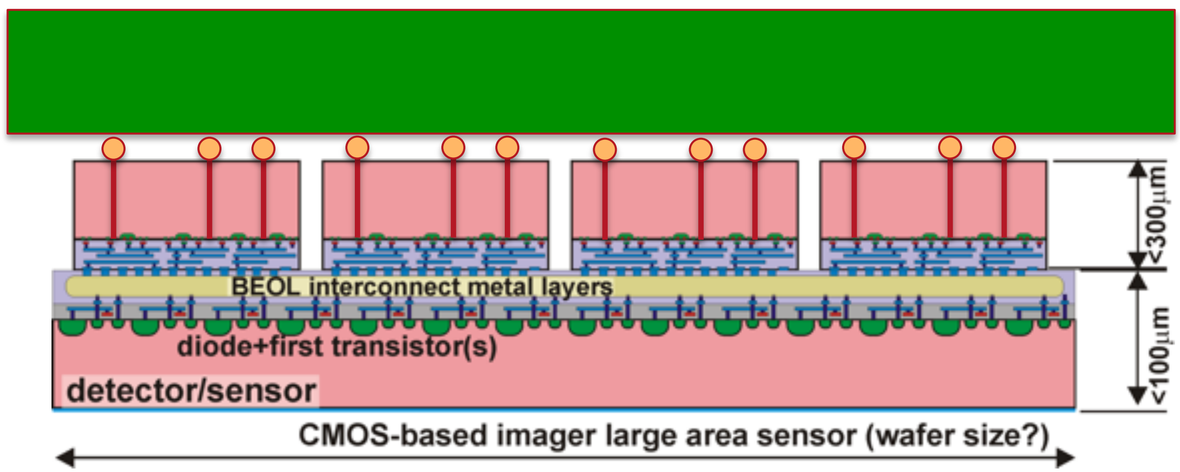


Almost 3D-IC

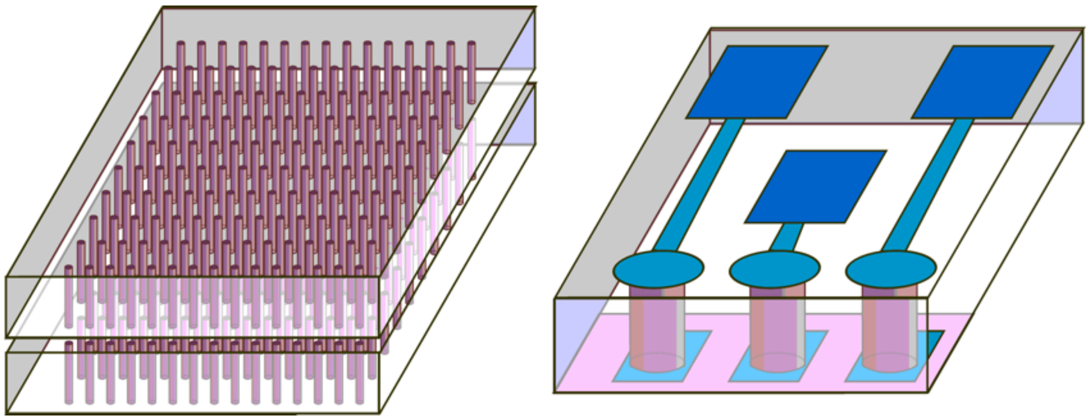
- Large diameter (~50 μm), deep (~100 μm) and coarse pitch or peripherally located Through Silicon Vias
- ASICs are single layer, and TSVs are used to carry I/Os from one side to another (few, high C)

3D IC

- Small diameter (~1 μm), shallow (<~10 μm) and highly dense pitch (~2 μm) Through Silicon Vias
- ASICs composed of multiple tiers that exchange signals through inter-tier bonding interfaces (dense and low C)



Full prototype will leverage advanced interconnects

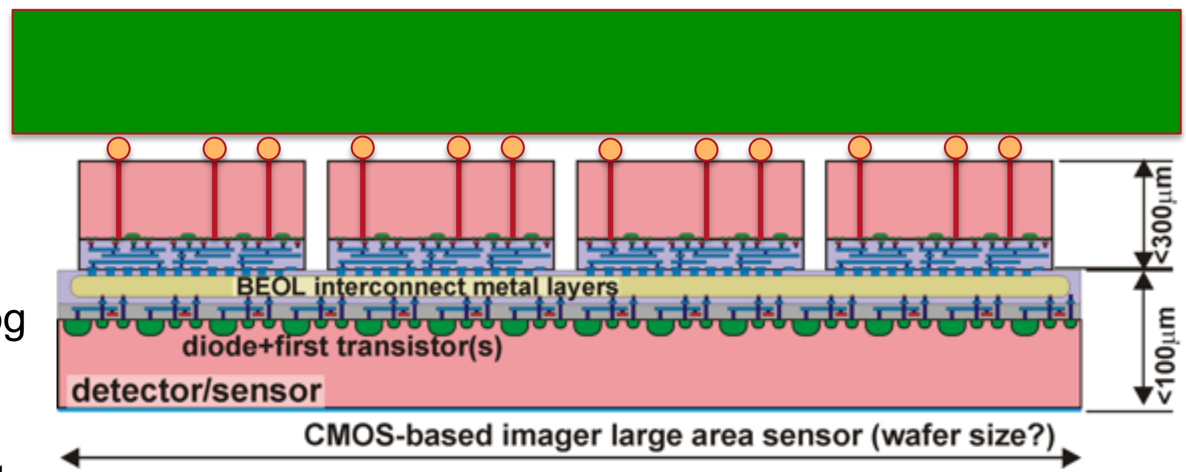


Almost 3D-IC

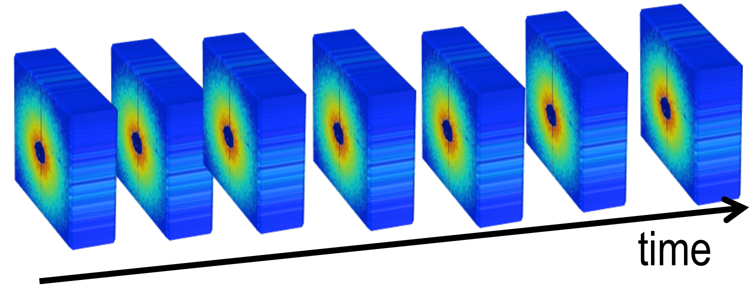
- Improved forms of pixel detectors with reduced dead zones
- Avoided wire-bonding and rigid form of pixilated layout
  - processing analog/digital ASIC with I/O control and other functions located on periphery/balcony
- Conservative technology > moderate costs

3D IC

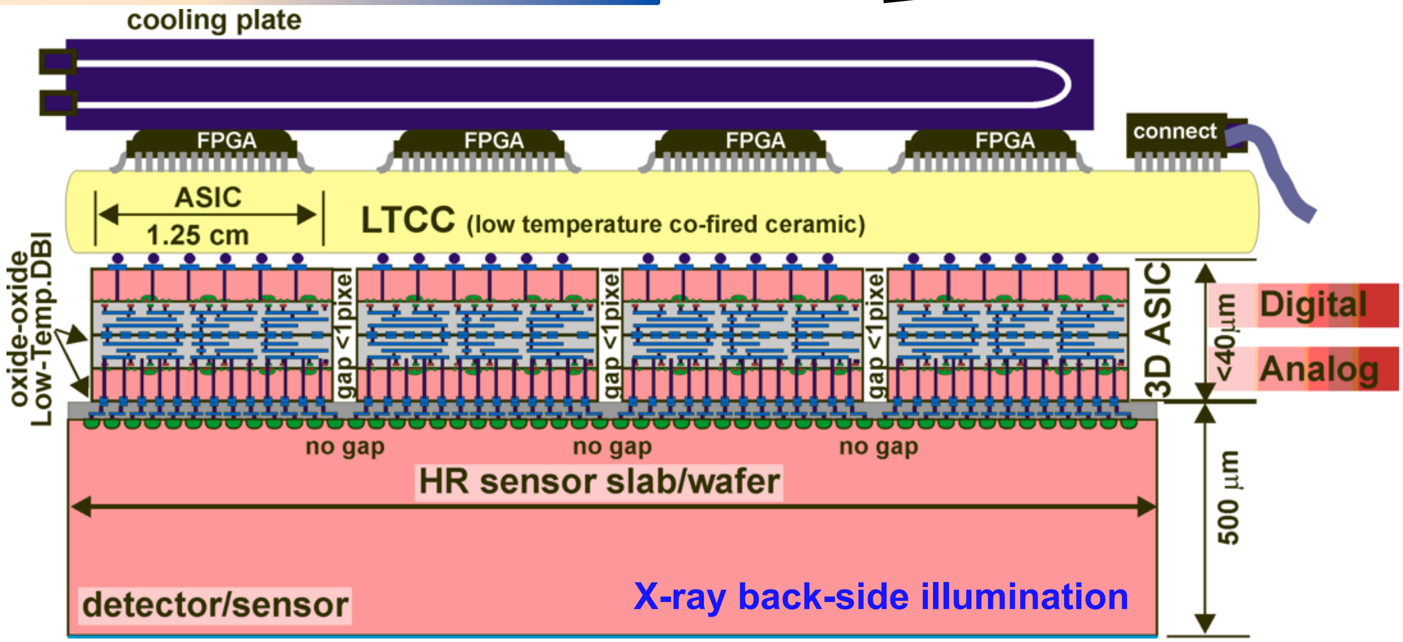
- Unprecedented forms of pixel detectors are possible, i.e. seamlessly assembled on large area pixel sensor (or entirely edgeless, i.e. 4-side buttable)
- Separate functions of tiers: analog (pixilated) and digital (distributed circuits) tiers
- New technology > increased costs



Currently underway: VIPIC-L camera



Single module X-ray camera for XCS



- **Features:**
  - 1Mpixel = 7×7 VIPIC-L directly bonded to a sensor wafer
  - 1FPGA per VIPIC-L for on the fly data processing (up to 3.5 Tbps of raw data produced)
  - Multi-layer (>20 routing layer LTCC) suports b-bonded detector structure
  - Flat back-side friendly to mounting of cooling plate
  - Challening under any aspect: 3D integration, assembly, DAQ, processing

BNL, Fermilab, APS

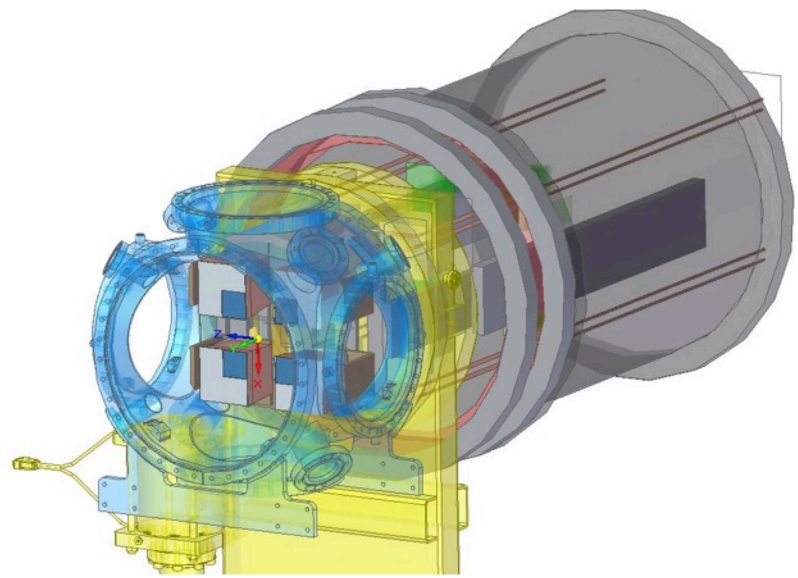
Something about the system

FLORA is foreseen as the upgrade of the forward scattering area detector for soft x-rays at LCLS-II

As such will have to:
- fit in the same experimental chamber
- re-use as much of the existing infrastructure as possible

Power considerations:
- we expect a power consumption similar to VIPIC
  - similar solutions for cooling can be adopted

- 1 Mpixel standalone quad at 10 kHz
- 4 Mpix per plane (4 x 100 Gbit/s)
- 4 x 40 GbE per quad
- Power: 38 W per quad
- Run at 10^{o}C (designed for -10^{o}C for engineering margin)
- Glycol cooling envisioned



Courtesy of Rebecca Armenta

Thanks

Questions?