

A Novel Experiment Searching for the Lepton Flavor Violating Decay



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On Behalf of the Mu3e Proto-Collaboration

July 17th 2012



Overview

- Physics Motivation
- Mu3e Experiment
- HV-MAPS
- Construction
- Timing detectors
- DAQ
- Summary





Physics Motivation

Lepton flavor violation?

Standard model:

- No lepton flavor violation

Three Generations of Matter (Fermions)

	I	II	III	
mass →	2.4 MeV/c ²	1.27 GeV/c ²	171.2 GeV/c ²	0
charge →	2/3	2/3	2/3	0
spin →	1/2	1/2	1/2	1
name →	u up	c charm	t top	γ photon
	4.8 MeV/c ²	104 MeV/c ²	4.2 GeV/c ²	0
	-1/3	-1/3	-1/3	0
	1/2	1/2	1/2	1
Quarks	d down	s strange	b bottom	g gluon
	<2.2 eV/c ²	<0.17 MeV/c ²	<15.5 MeV/c ²	91.2 GeV/c ²
	0	0	0	0
	1/2	1/2	1/2	1
	ν_e electron neutrino	ν_μ muon neutrino	ν_τ tau neutrino	Z⁰ Z boson
	0.511 MeV/c ²	105.7 MeV/c ²	1.777 GeV/c ²	80.4 GeV/c ²
	-1	-1	-1	±1
	1/2	1/2	1/2	1
Leptons	e electron	μ muon	τ tau	W[±] W boson

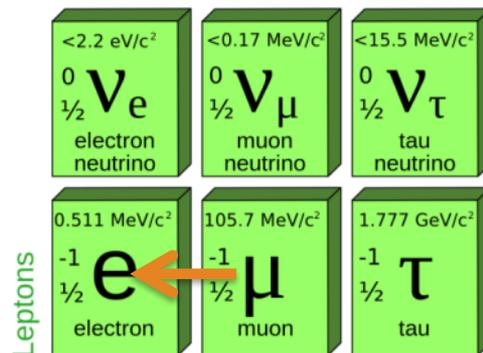
Gauge Bosons

Physics Motivation

Lepton flavor violation?

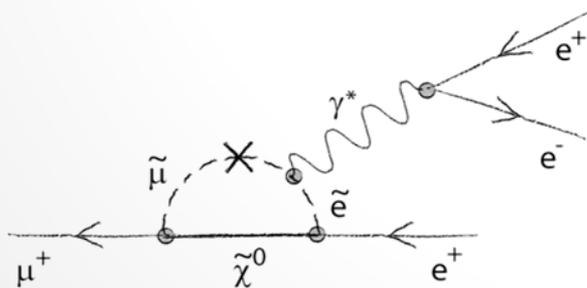
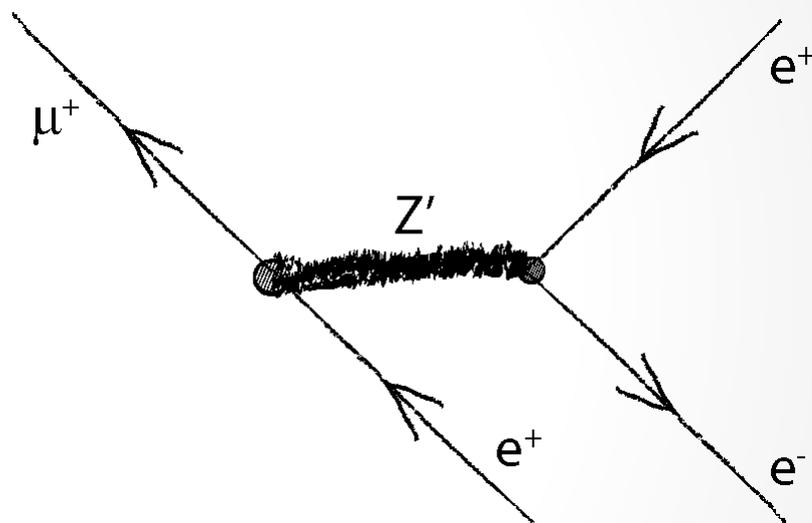
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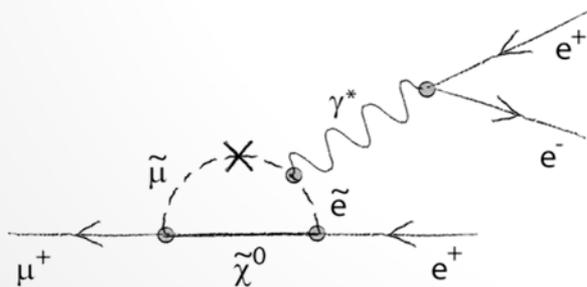
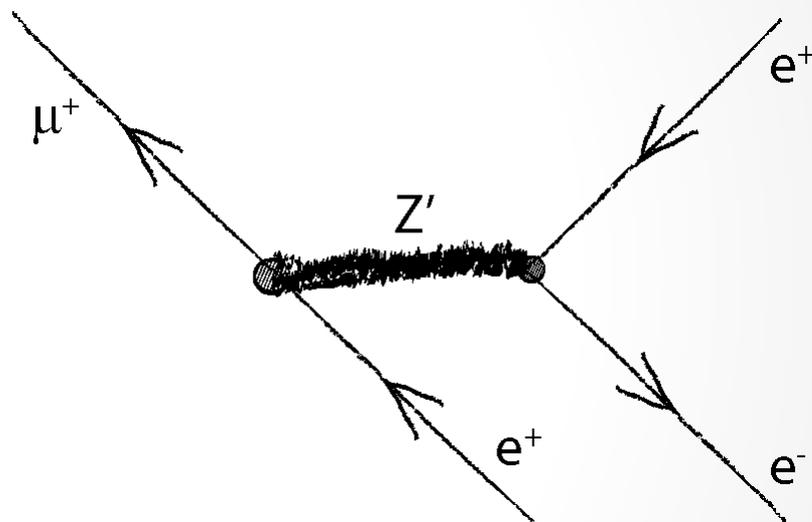
The Mu3e Signal

- $\mu \rightarrow eee$ rare in SM
- Enhanced in:
 - Super-symmetry
 - Grand unified models
 - Left-right symmetric models
 - Extended Higgs sector
 - Large extra dimensions



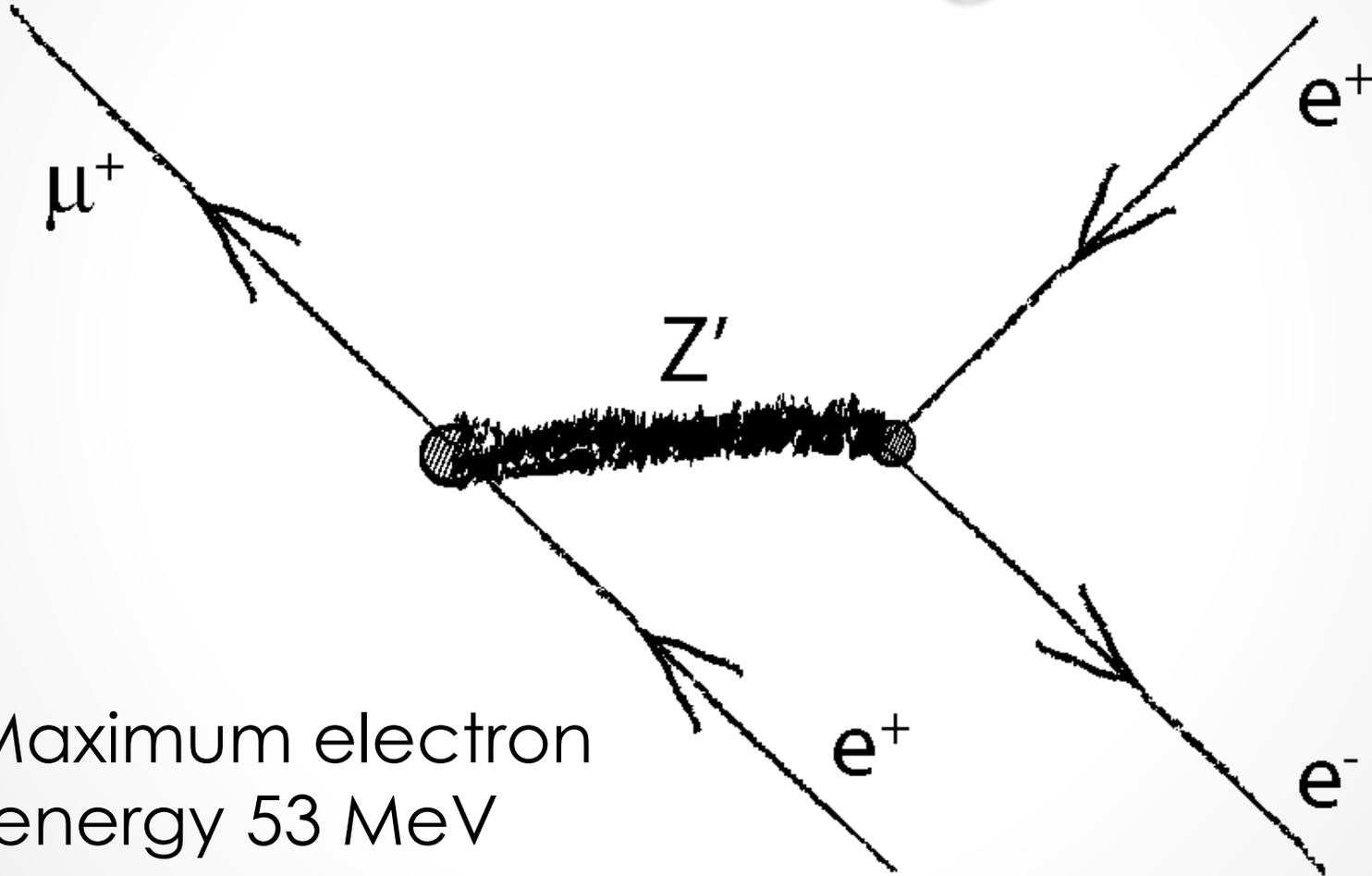
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- Rare decay (BR 10^{-12}, SINDRUM)
- For BR $O(10^{-16})$
 - $>10^{16}$ muon decays
 - High decay rates $O(10^9)$ muon/s

The Mu3e Signal



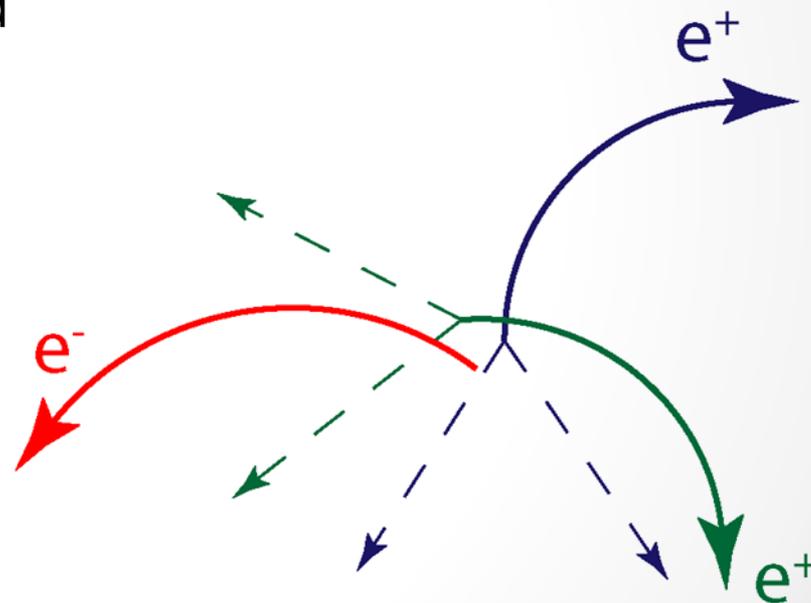
→ Maximum electron energy 53 MeV



The Mu3e Background

- Combinatorial background
 - $\mu^+ \rightarrow e^+ \nu \nu$ & $\mu^+ \rightarrow e^+ \nu \nu$ & $e^+ e^-$
 - many possible combinations

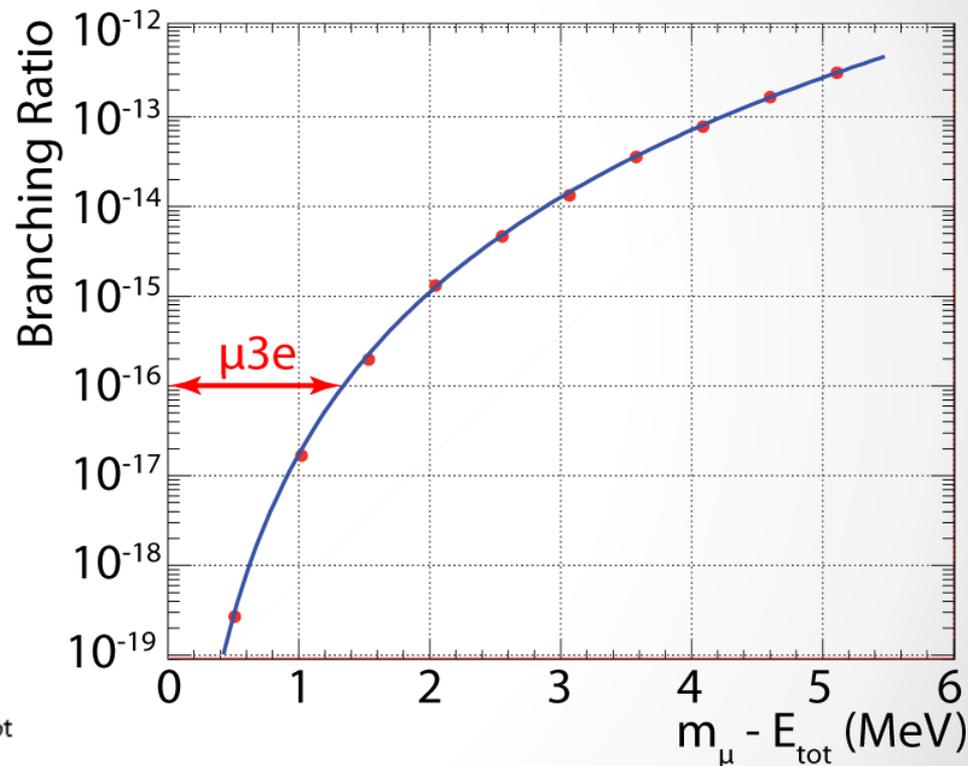
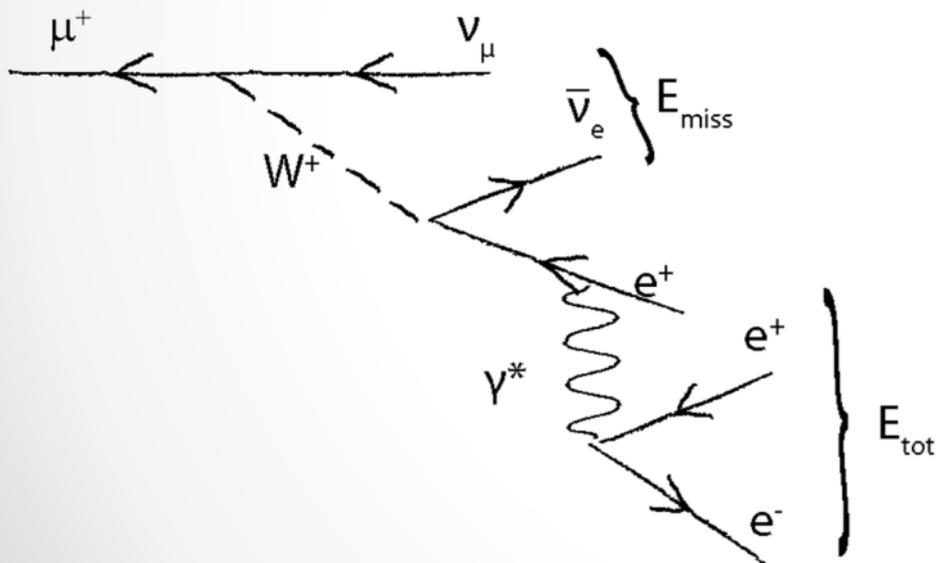
- Good time and
- Good vertex resolution required





The Mu3e Background

- $\mu^+ \rightarrow e^+ e^- e^+ \nu \nu$
 - Missing energy (ν)
 - Good momentum resolution



(R. M. Djilkibaev, R. V. Konoplich,
Phys.Rev. D79 (2009) 073004)



Challenges

...



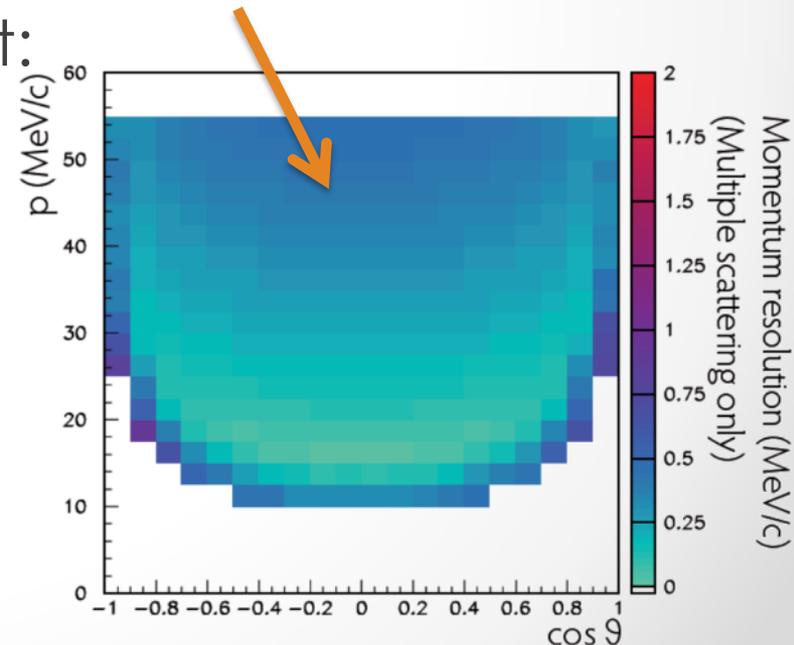
Challenges

- High rates
- Good timing resolution
- Good vertex resolution
- Excellent momentum resolution
- Extremely low material budget



Challenges

- High rates: $10^9 \mu/s$
- Good timing resolution: 100 ps
- Good vertex resolution: $\sim 100 \mu m$
- Excellent momentum resolution: $\sim 0.5 \text{ MeV}/c^2$
- Extremely low material budget:
 - $1 \times 10^{-3} X_0$ (Si-Tracker Layer)
- HV-MAPS spectrometer
 - 50 μm thin sensors
 - B ~ 1 T field
- + Timing detectors





The Mu3e Experiment

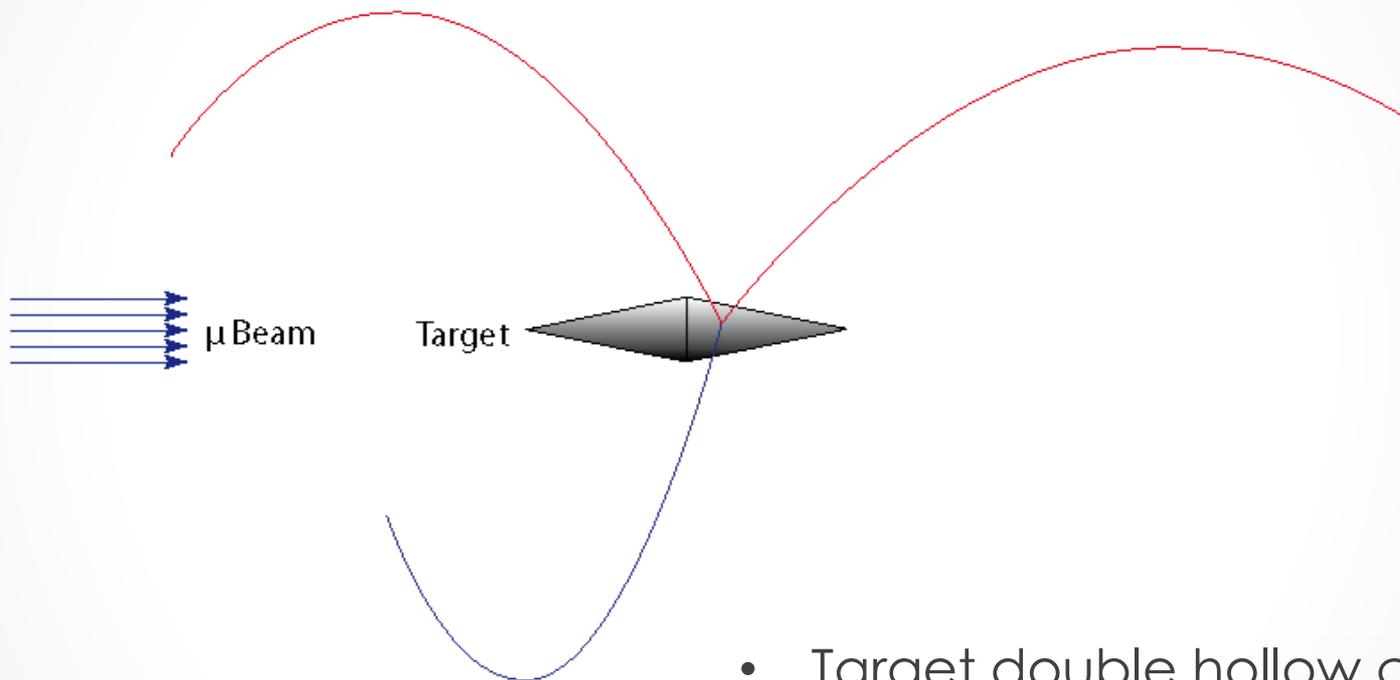


- Muon beam $O(10^9/s)$
- Helium atmosphere
- 1 T B-field

- Target double hollow cone
- Silicon pixel tracker
- Scintillating fiber tracker
- Tile hodoscope



The Mu3e Experiment

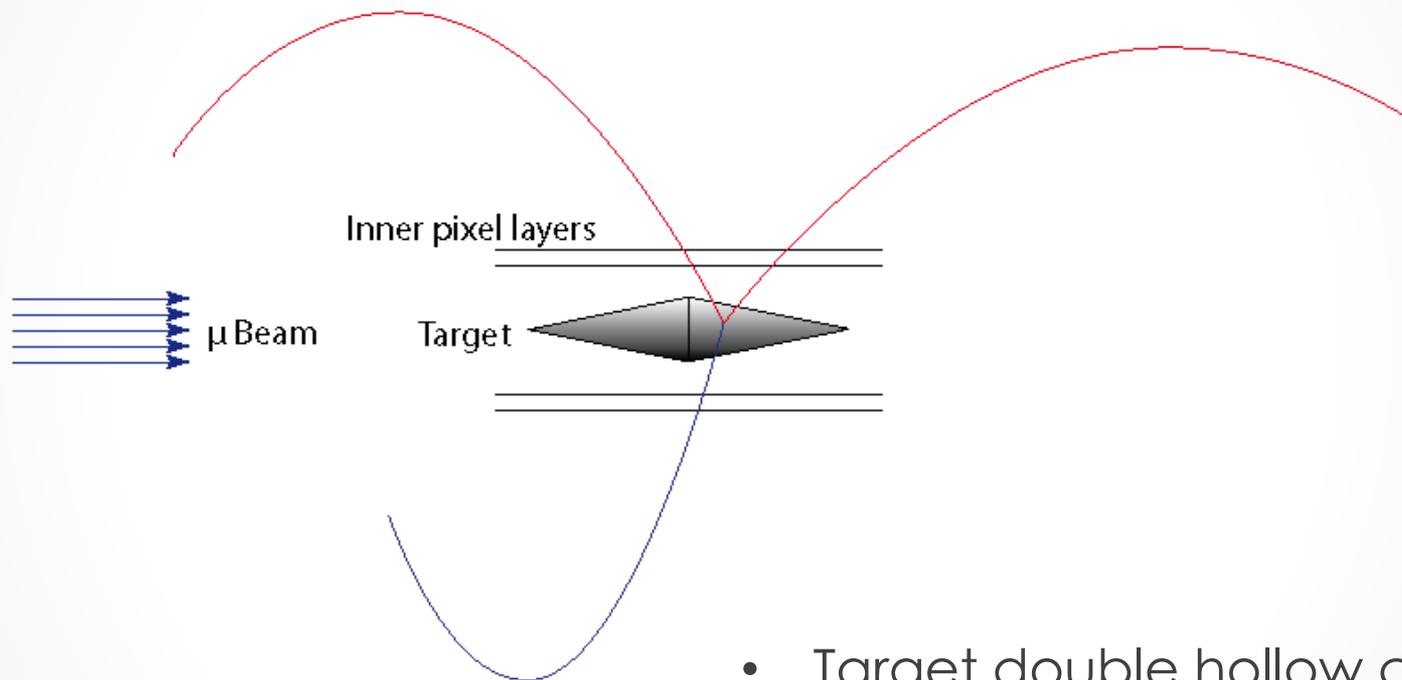


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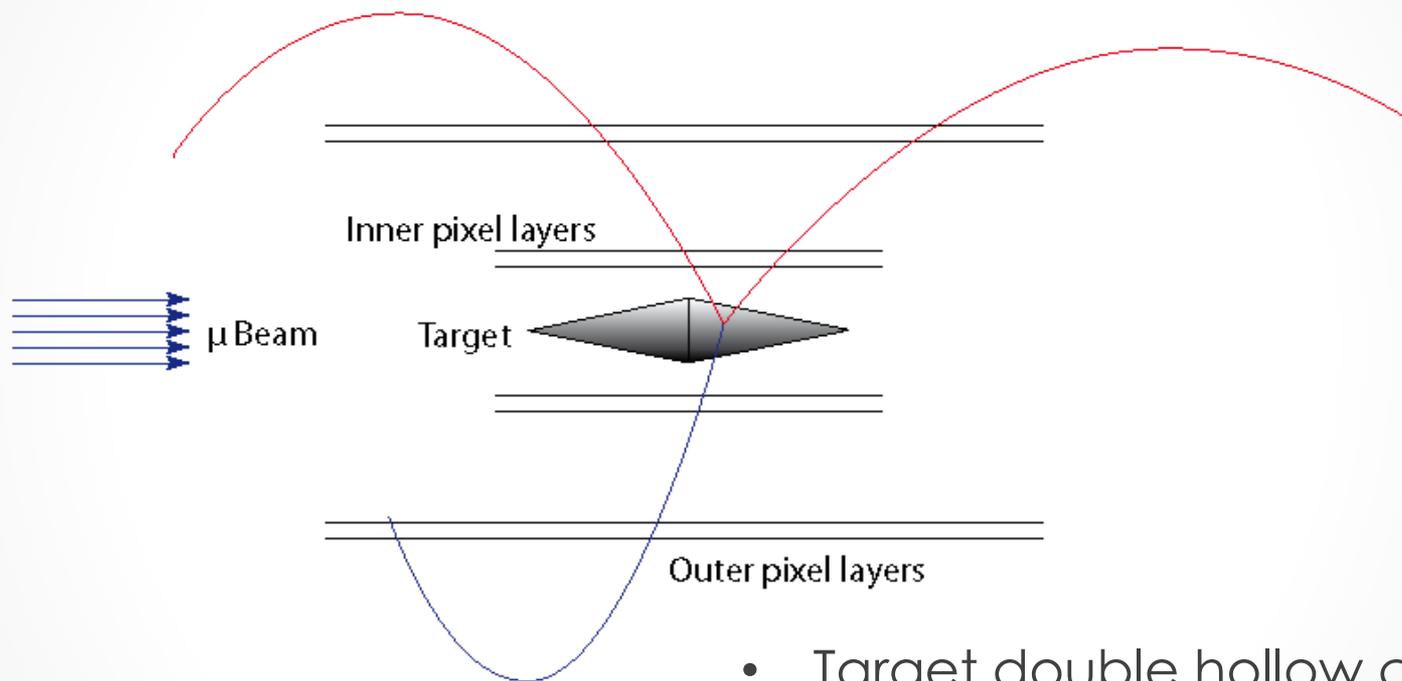


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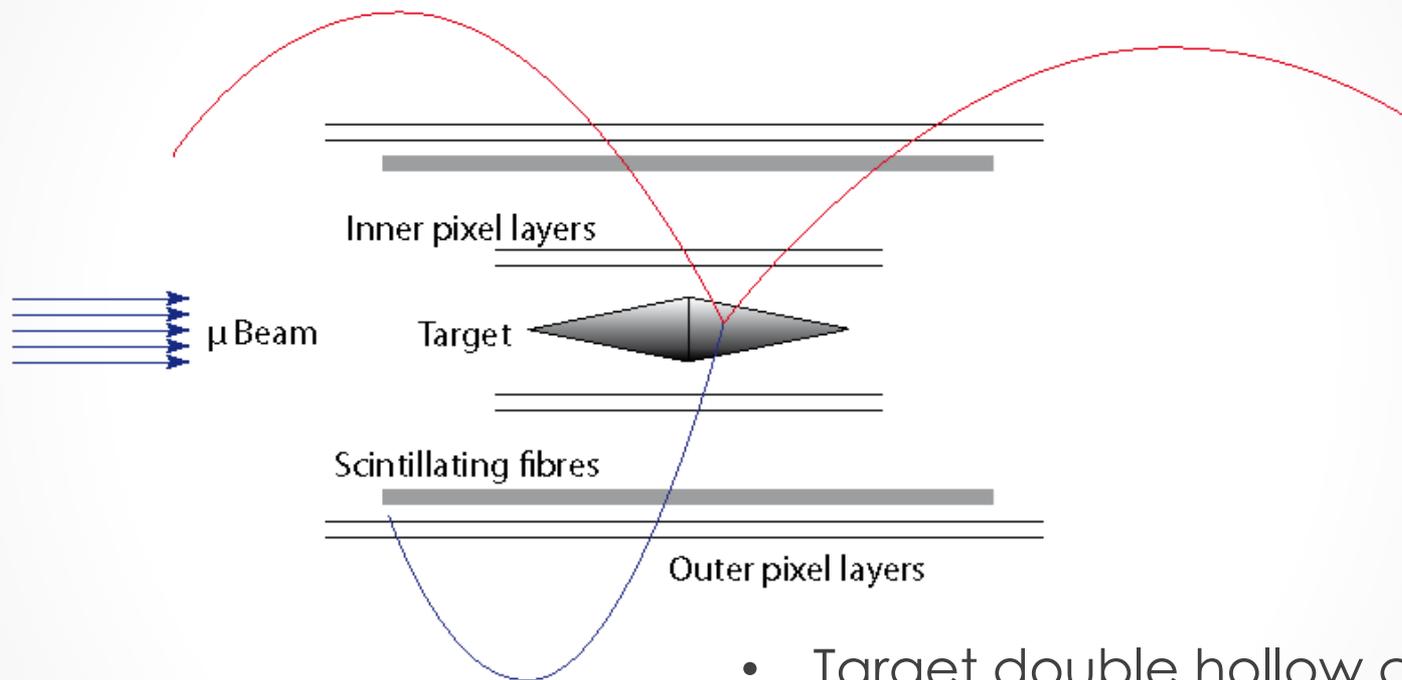


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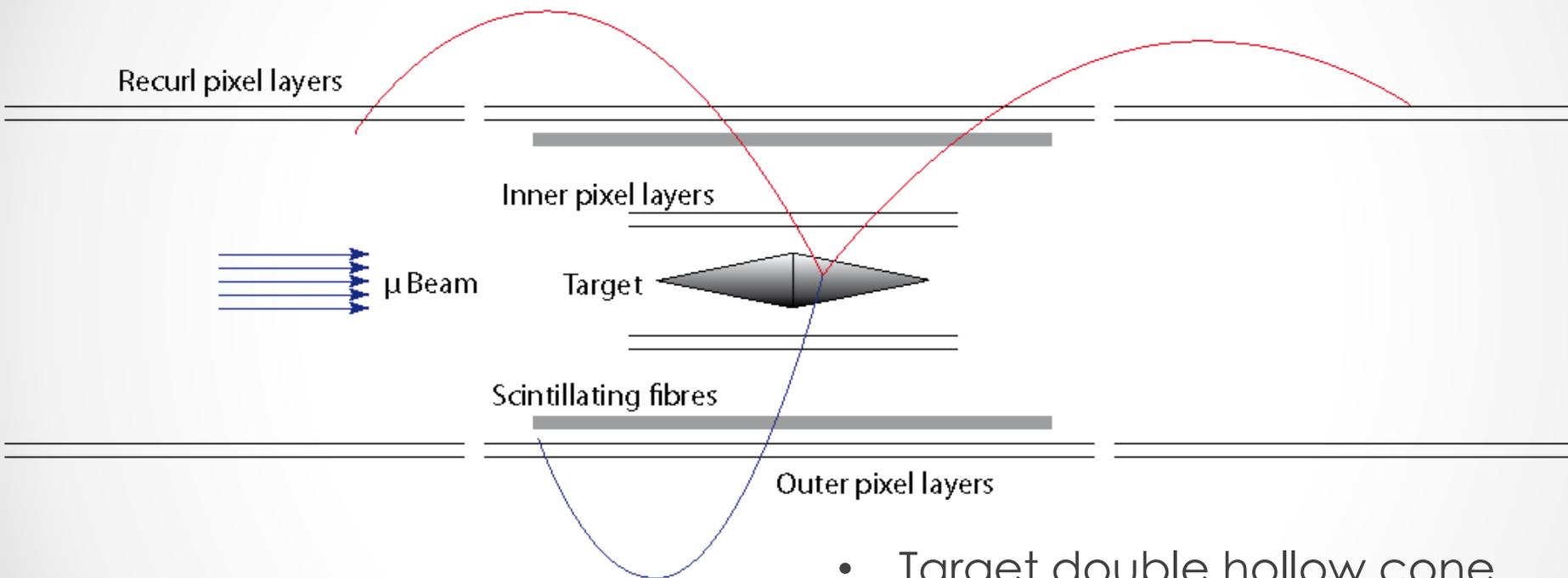


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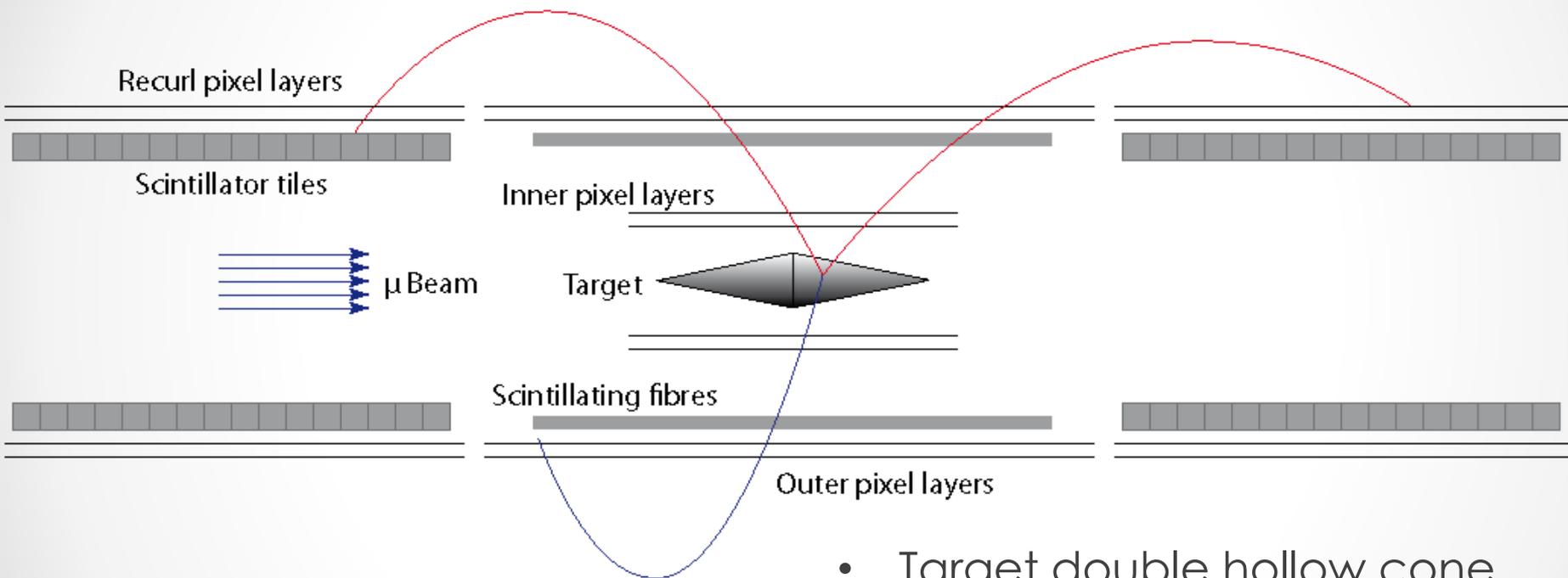


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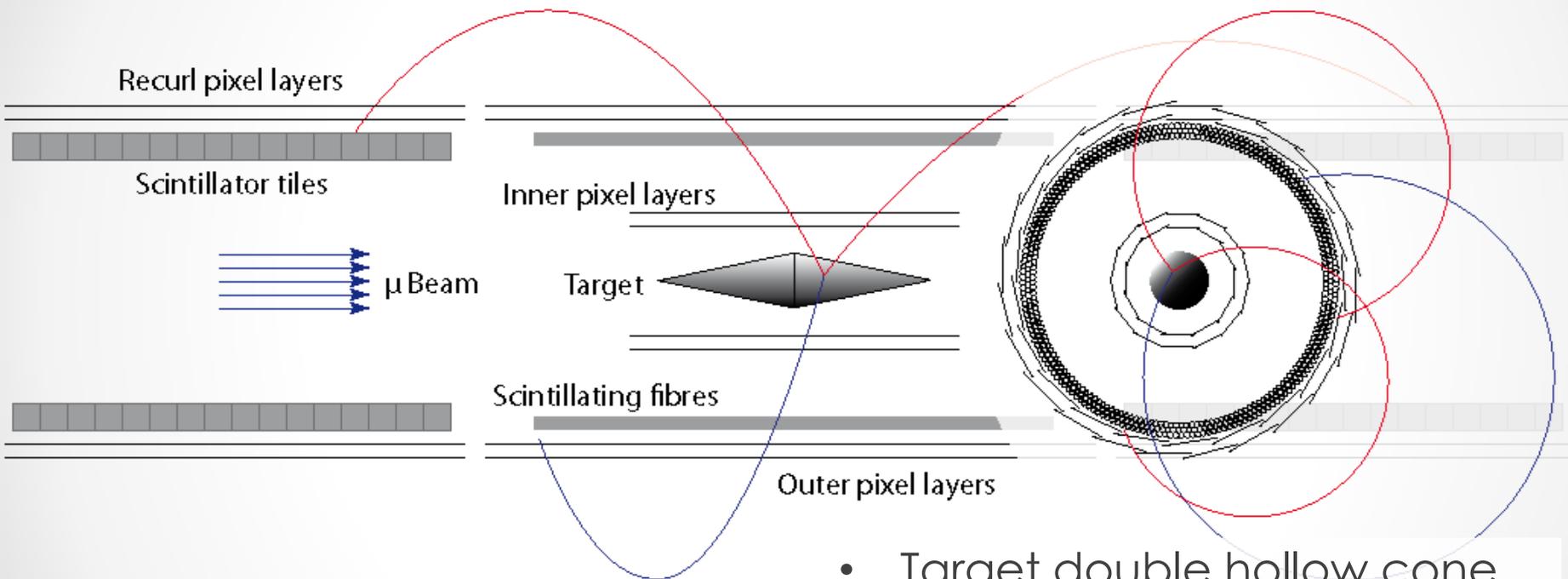


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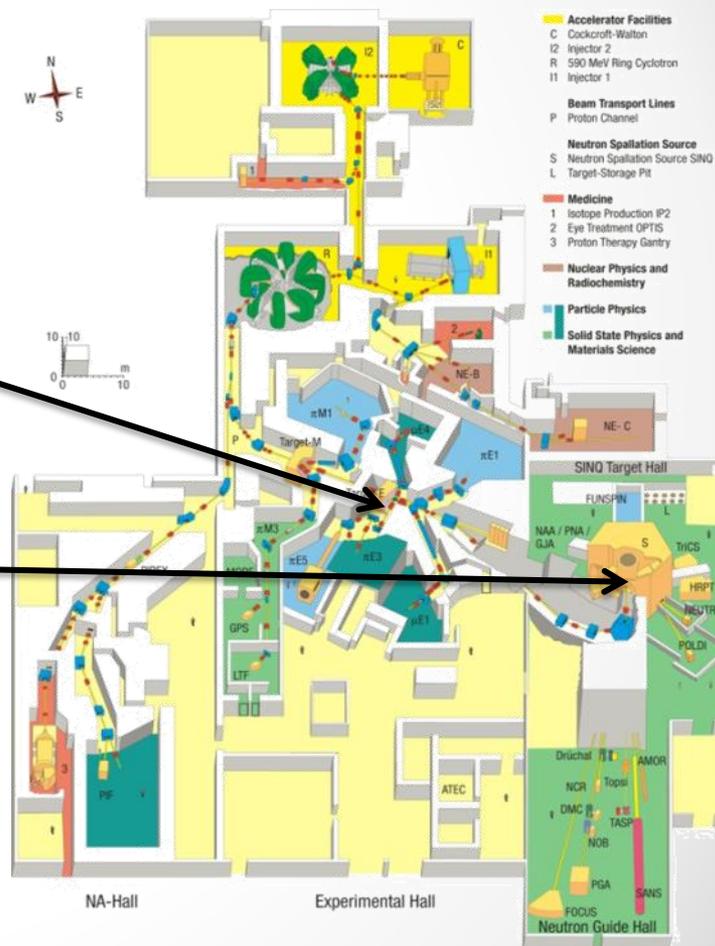
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PSI μ -Beam

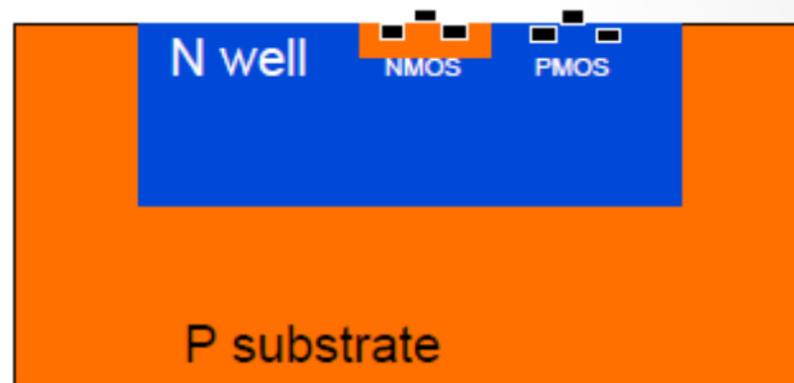
Paul Scherrer Institute Switzerland:

- 2.2 mA of 590 MeV/c protons
- Phase I:
 - Surface muons from target E
 - Up to a few $10^8 \mu/s$
- Phase II:
 - New beam line at the neutron source
 - Several $10^9 \mu/s$ possible
 - $>10^{16}$ muon decays per year
 - BR 10^{-16} (90% CL)



HV-MAPS

- **H**igh **V**oltage **M**onolithic **A**ctive **P**ixel **S**ensors
- Pixel sensors
- HV-CMOS technology
- N-well in p-substrate
- Reverse biased

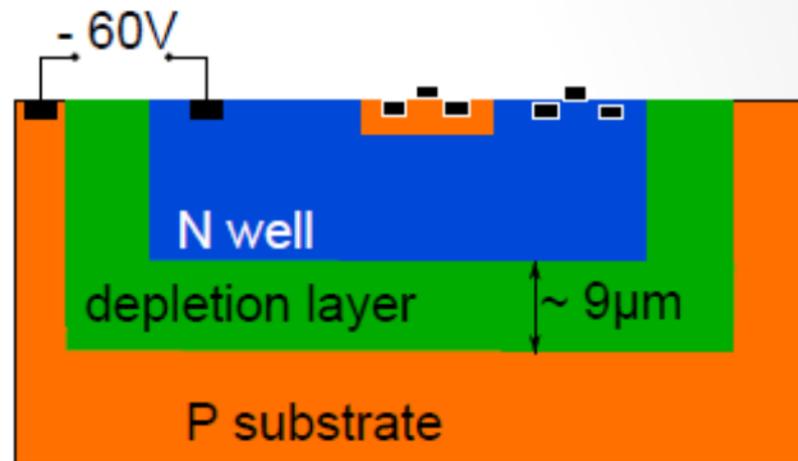


by Ivan Peric

I. Peric, A novel monolithic pixelated particle detector implemented in high-voltage CMOS technology
Nucl.Instrum.Meth., 2007, A582, 876

HV-MAPS

- **H**igh **V**oltage **M**onolithic **A**ctive **P**ixel **S**ensors
- Pixel sensors
- HV-CMOS technology
- N-well in p-substrate
- Reversely biased $\sim 60\text{V}$
 - Depletion layer
 - Charge collection via drift
 - Fast $O(100\text{ ns})$ charge collection
 - Thinning to $< 50\ \mu\text{m}$ possible

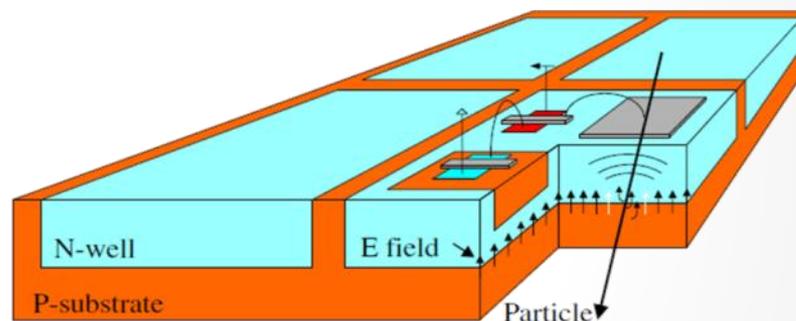


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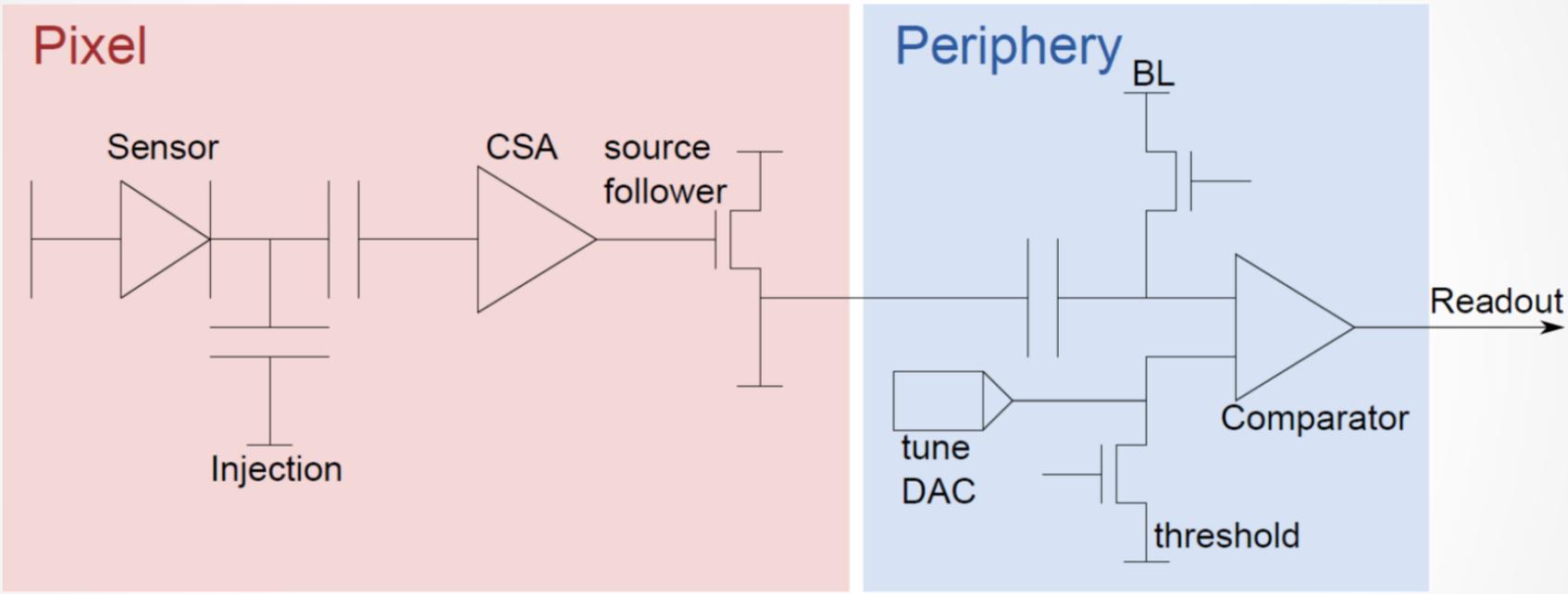
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- Integrated readout electronics



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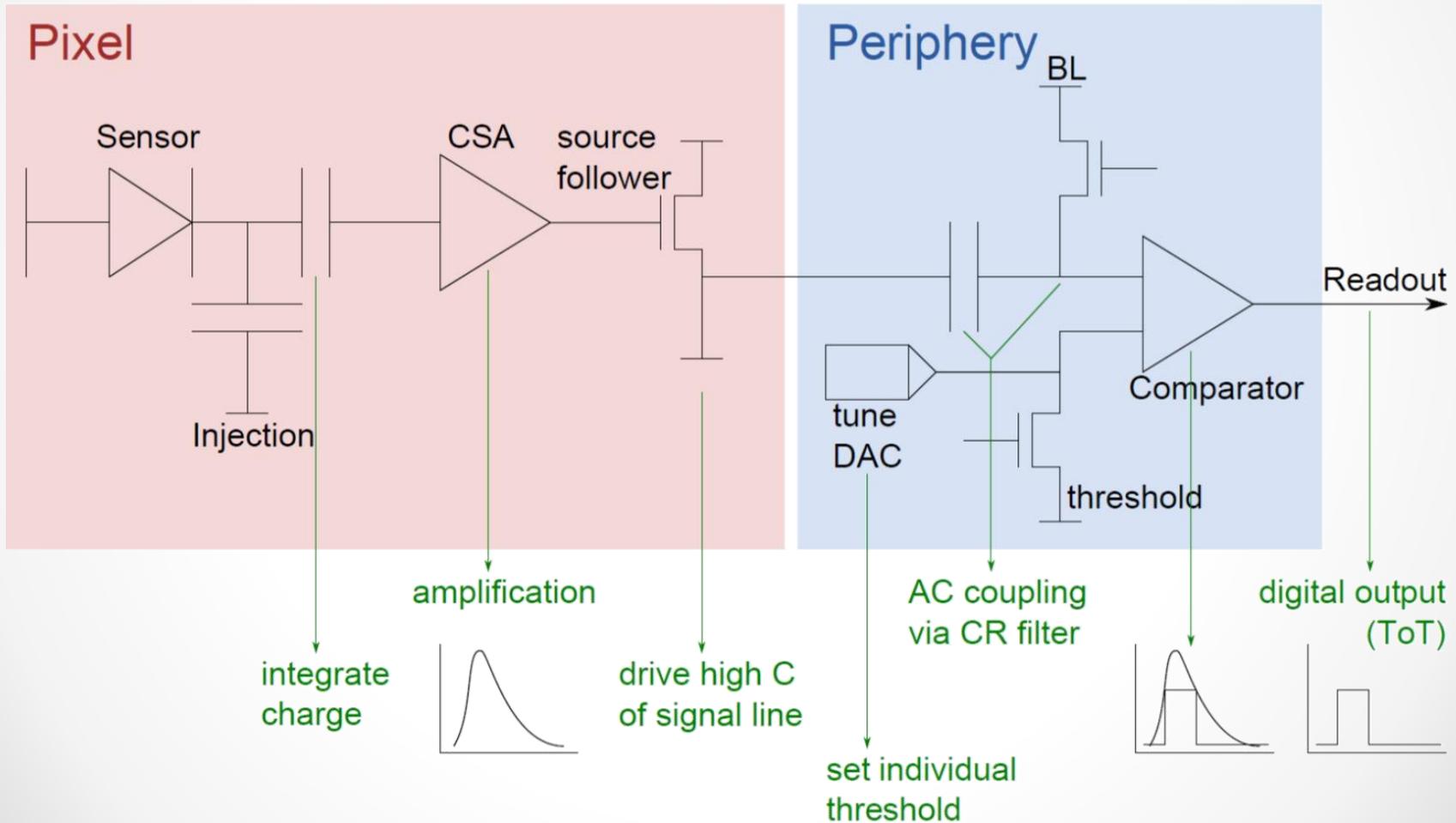
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Sensor + Analog + Digital



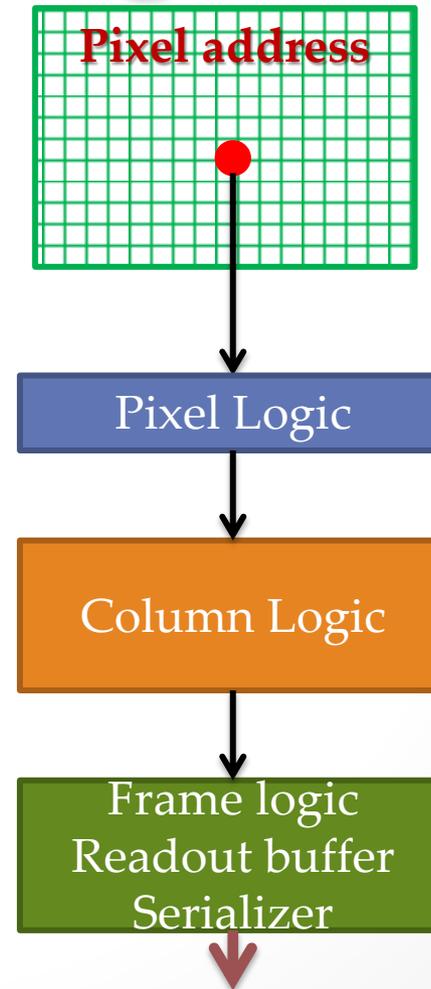


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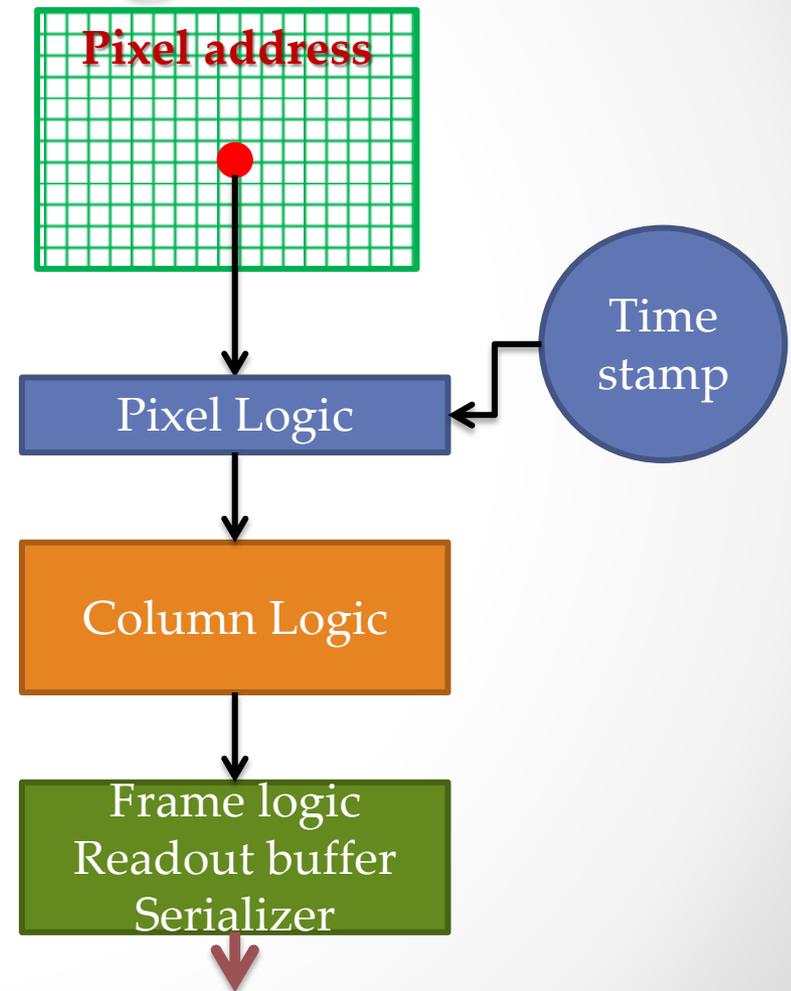
Digital Logic

- Pixel logic:
 - Address generation
 - Time stamp
 - Column bus logic
- Column logic
 - Priority logic
 - ... using tri-state bus
 - Fifo buffer
- Chip wide logic
 - Data frame generation
- Serializer(s)
 - 800 Mbit/s LVDS



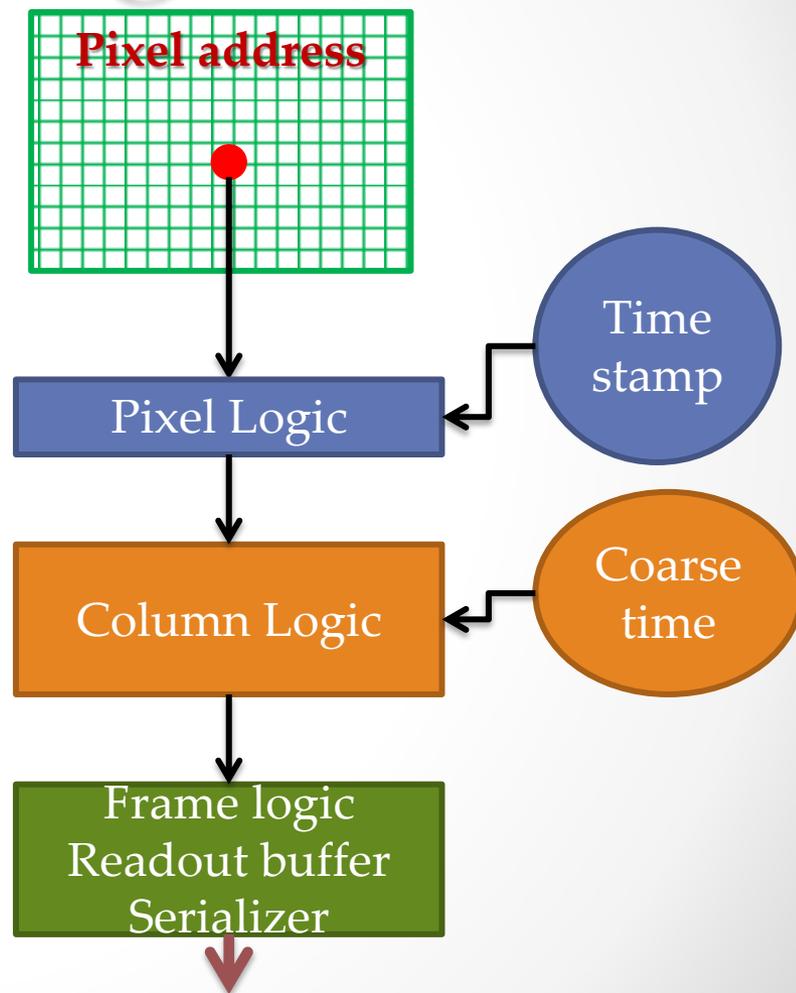
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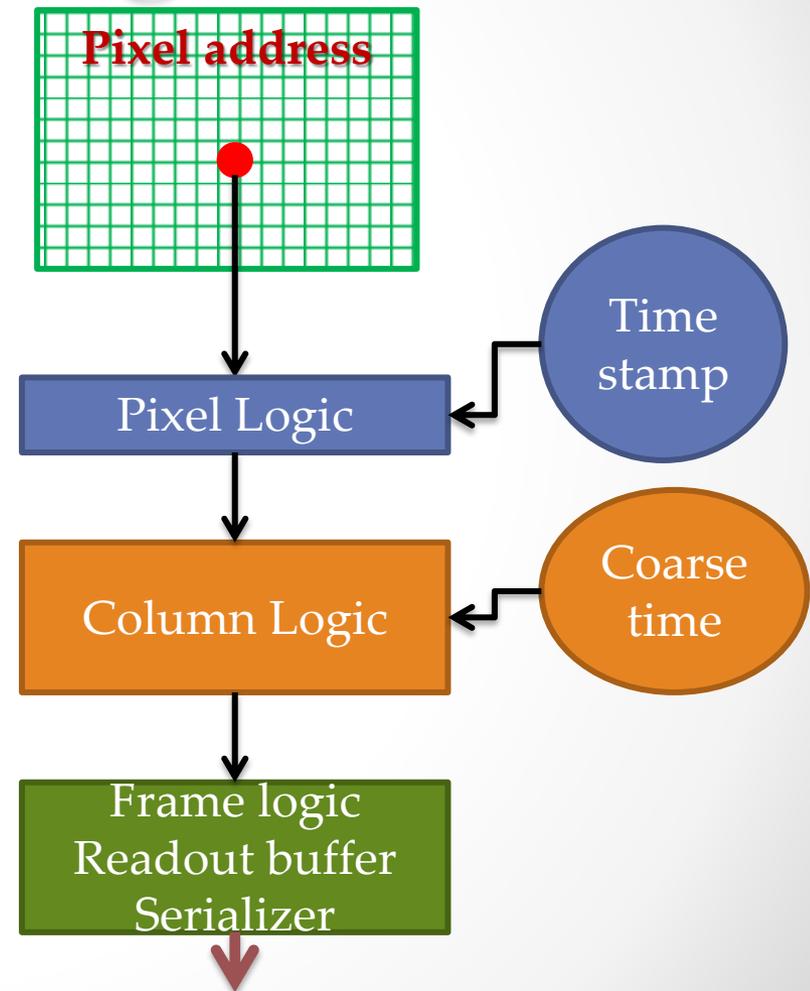
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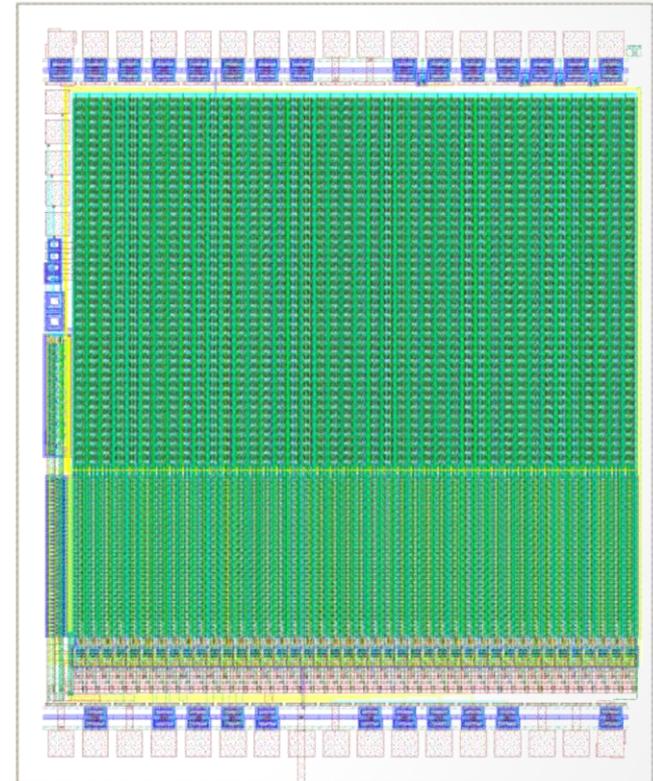


Test Results

...

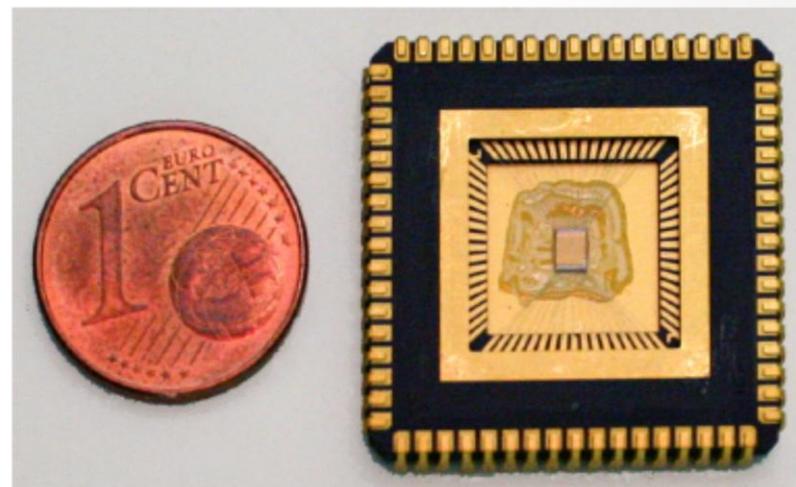
Current Chip Prototype

- 180 nm HV-CMOS
- Pixel matrix:
 - 42 x 36 pixel
 - 39 x 30 μm^2 each
- Ivan Peric ZITI
 - Analog part almost final
 - Digital part in next submission

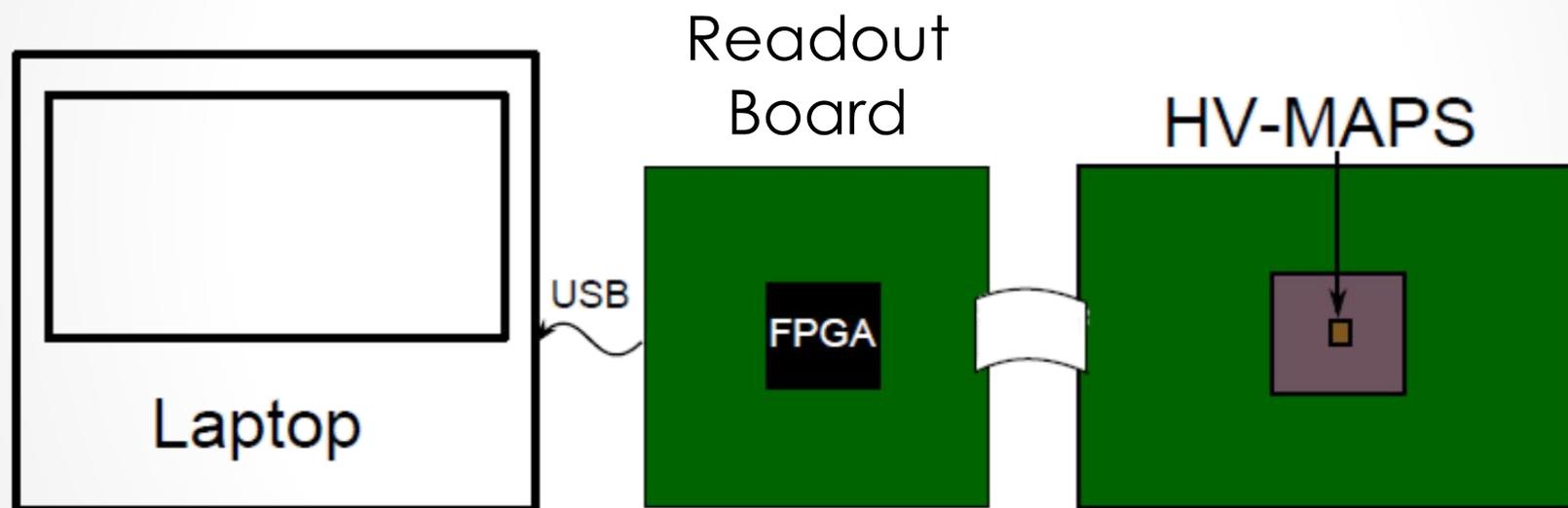


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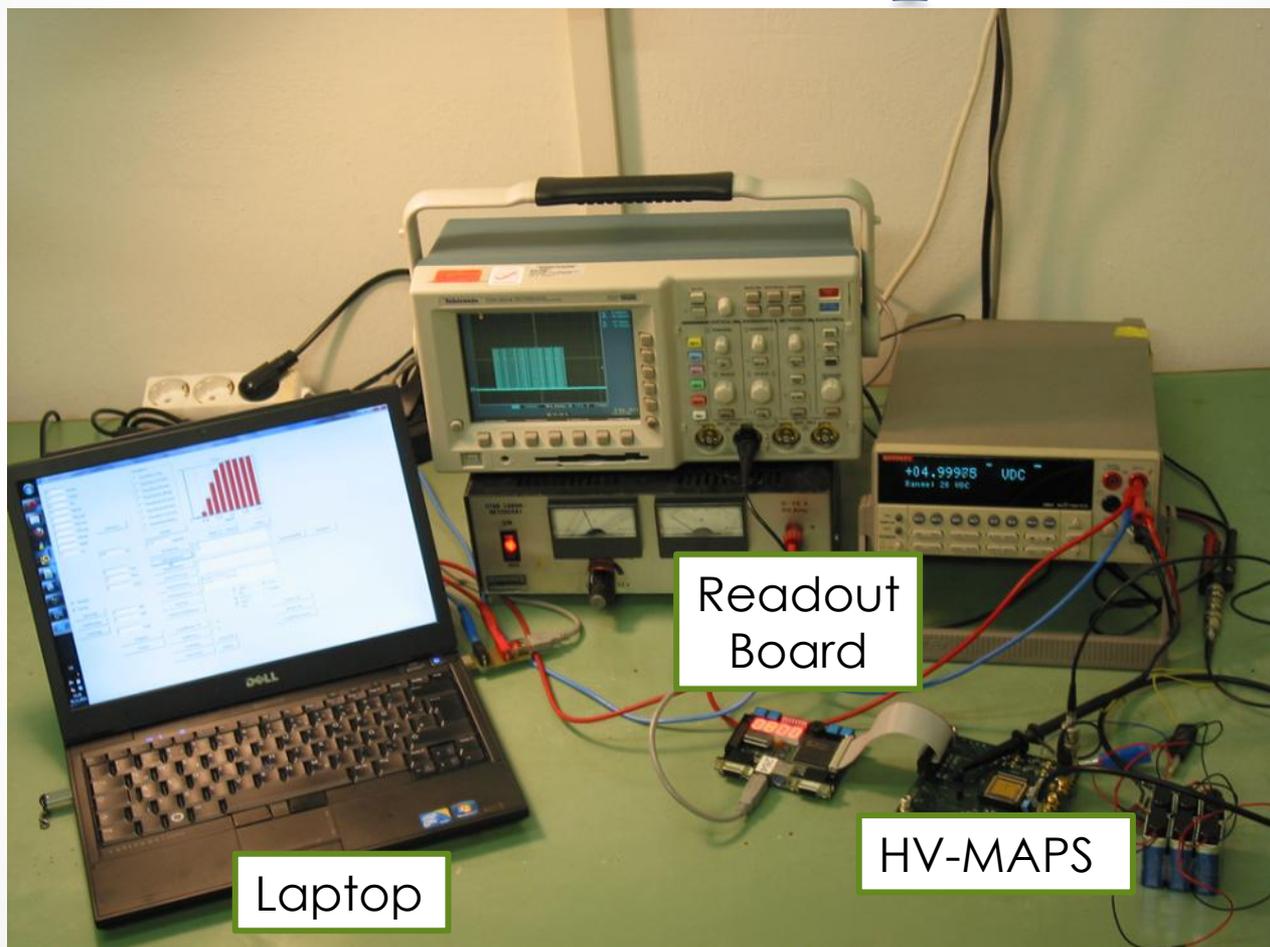
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Test Setup



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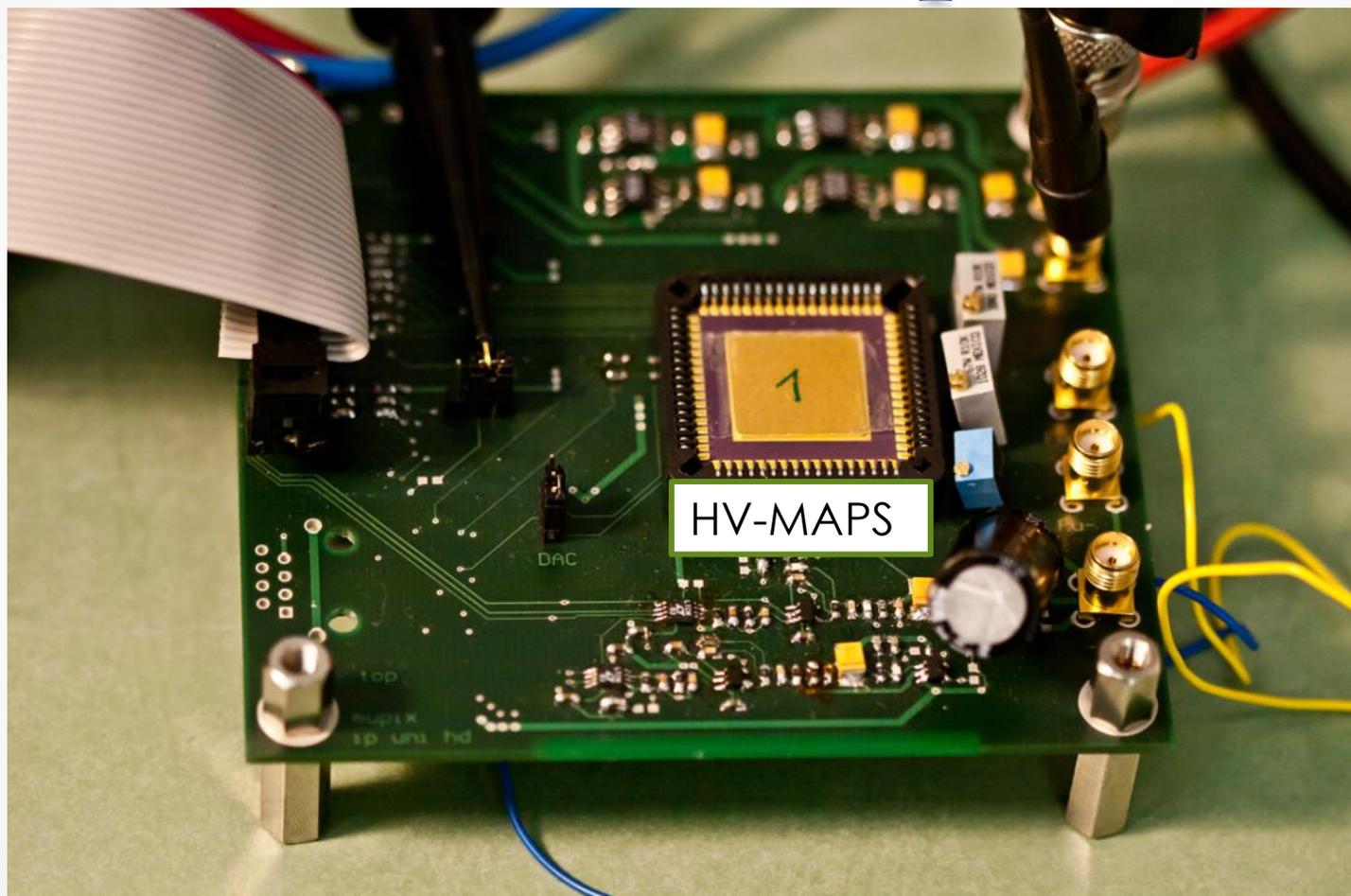


Laptop

Readout Board

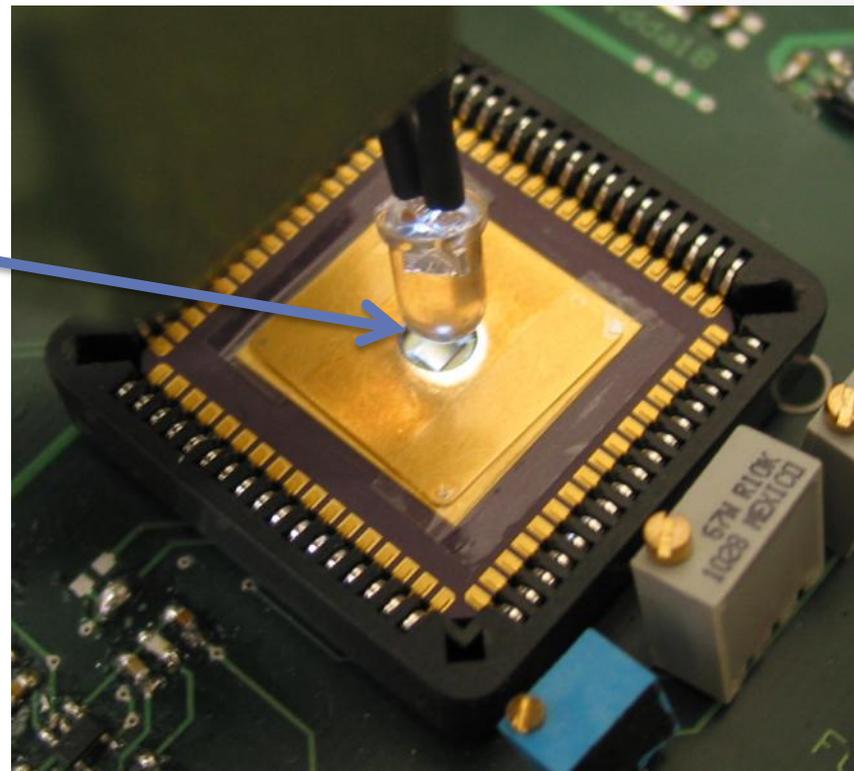
HV-MAPS

Test Setup



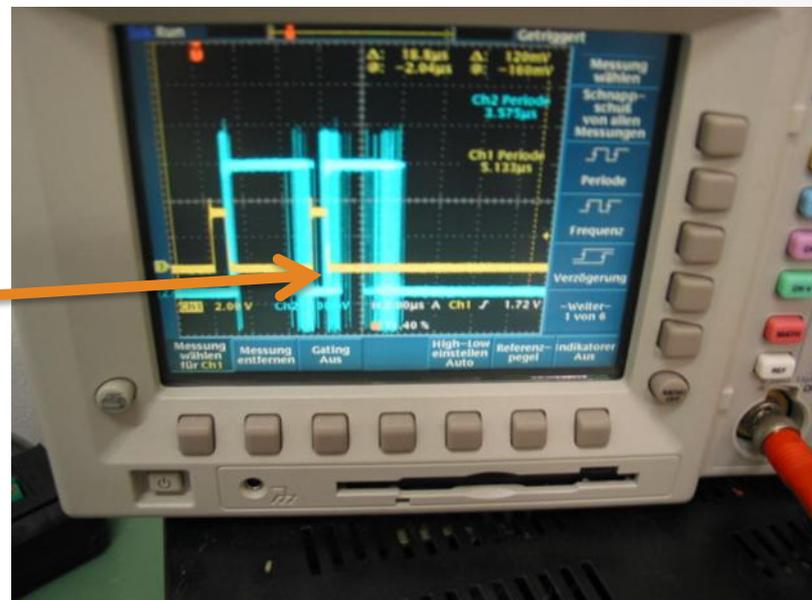
Timing Tests

- Timing critical
 - $10^9 \mu/s$
 - $O(10 \text{ ns})$ resolution
- LED pulsed sensor
- Double pulse resolution



Timing Tests

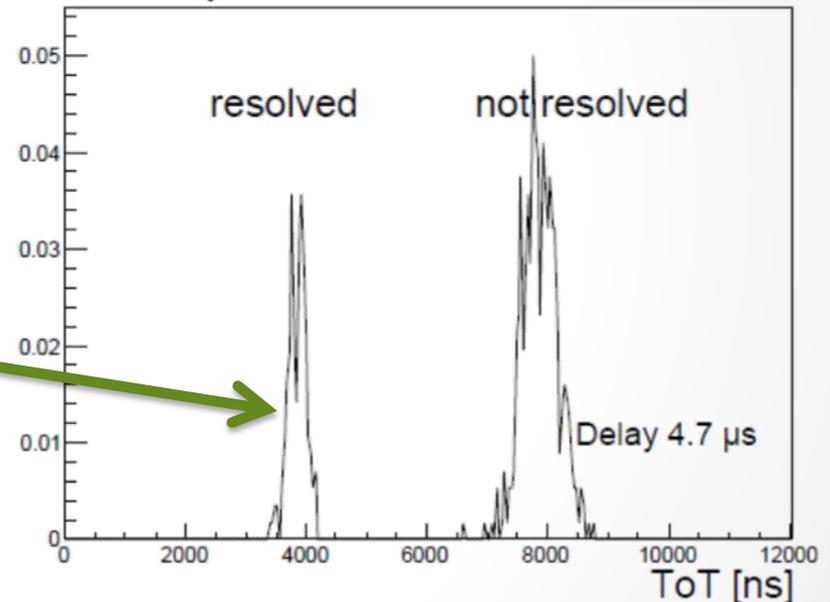
- LED pulsed sensor
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 - Visible in oscilloscope



Timing Tests

- LED pulsed sensor
- Double pulse resolution
 - Visible in oscilloscope
 - ... or time over threshold

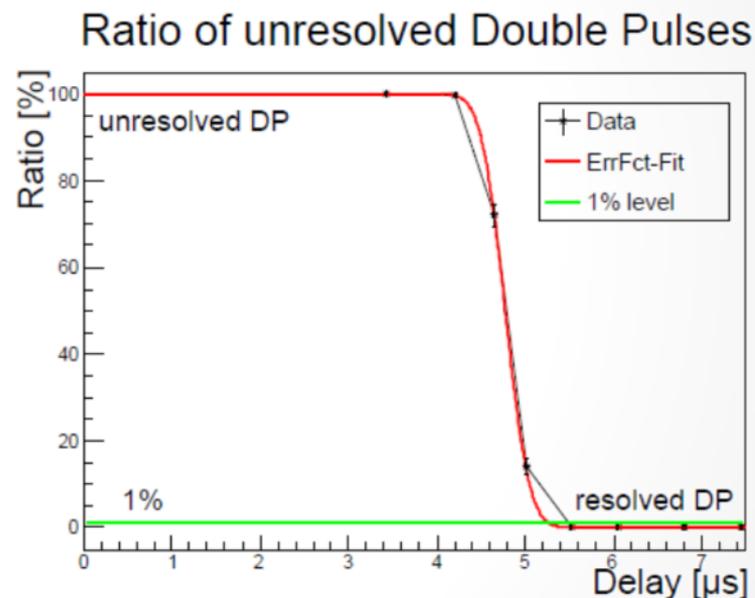
ToT Spectrum of Double Pulses





Double Pulse Resolution

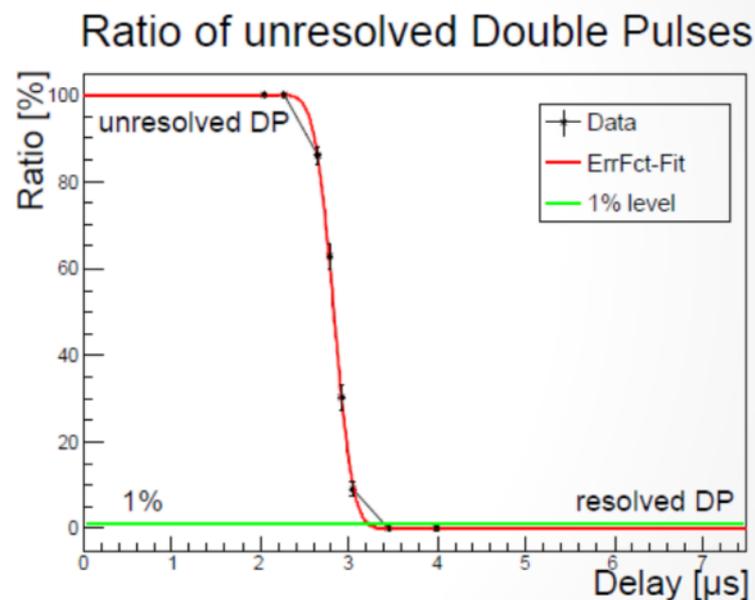
- Ratio of
 - resolved to
 - unresolved double pulses
- Default: $5.27 \pm 0.01 \mu\text{s}$





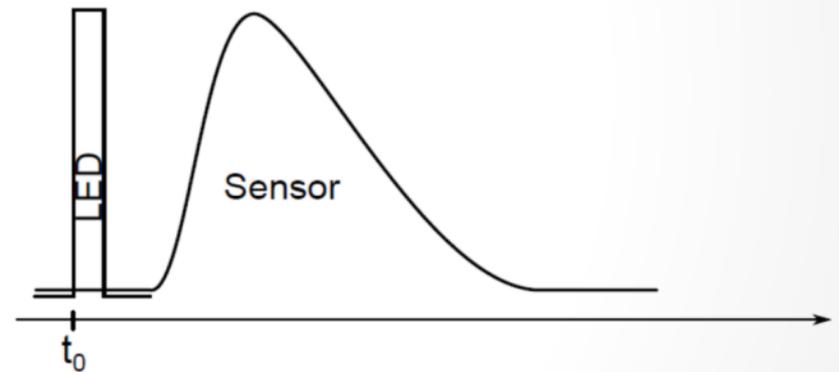
Double Pulse Resolution

- Ratio of
 - resolved to
 - unresolved double pulses
- Default: $5.27 \pm 0.01 \mu\text{s}$
 - Pixel bias current adjustment
 - Optimized: $3.23 \pm 0.01 \mu\text{s}$
 - Further reduction required



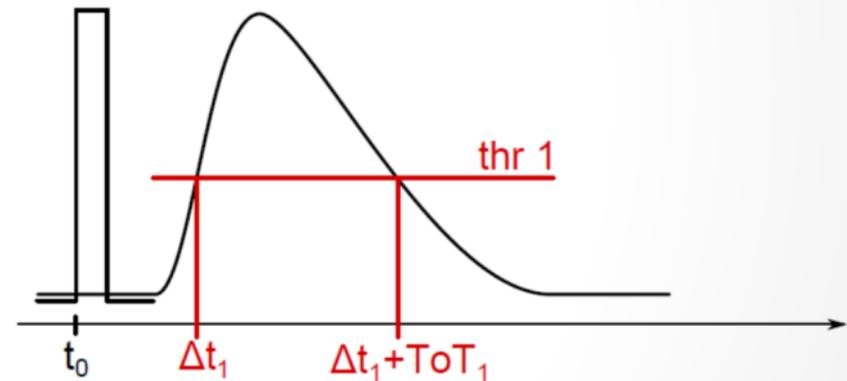
Pulse Shape

- LED setup
- Test pulse latency
- + time over threshold
- ... for different thresholds



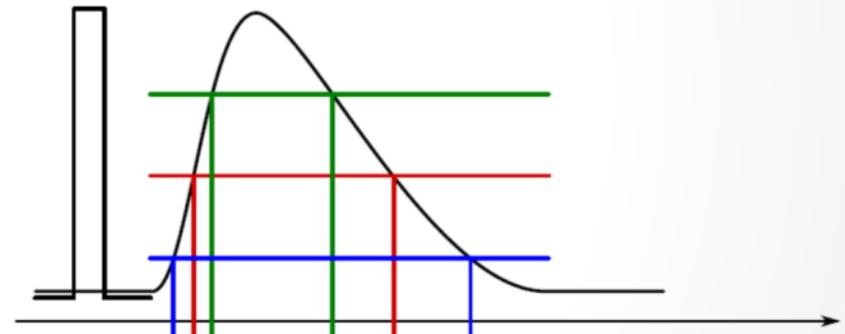
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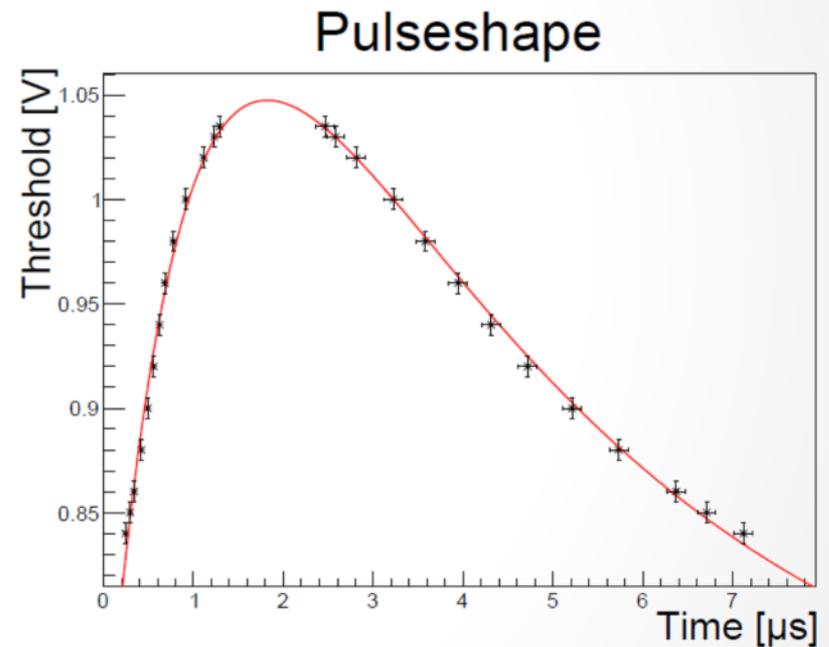
Pulse Shape

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Pulse Shape

- LED setup
- Test pulse latency
- + time over threshold
- ... for different thresholds
- faster shaping needed

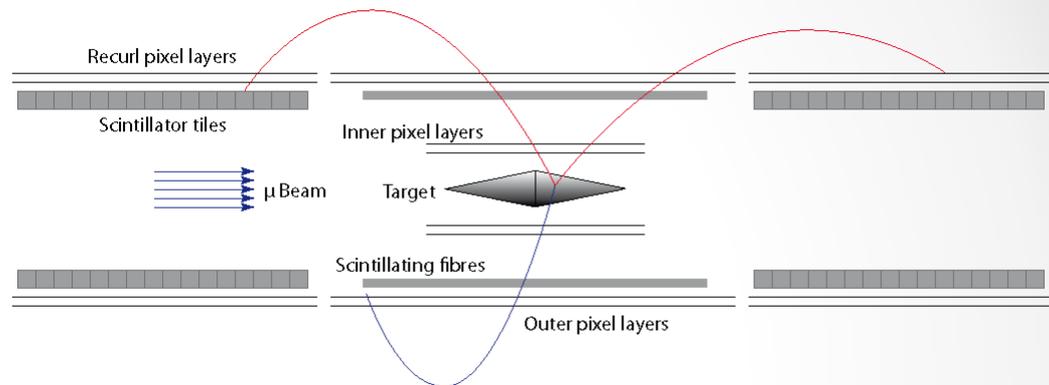




Construction

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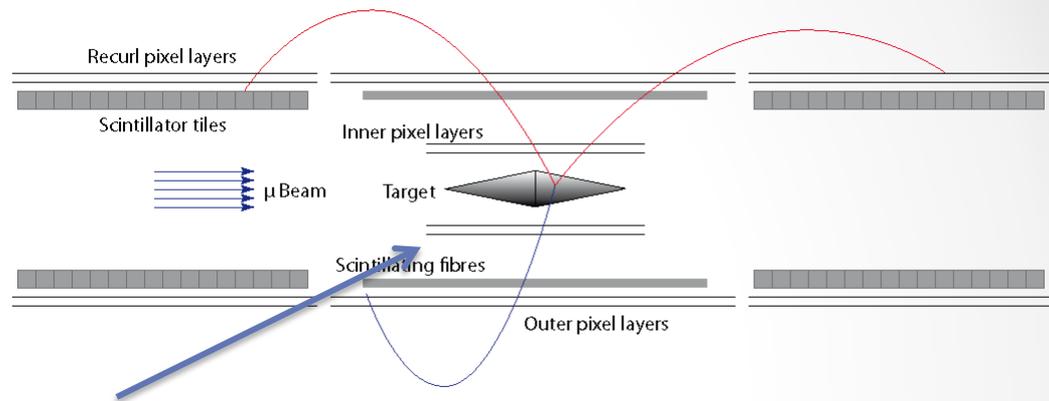
Mu3e Silicon Detector



- Conical target
- Inner double layer
 - 12 and 18 sides of 1 x 12 cm
- Outer double layer
 - 24 and 28 sides of 2 x 36 cm
- Re-curl layers
 - 24 and 28 sides of 2x 72 cm
 - Both sides (x2)

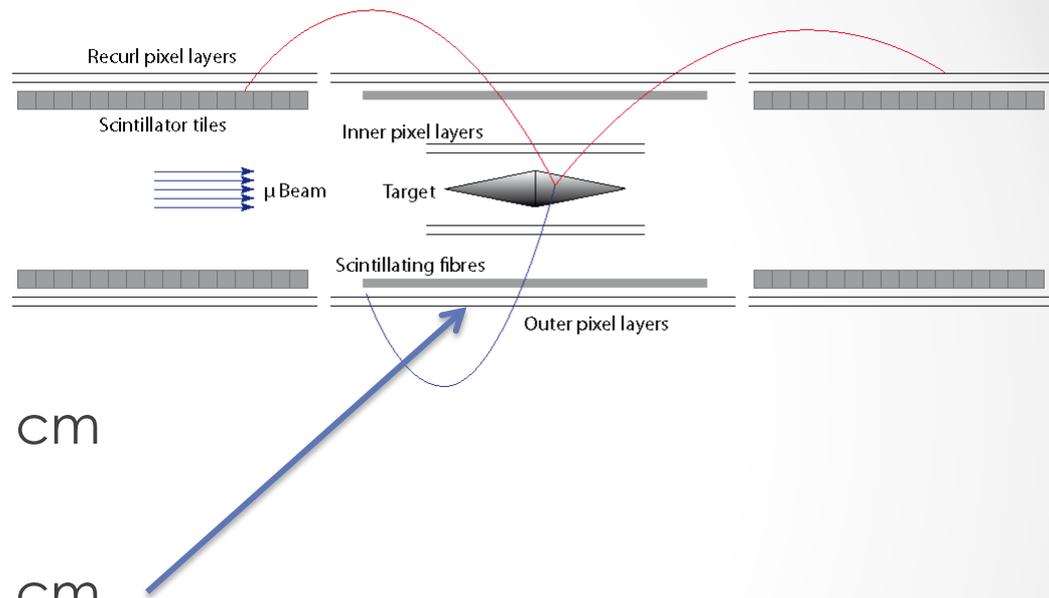
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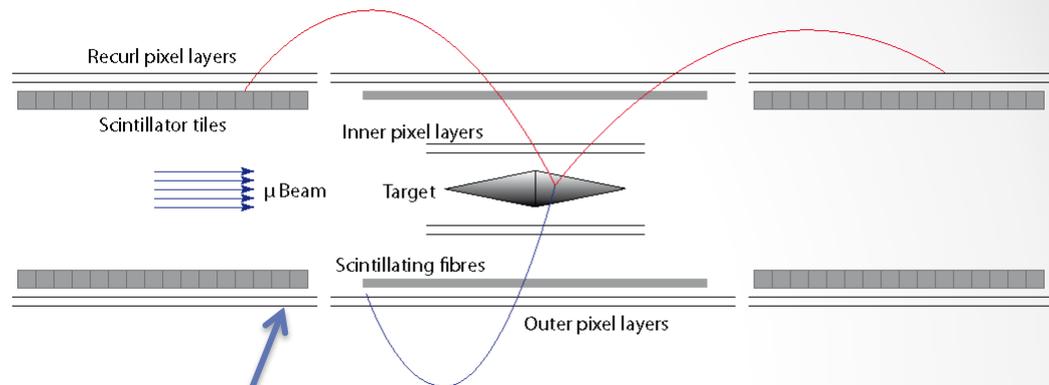
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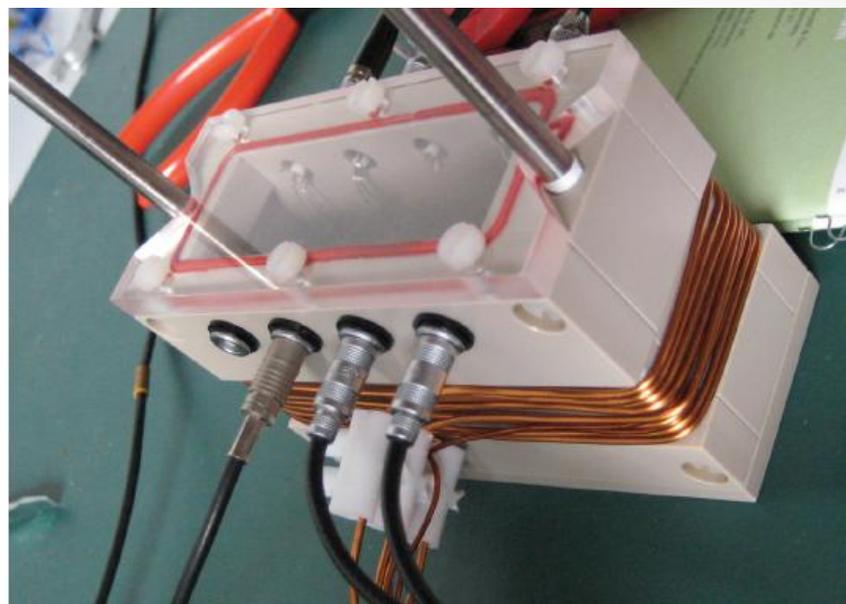
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180 inner sensors
4680 outer sensors
➤ 274 752 000 pixel

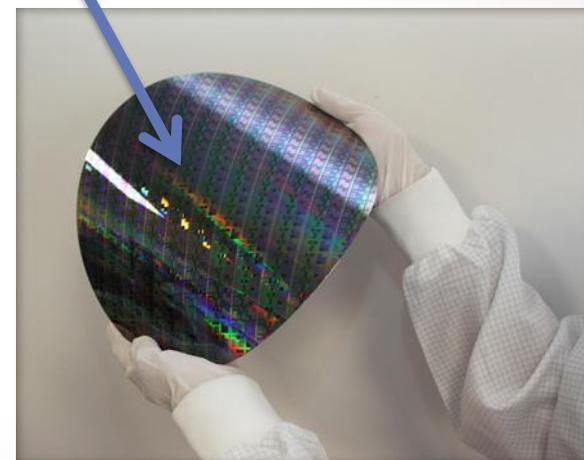
Cooling

- 2 m² silicon detector
- Up to 200mW/cm²
- 60 °C maximum
- Gaseous helium
- Laminar flow
- Tests:
 - Inductive heating
 - Aluminum foil



Thinning

- 50 μm Si-wafers
 - Commercially available
 - HV-CMOS 75 μm (AMS)
- Single die thinning
 - For chip sensitivity studies
 - < 50 μm desirable
 - In house grinding?

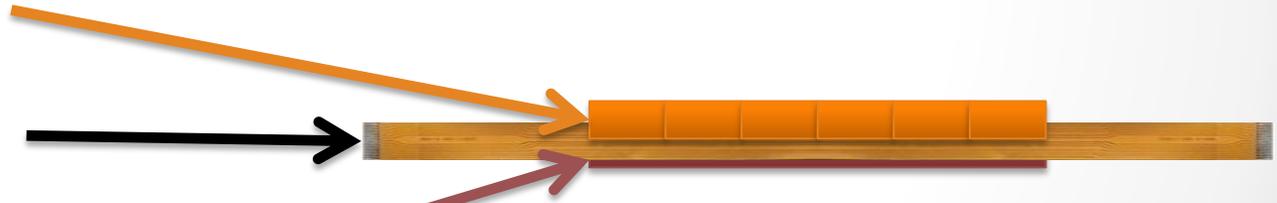


Material

- HV-MAPS

- Flex print

- Kapton Frame

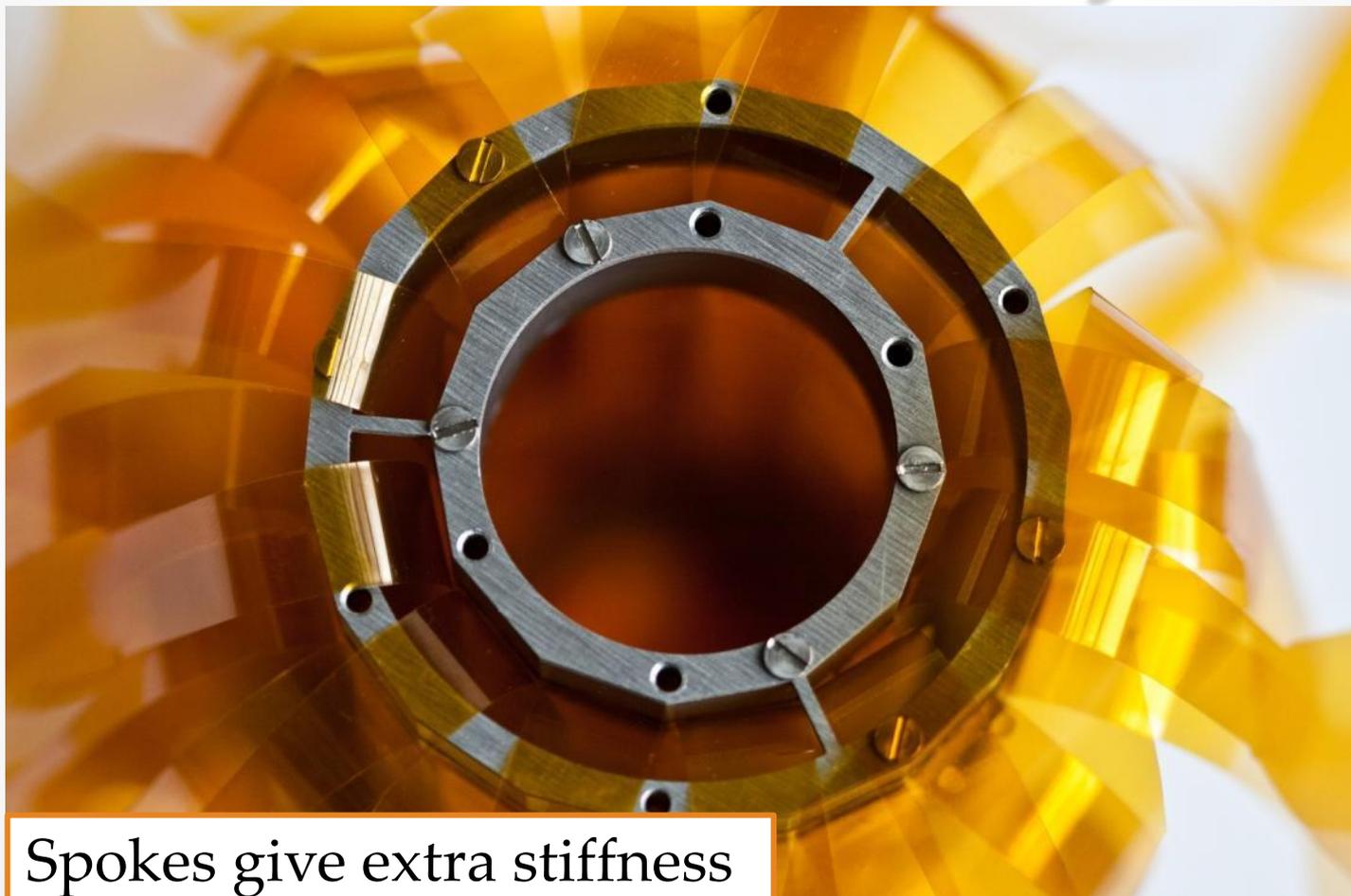


Inner Double Layer



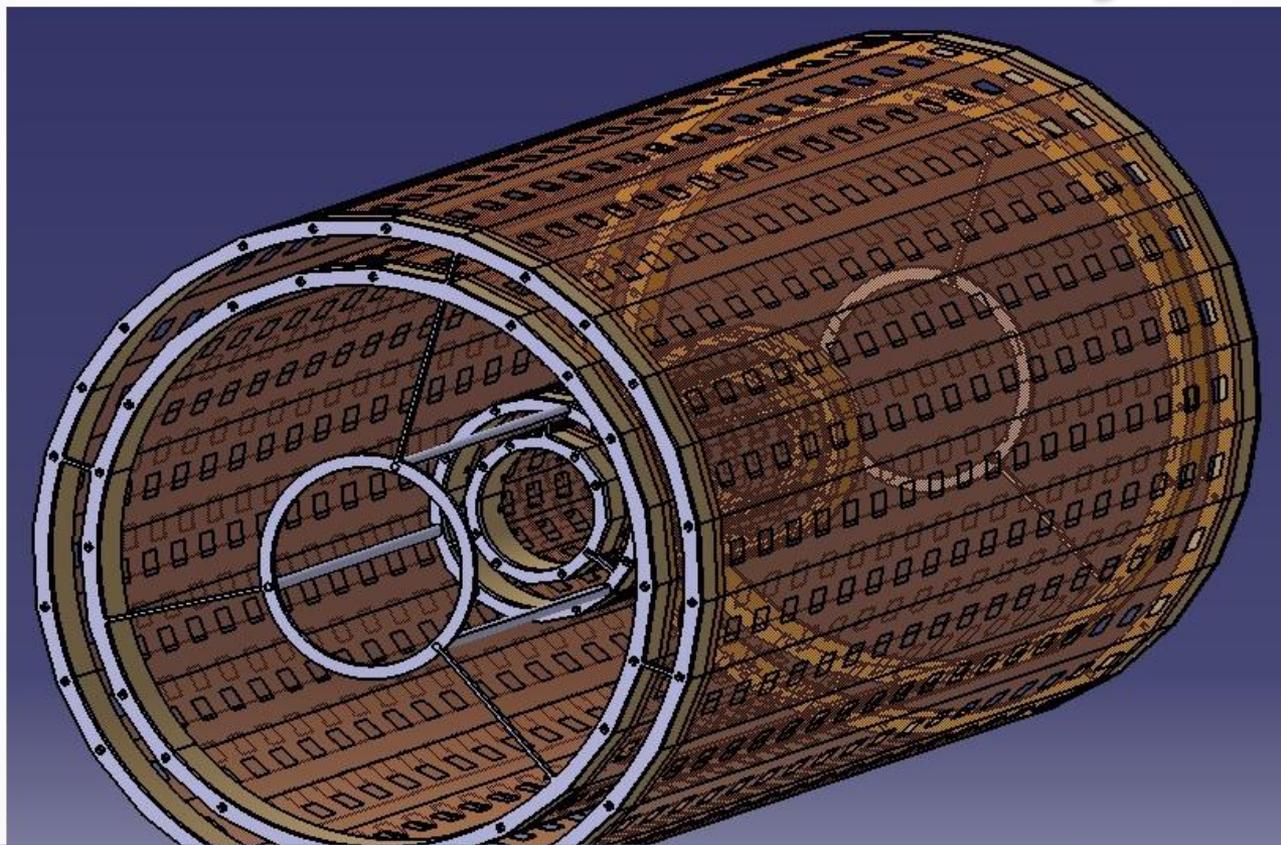
Very stable self supporting structure

Inner Double Layer



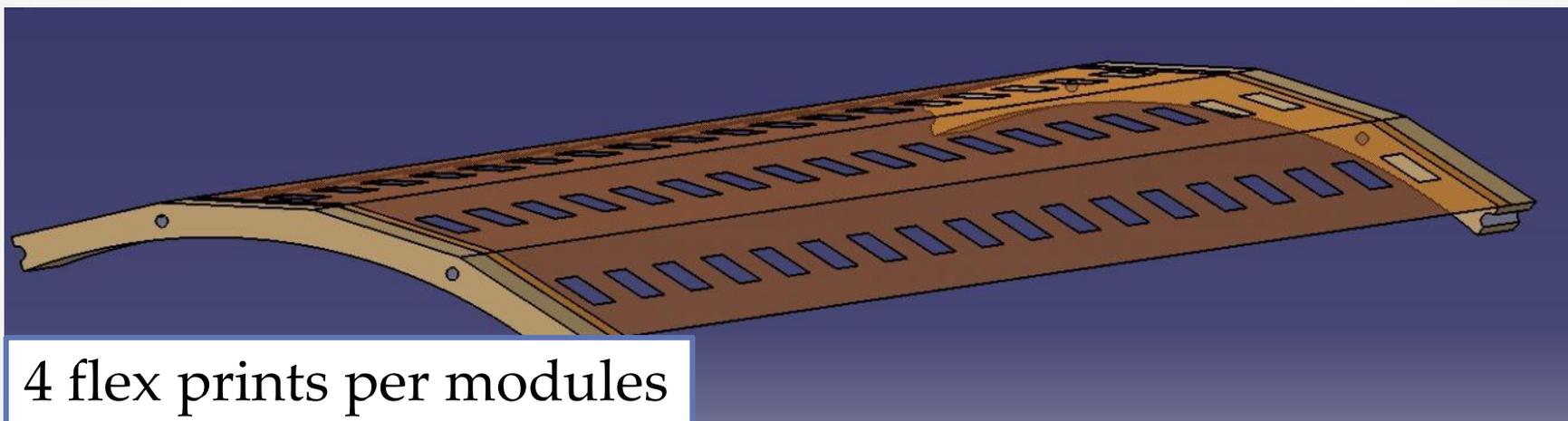
Spokes give extra stiffness

Outer Double Layer

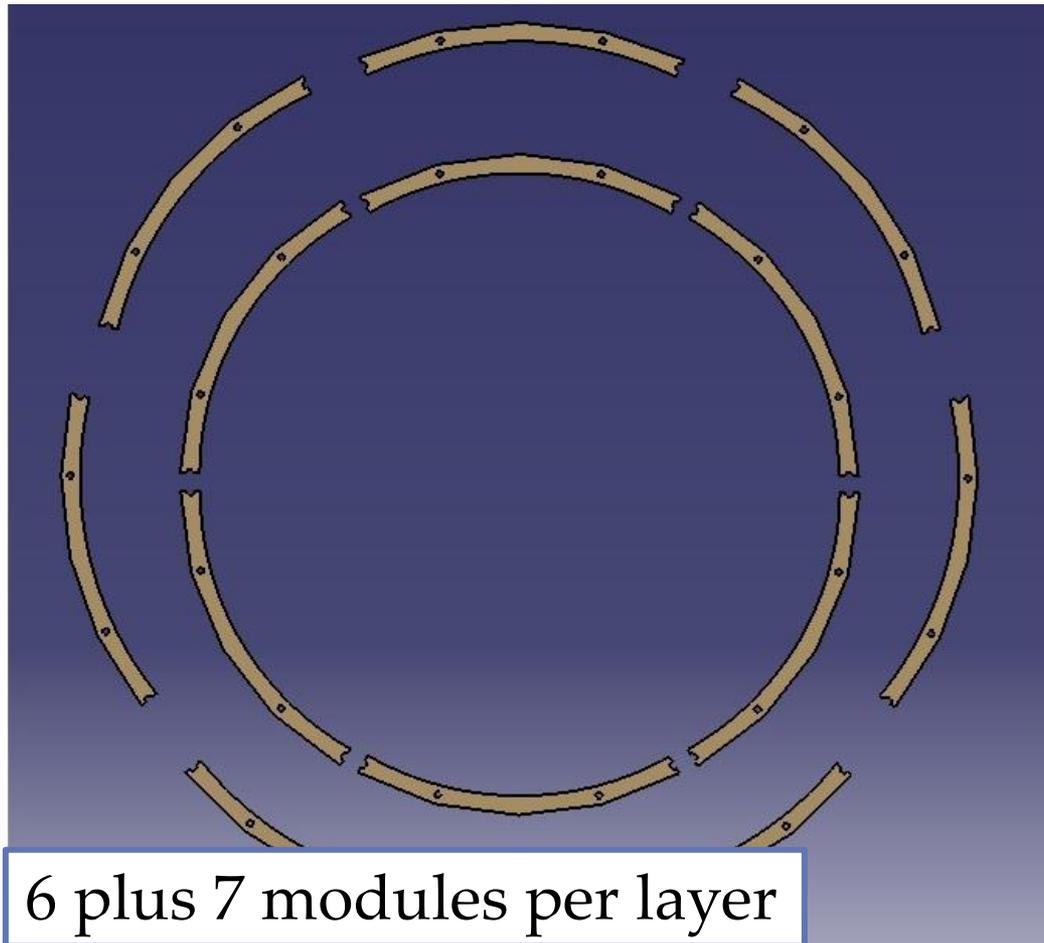


Minimal material in sensitive region

Outer Double Layer



End Pieces

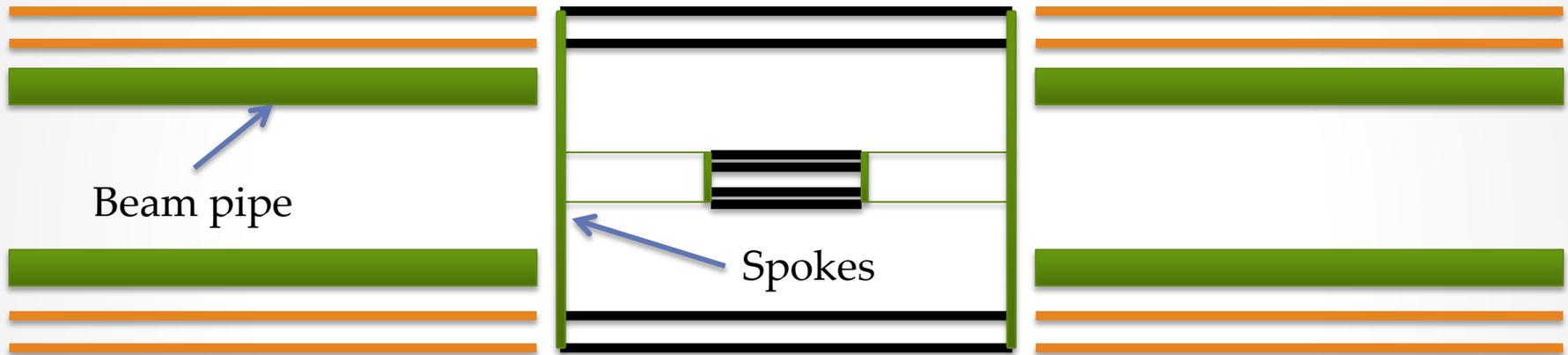


End Pieces

- End pieces for modules
 - PVC
 - PEEK in future?
- Production done

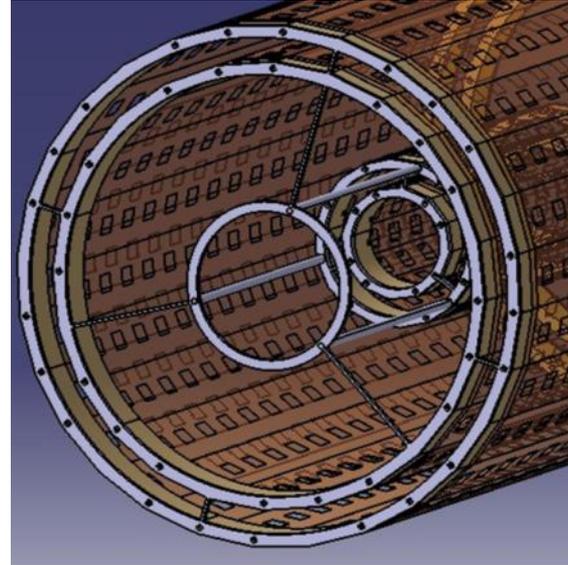


Frame Support



- Support design light weight
 - Spokes combine all separate modules
 - Connected by metal beams
 - ... running in bushings

Frame Support

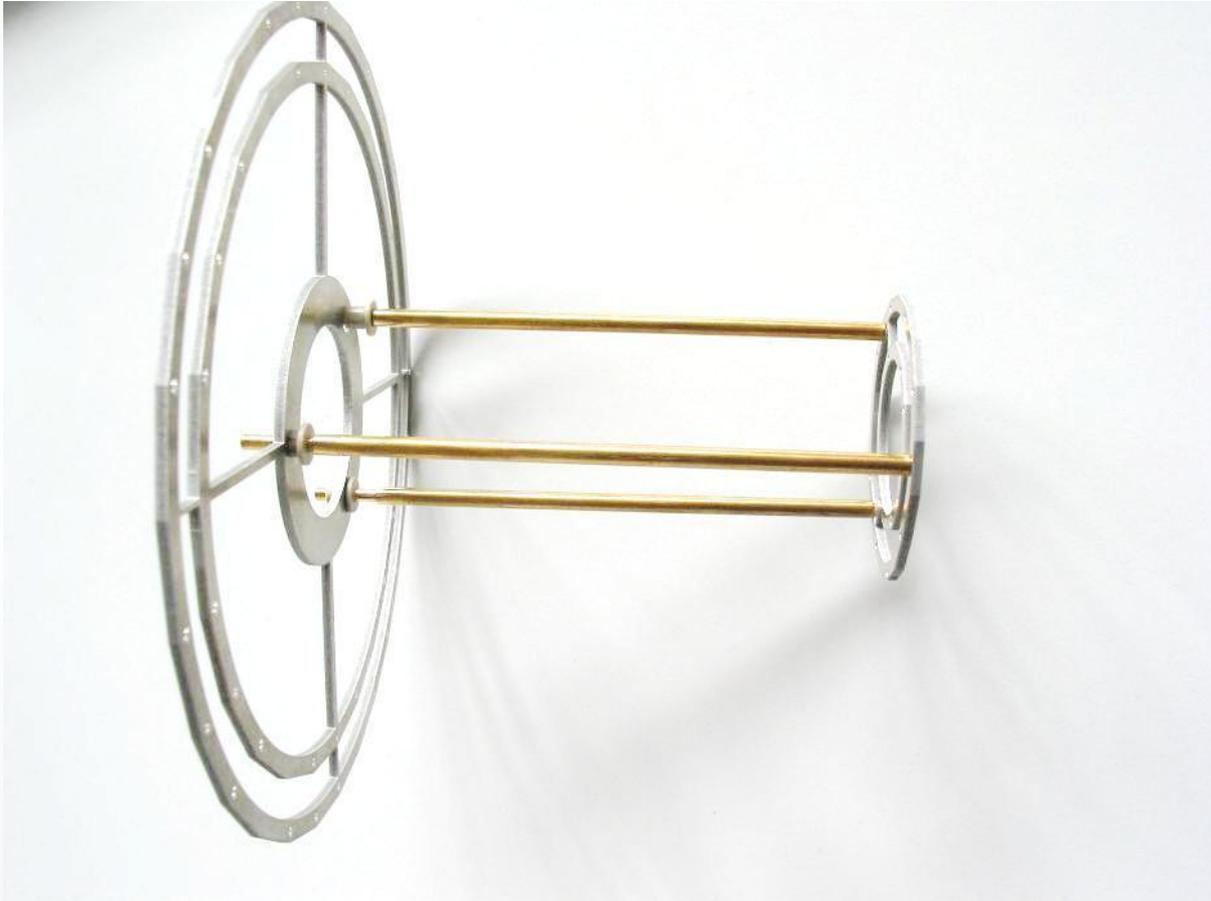


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Spoke Assembly

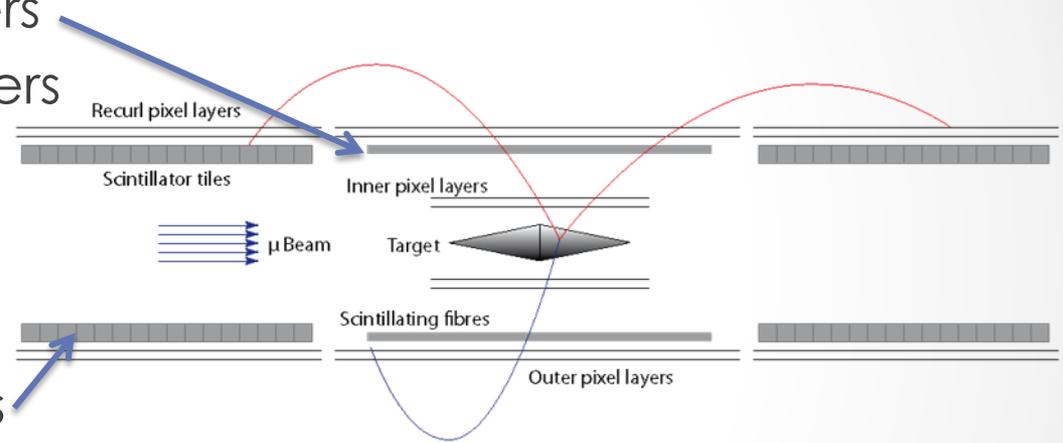


Spoke Assembly



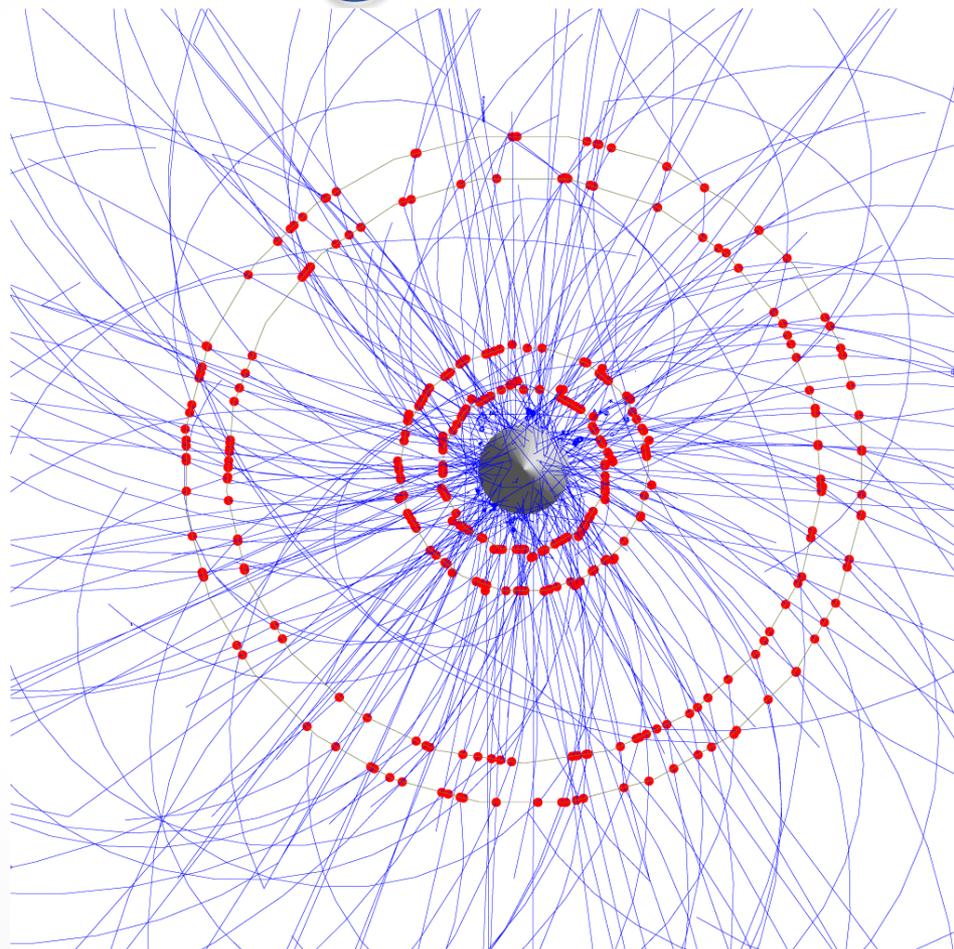
Timing Detectors

- Fiber hodoscope
 - Before outer pixel layers
 - 250 μm scintillating fibers
 - SiPMs
 - 1 ns resolution

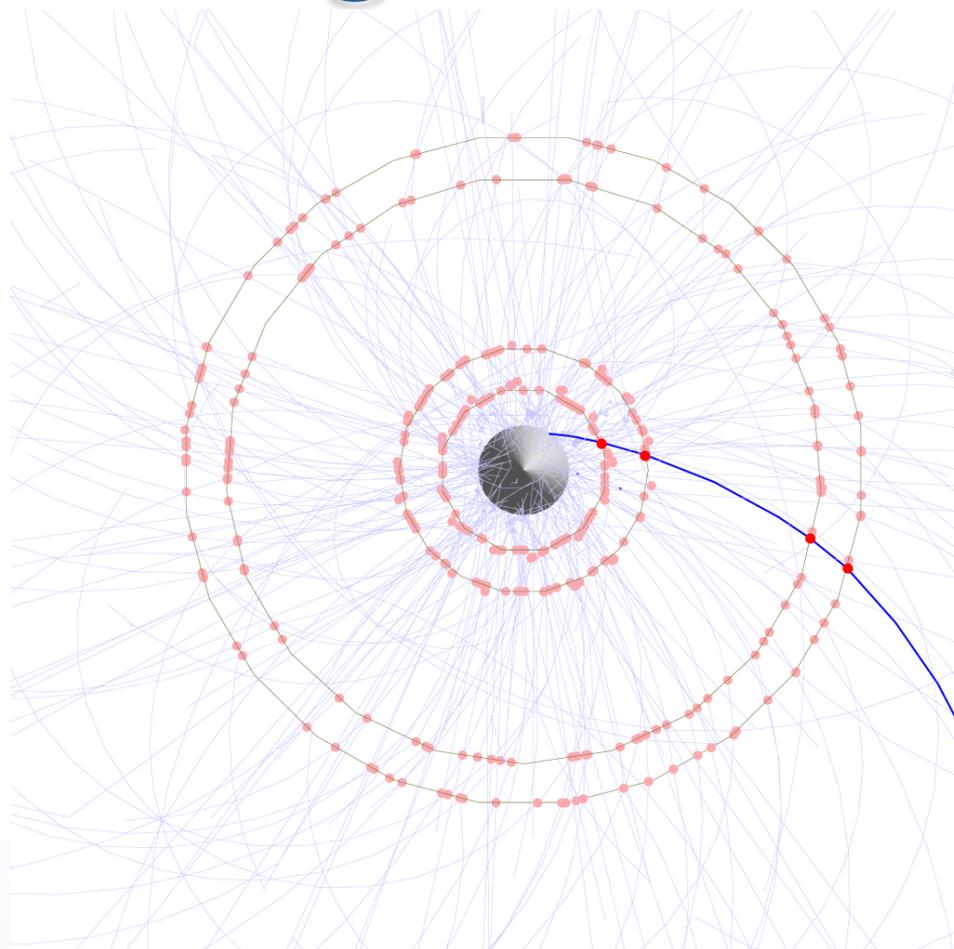


- Tile detector
 - After recurl pixel layers
 - 1x1 cm^2 scintillating tiles
 - SiPMs
 - 100 ps resolution

Timing Detectors



Timing Detectors



Fiber Hodoscope

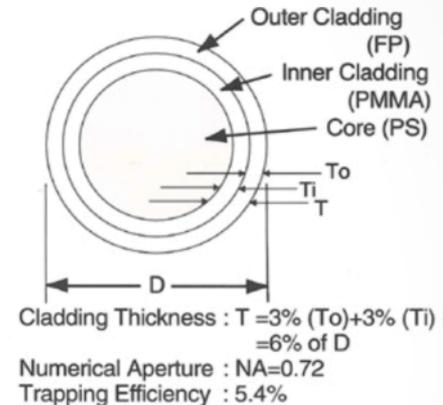
- 250 μm scintillating fibers
 - Kuraray SCSF-81M
 - double cladding
 - 7500 in total
- Very high occupancies:
 - 24% in 50ns time frame
- Sampling readout
 - SiPM
 - DRS5 chip
 - From Stefan Ritt, PSI



Kuraray

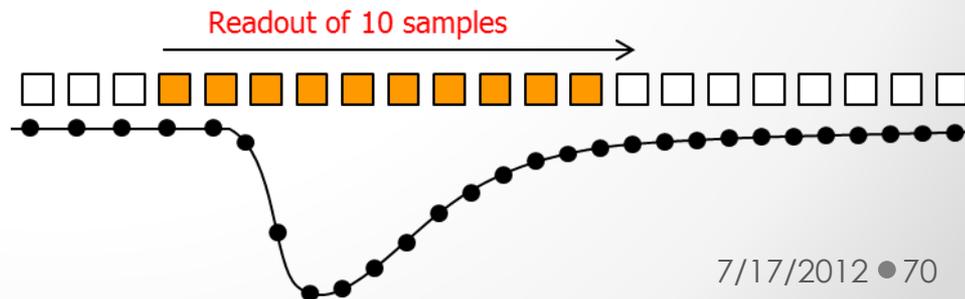
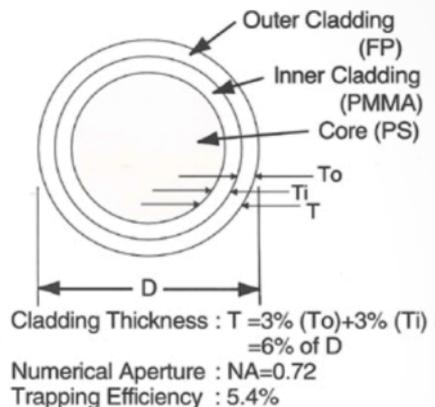
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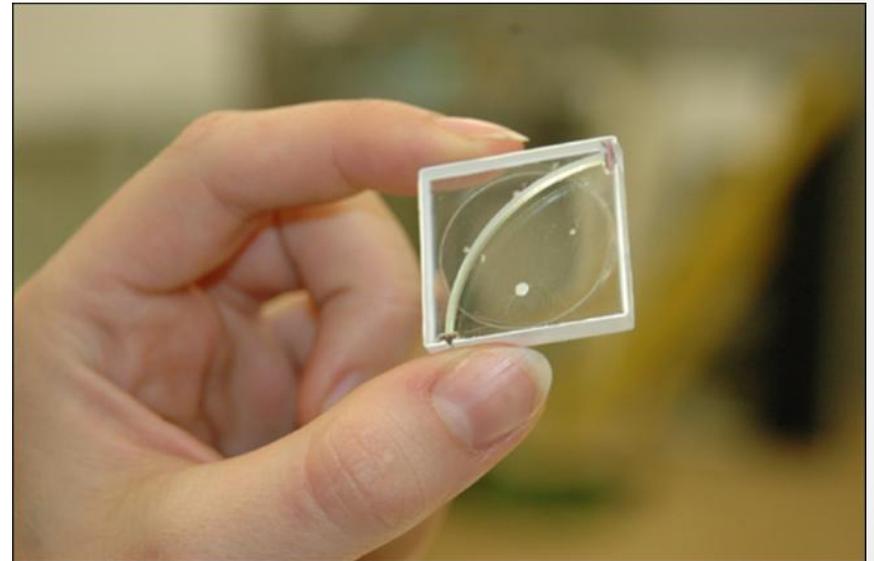
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Tile Detector

- 1x1 cm² scintillating tiles
 - O(7000)
- GosSip simulation
 - MPPC with 3600 pixels
 - 100 ps resolution (RMS)
 - 97% efficiency

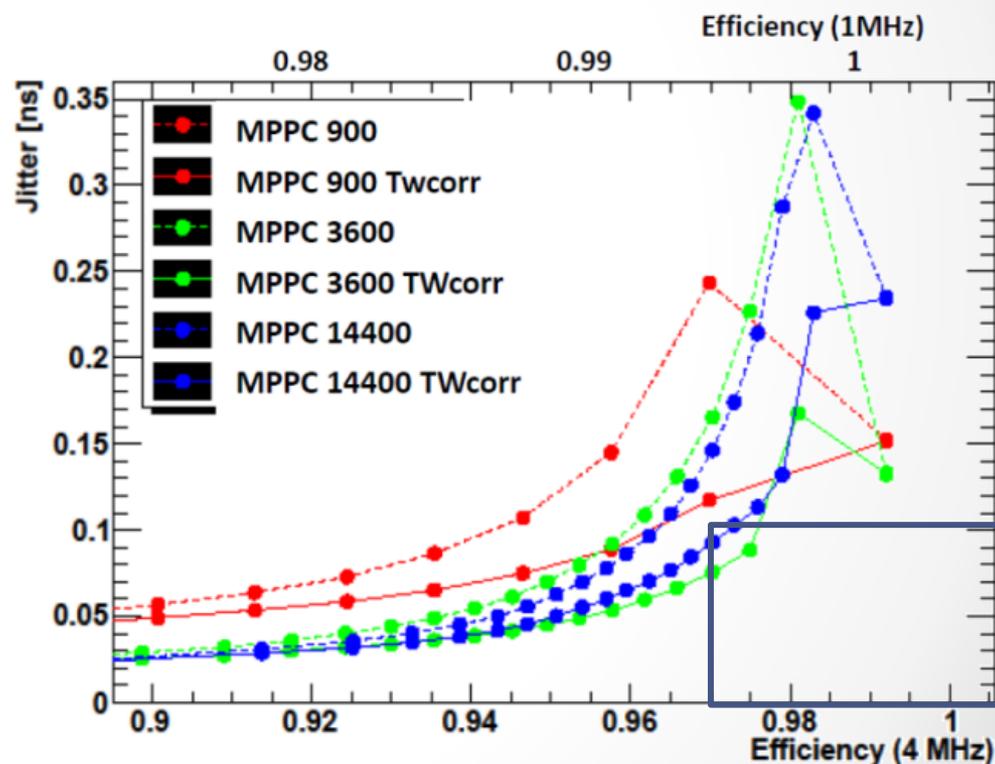


Kirchhoff-Institut für Physik



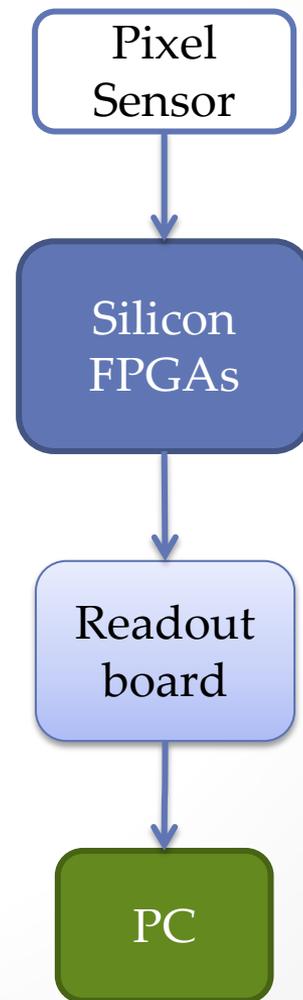
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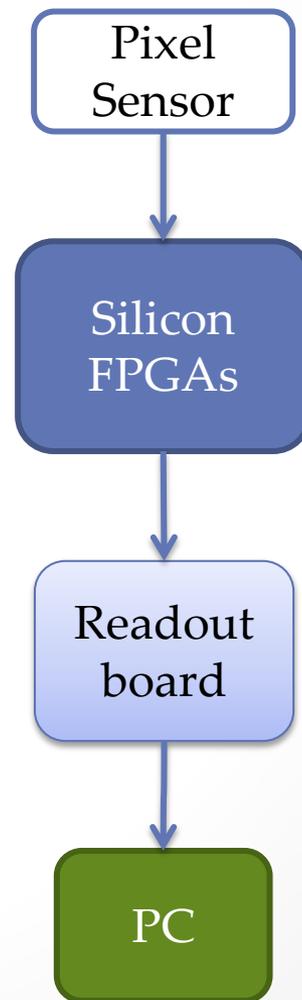
Data Acquisition

- 2.5 GHz muon decays
- 50 ns readout frames
- $O(5000)$ pixel chips
 - 800 Mb/s readout links
- $O(7500)$ scintillating fibers
- $O(7000)$ timing tiles
 - DRS readout
- 3 layers switching FPGAs
 - Optical data links
- Online filtering



Data Acquisition

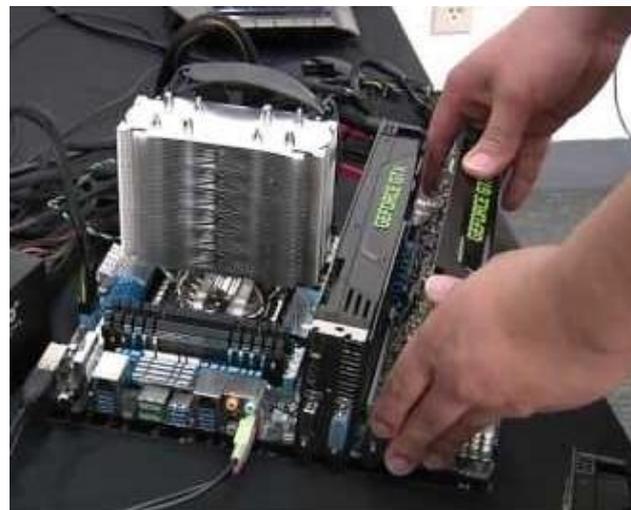
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Event Filter Farm

- Triggerless readout
- GPU computers
 - PCIe FPGA/optical input
 - Tflop/s GPU
- 10x faster than CPU
 - Requires custom code
 - + Makes farm affordable

Optical mezzanine connectors



GPU computer

Schedule

- **2012 Letter of intent** to PSI, tracker prototype, technical design, technical design report
- **2013** Detector **construction**
- **2014** Installation and **commissioning** at PSI
- **2015** Data taking at up to a few $10^8 \mu/s$
- **2016+** Construction of **new beam-line** at PSI
- **2017++** Data taking at up to $3 \cdot 10^9 \mu/s$





Institutes

- Mu3e proto-collaboration:

- DPNC Geneva University



- Paul Scherrer Institute



- Particle Physics ETH Zürich



- Physics Institute Zürich University



- Physics Institute Heidelberg University



- ZITI Mannheim

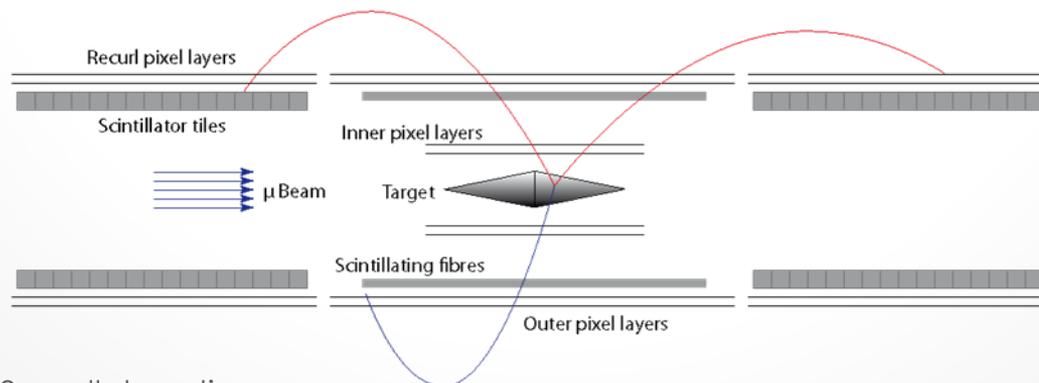


- KIP Heidelberg



Summary

- Mu3e searches for lepton flavor violation
- $> 10^{16}$ μ -decays \rightarrow BR $< 10^{-16}$ (90% CL)
- Silicon tracker with ~ 275 M pixel
- HV-MAPS 50 μ m thin
- Two SiPM based timing systems
- Prototypes look encouraging





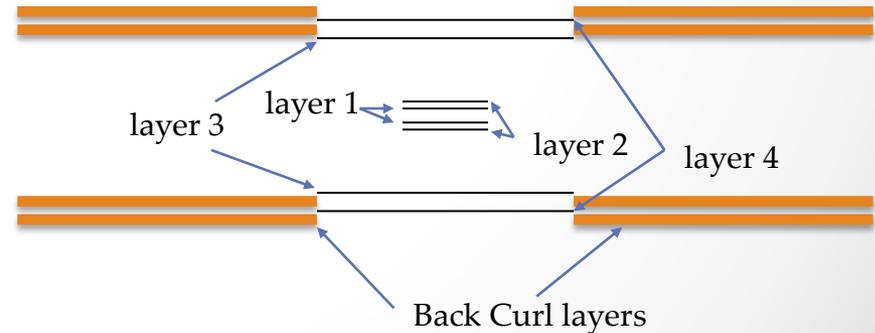
Backup Slides

...



Si-Layer Rad Length

- Radiation length per layer
 - 2x 25 μm Kapton
 - $X_0 = 1.75\text{e-}4$
 - 15 μm thick aluminum traces (50% coverage)
 - $X_0 = 8.42\text{e-}5$
 - 50 μm Si MAPS
 - $X_0 = 5.34\text{e-}4$
 - 10 μm adhesive
 - $X_0 = 2.86\text{e-}5$
- Sum: $8.22\text{e-}4$ (x4 layers)
 - For $\Theta_{\text{min}} = 22.9^\circ$
 - $X_0 = 21.1\text{e-}4$



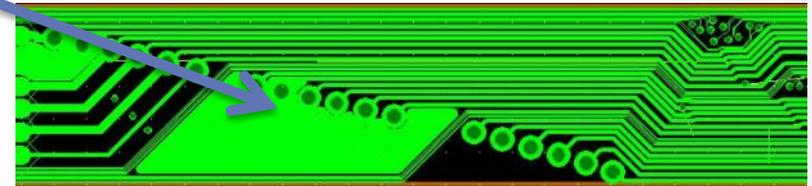
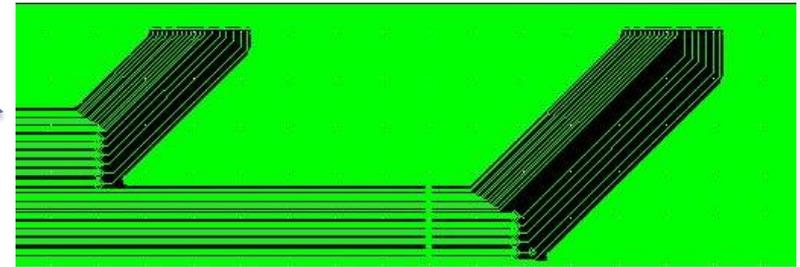
MAPS Tiles

- MAPS
 - 2 cm x 1 cm for inner layers
 - 2 cm x 2 cm for outer layers
 - Pixel size 80 μm x 80 μm
- Size defined by reticle: 2 cm x 2 cm
 - Cut 6 cm x 2 cm stripes from wafer
 - Bond to flex print
 - Mount sensor-equipped flex print on carrier



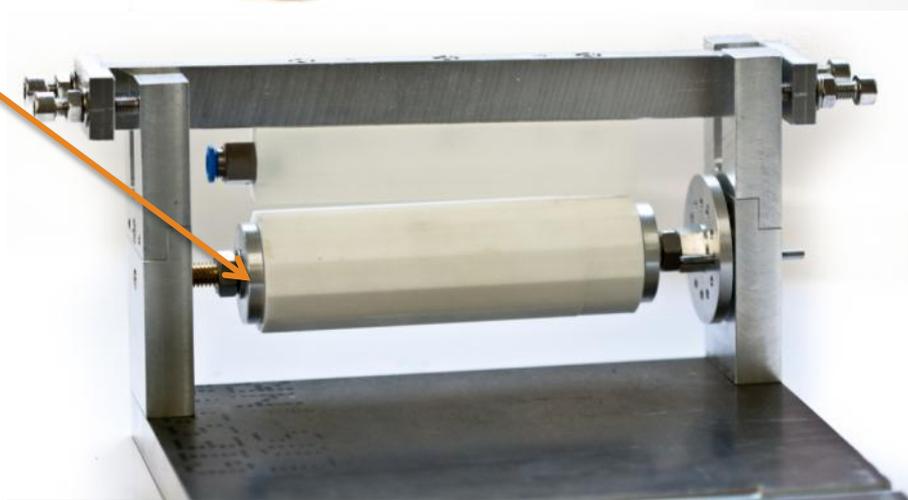
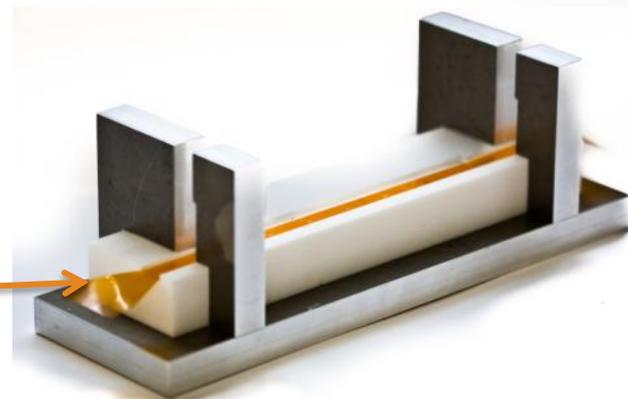
Flex Print

- Single Layer in active region
- Multilayer in “cable” end
- LVDS buffers at edge



Tools

- Kapton-Frame tools:
 - Sensor on Flex print
 - Gluing groove
 - Vacuum lift
 - Tools are tested with
 - 25 μm Kapton foil
 - 50 μm glass

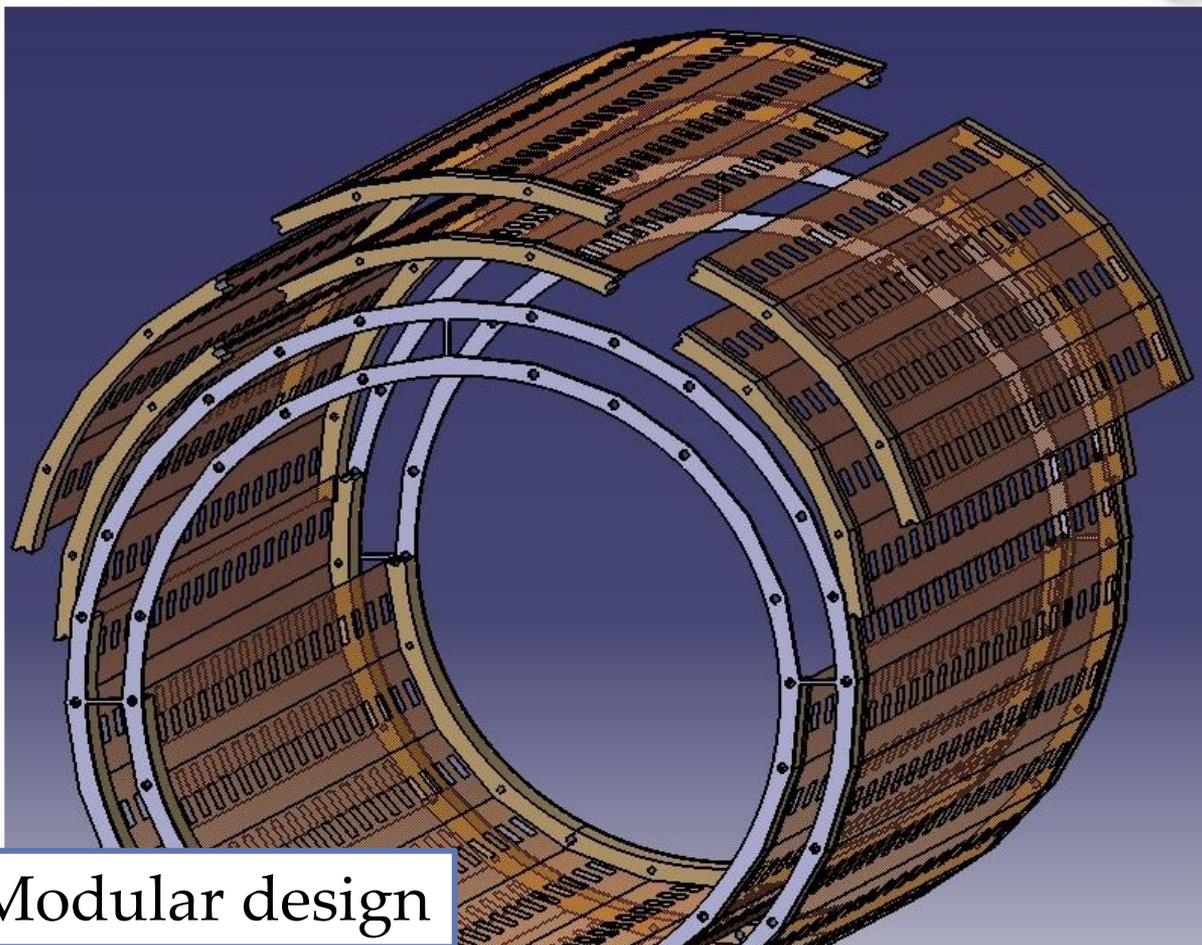


Inner Double Layer



25 μm Kapton frame
+ 25 μm Kapton strip
+ 50 μm glass

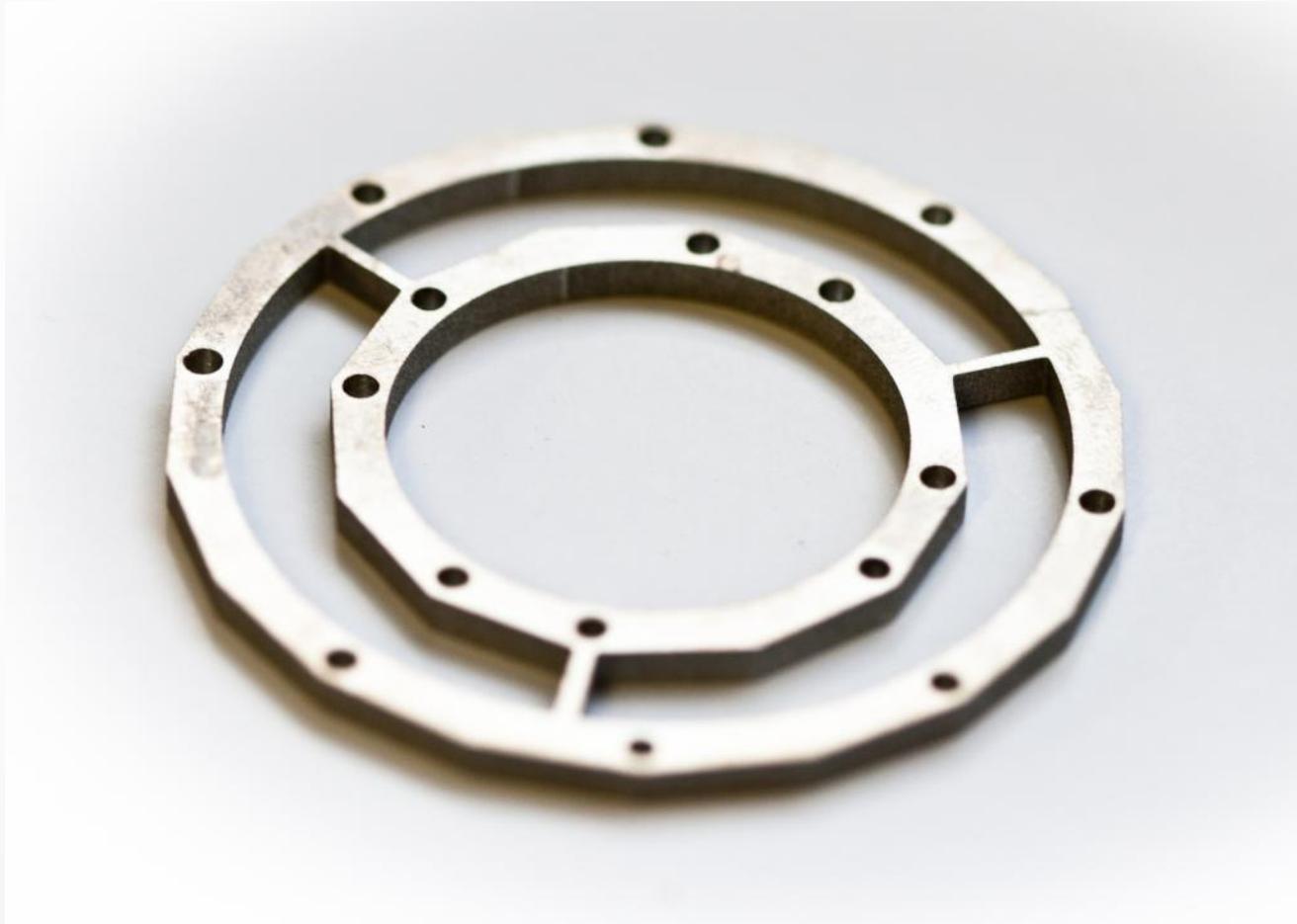
Outer Doublet Design



Modular design

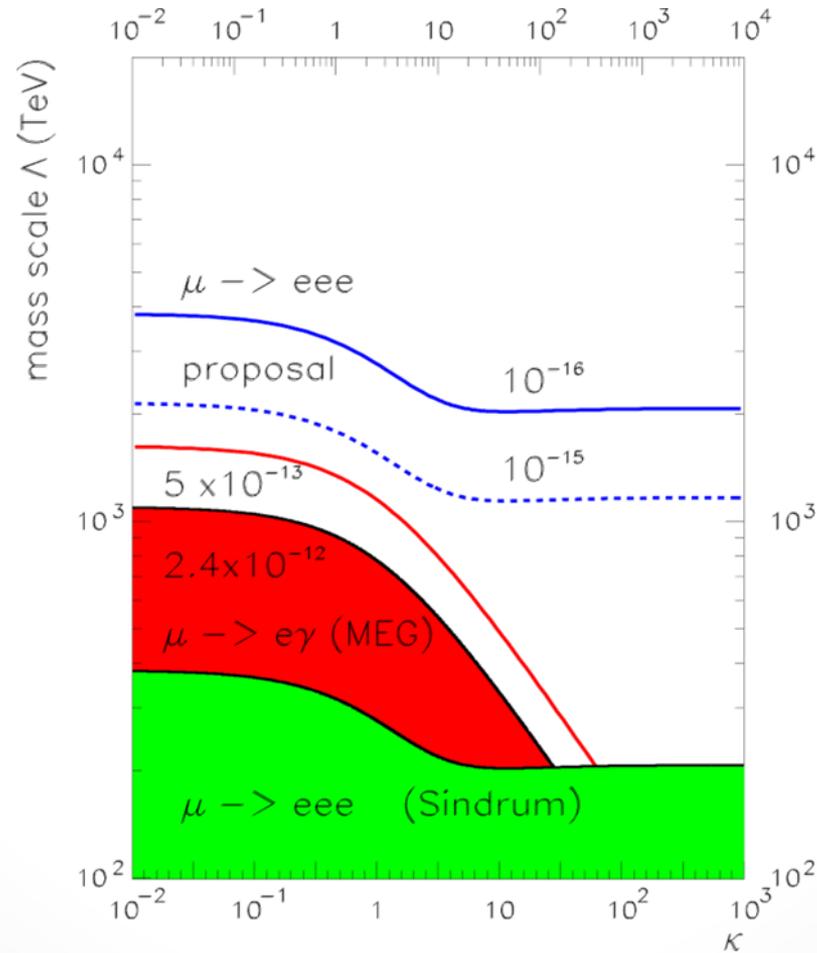
Spokes Between Layers

1+2





Mu3e vs. MEG





Momentum Resolution

- Multiple scattering only
- Current design:
 - 50 μm silicon
 - 50 μm Kapton
 - Helium gas cooling
 - 3 layer fiber tracker

